

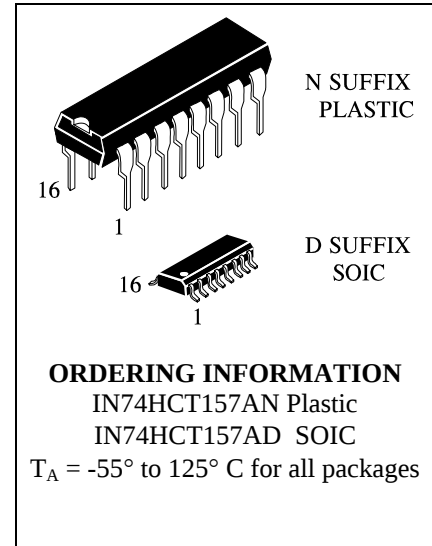
IN74HCT157A

Quad 2-Input Data Selectors/Multiplexer **High-Performance Silicon-Gate CMOS**

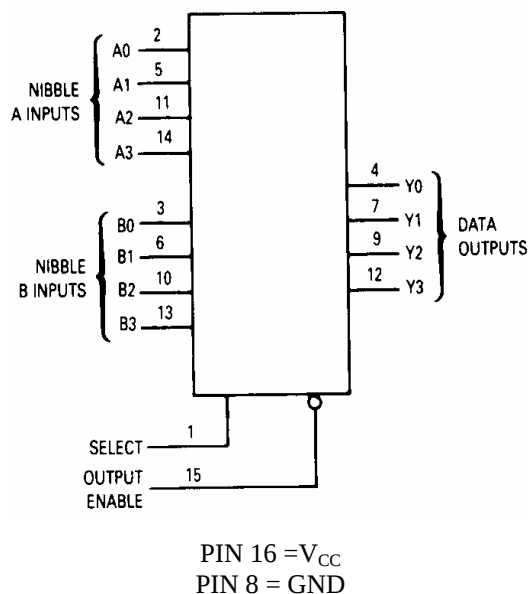
The IN74HCT157A is identical in pinout to the LS/ALS157. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

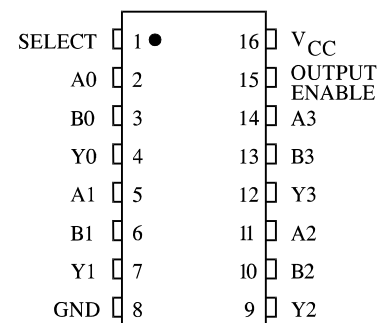
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs Y0-Y3
Output Enable	Select	
H	X	L
L	L	A0-A3
L	H	B0-B3

X=don't care

A0-A3,B0-B3=the levels of the respective Data-Word Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

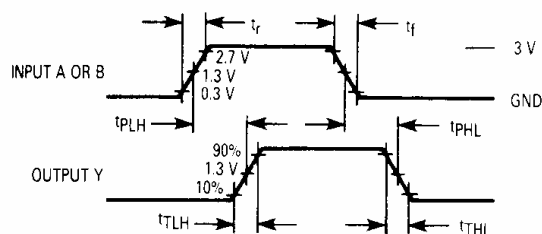
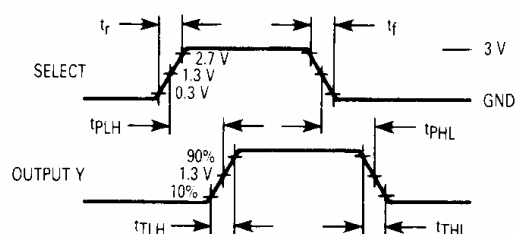
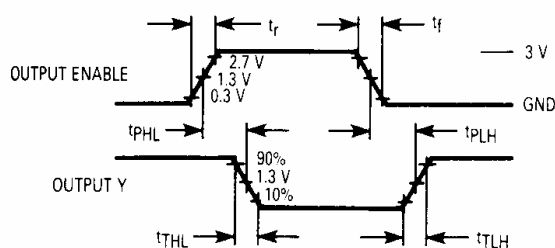
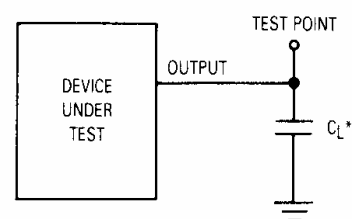
DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{IN} =2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Inputs		-55°C	25°C to 125°C		mA
		I _{OUT} =0μA	5.5	2.9	2.4		

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	27	34	41	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Select to Output Y (Figures 2 and 4)	37	46	56	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Output Enable to Output Y (Figures 3 and 4)	30	38	45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF

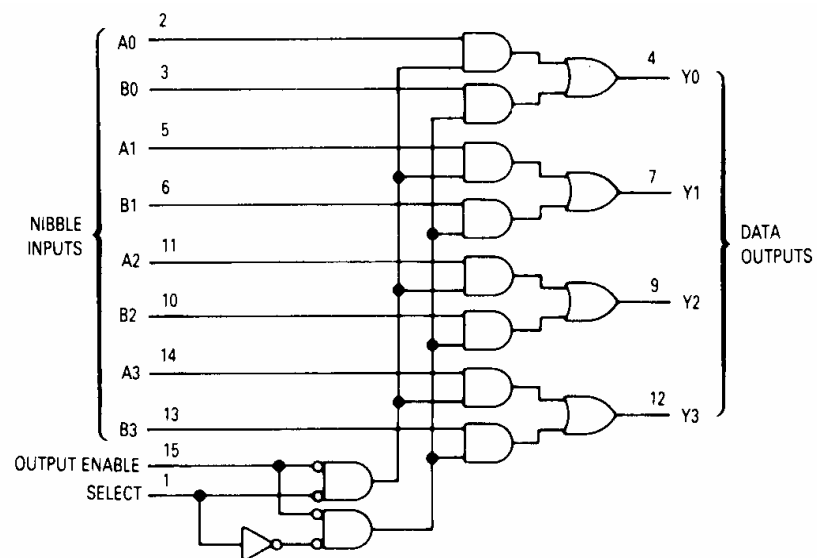
C _{PD}	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @25°C, V _{CC} =5.0 V	pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}	64	


Figure 1. Switching Waveforms

Figure 2. Switching Waveforms

Figure 3. Switching Waveforms


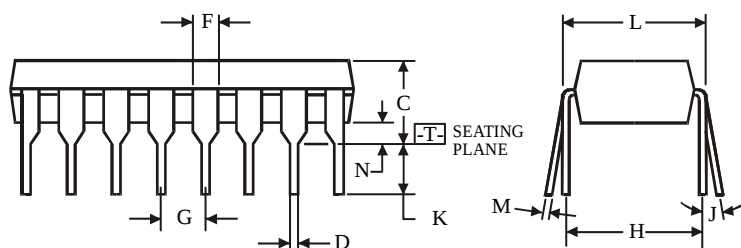
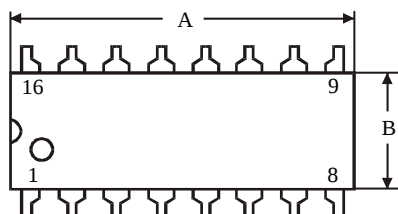
*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



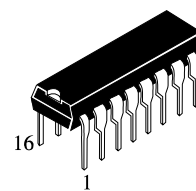
N SUFFIX PLASTIC DIP
(MS - 001BB)



$$\oplus 0.25 (0.010) \text{ (M) } T$$

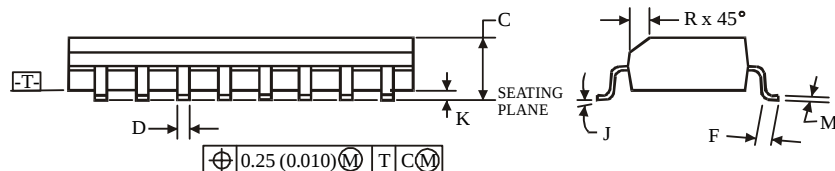
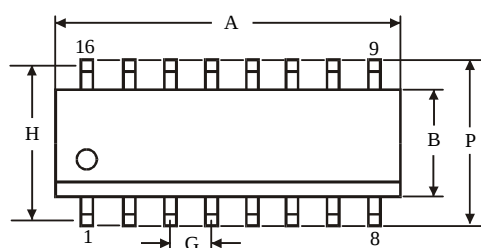
NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.



	Dimension, mm	
Symbol	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

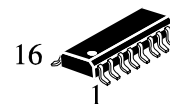
D SUFFIX SOIC
(MS - 012AC)



$$\oplus 0.25 (0.010) \text{ (M) } T \text{ (C) } \text{ (M)}$$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.



	Dimension, mm	
Symbol	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5