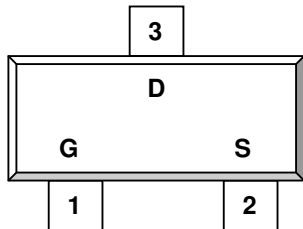
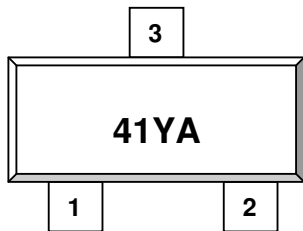


DESCRIPTION

ST2341A is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION
SOT-23-3L**


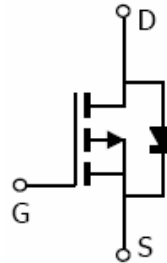
1.Gate 2.Source 3.Drain

**PART MARKING
SOT-23-3L**



Y: Year Code A: Process Code

FEATURE

- -30V/-6.0A, $R_{DS(ON)} = 20\text{m-ohm}$ (Typ.) @VGS = -10V
- -30V/-3.8A, $R_{DS(ON)} = 28\text{m-ohm}$ @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design





ST2341A 


P Channel Enhancement Mode MOSFET

-6.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C -6.0	A
		T _A =70°C -4.5	
Pulsed Drain Current	I _{DM}	-30	A
Continuous Source Current (Diode Conduction)	I _S	-1.0	A
Power Dissipation	P _D	T _A =25°C 1.25	W
		T _A =70°C 0.80	
Operation Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	140	°C/W



ST2341A 

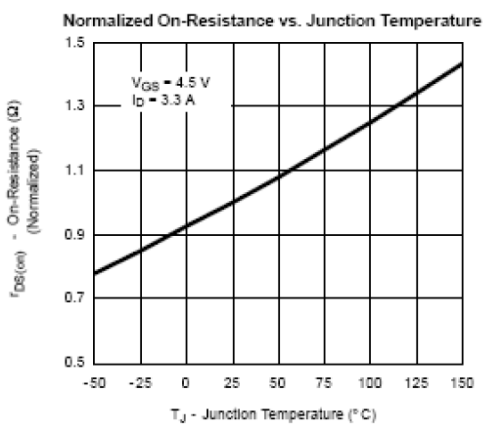
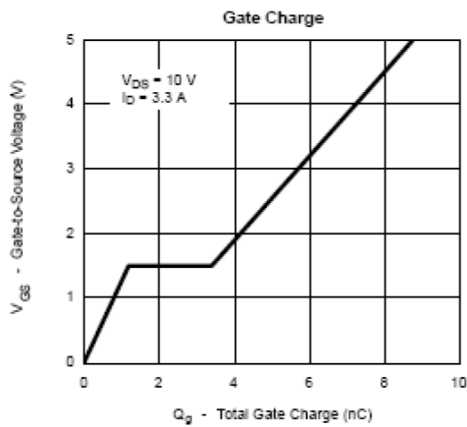
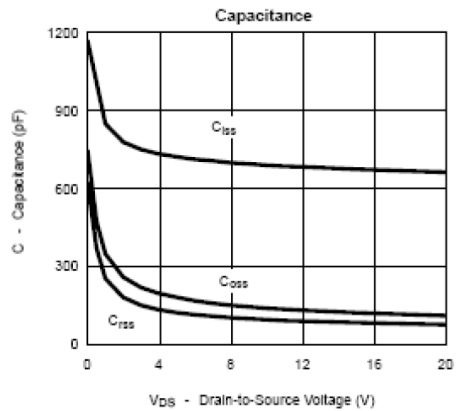
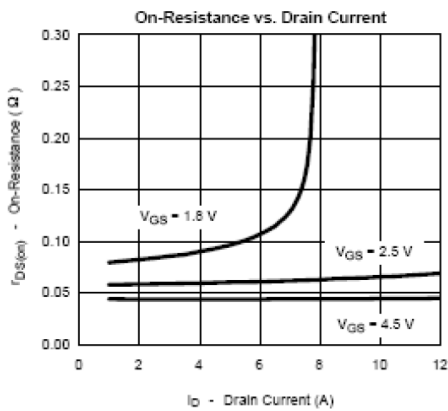
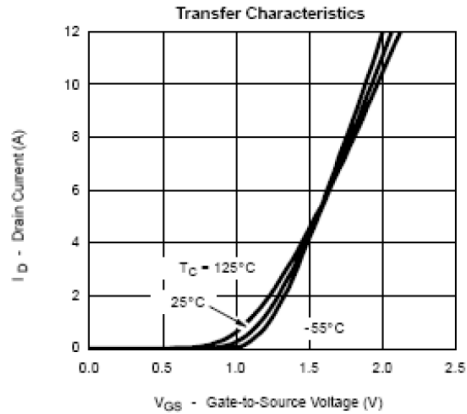
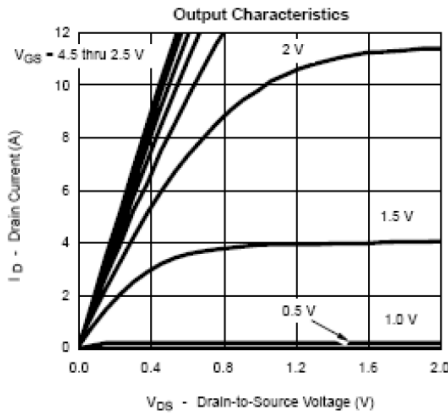
P Channel Enhancement Mode MOSFET

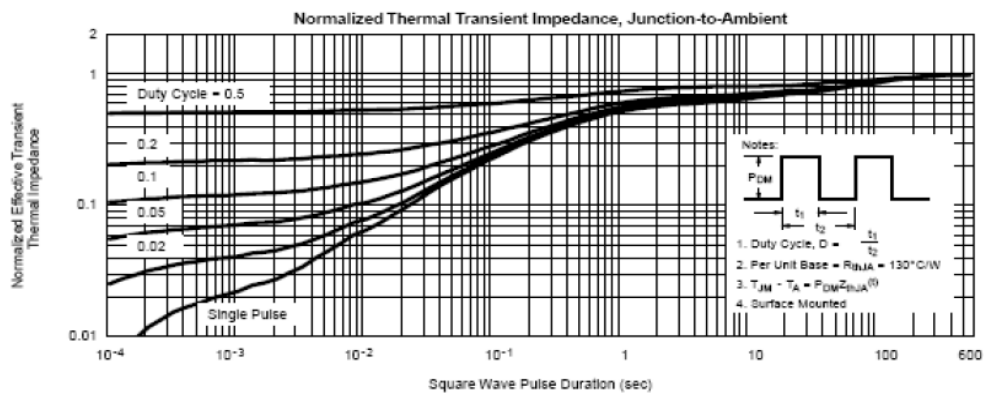
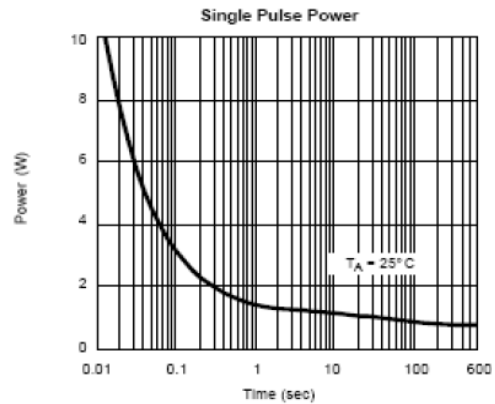
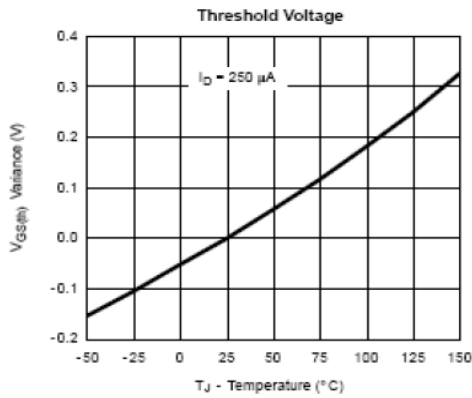
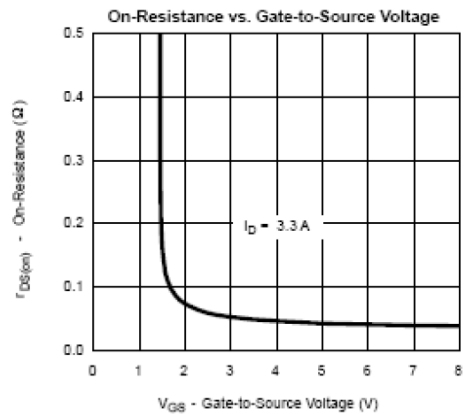
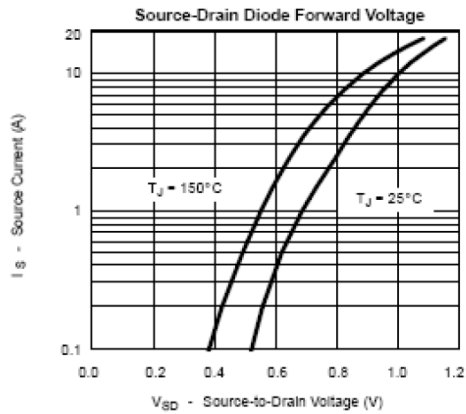
-6.0A

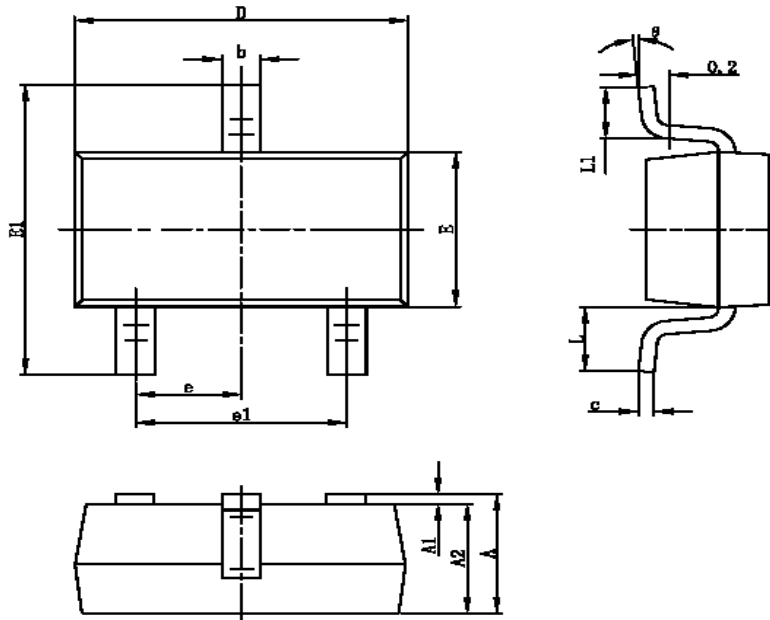
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10, I_D=-6.0A$ $V_{GS}=-4.5V, I_D=-3.8A$		0.025 0.035	0.030 0.042	
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-4V$		3.0		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-6V$ $V_{GS}=-4.5V$ $I_D=-3.3A$		8.0	13	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			2.2		
Input Capacitance	C_{iss}	$V_{DS}=-6.0V$ $V_{GS}=0V$ $F=1MHz$		700		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			120		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=-6V$ $R_L=6\Omega$ $I_D=-1.0A$		15	25	nS
				35	55	
Turn-Off Time	$t_{d(off)}$ t_f	$V_{GEN}=-4.5V$ $R_G=6\Omega$		60	90	
				40	40	

TYPICAL CHARACTERISTICS (25°C Unless noted)



TYPICAL CHARACTERISTICS (25°C Unless noted)


SOT-23-3L PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°