

## Main Features

- Programmable DMUX Ratio:
  - 1:4 Data Rate Max = 1 Gsps
  - $P_D$  (8b/10b) < 4.3/4.7 W (ECL 50  $\Omega$  Output)
  - 1:8 Data Rate Max = 2 Gsps
  - $P_D$  (8b/10b) < 6/6.9 W (ECL 50  $\Omega$  Output)
  - 1:16 With 1 TS8388B or 1 TS83102G0 and 2 DMUX
- Parallel Output Mode
- 8/10-bit
- ECL Differential Input Data
- Data Ready or Data Ready 2 Input Clock
- Input Clock Sampling Delay Adjust
- Single-ended Output Data:
  - Adjustable Common Mode and Swing
  - Logic Threshold Reference Output
  - ECL, PECL, TTL
- Asynchronous Reset
- Synchronous Reset
- ADC and DMUX Multi-channel Applications:
  - Stand-alone Delay Adjust Cell for ADCs Sampling Instant Alignment
- Differential Data Ready Output
- Built-in Self Test (BIST)
- Dual Power Supply  $V_{EE} = -5$  V,  $V_{CC} = 5$  V
- Radiation Tolerance Oriented Design (More Than 100 Krad (Si) Expected)
- Thermally Enhanced CQFP196 Cavity Up Package

## Screening

- Temperature Range:
  - C Grade:  $0^{\circ}\text{C} < T_c; T_j < 90^{\circ}\text{C}$
  - V Grade:  $-40^{\circ}\text{C} < T_c; T_j < 110^{\circ}\text{C}$
  - M Grade:  $-55^{\circ}\text{C} < T_c; T_j < 125^{\circ}\text{C}$
- Standard Screening Level for “C”, “V” and “M” Grades
- ESA SCC 9000 Space Screening Flow for “M” Grade (on Request)

Note: For commercial and industrial temperature ranges the DMUX is also available in a TBGA240 package (P/N: TS81102G0CTP and TS81102G0VTP).

## Description

The TS81102G0 is a monolithic 10-bit high-speed (up to 2 Gsps) demultiplexer. The DMUX is designed to run with all kinds of ADCs and more specifically, it fits perfectly with Atmel's high-speed ADC 8-bit 1 Gsps TS8388B and ADC 10-bit 2 Gsps TS83102G0B. The TS81102G0 uses an innovative architecture, including a sampling delay adjust and tunable output levels. This DMUX allows users to process the high-speed output data stream down to standard signal processors speed (standard FPGAs).



**1:4/1:8 8/10-bit  
2 Gsps  
DMUX**

**TS81102G0FS  
Target  
Specification**

## Summary

For more information please  
contact  
hotline-bdc@gfo.atmel.com

5344AS-BDC-09/03



Note: This is a summary document. A complete document is not available at this time. For more information, please contact your local Atmel sales office.

## Package Description

**Table 1.** Pin Description

Symbol	Pin Number	Description
<b>Power Supplies</b>		
V <sub>CC</sub>	5, 127	Positive 5 V power supply
V <sub>EE</sub>	1, 10, 16, 22, 28, 34, 40, 46, 58, 73, 92, 112, 123, 141, 155, 172, 189, 196	Negative -5 V power supply
V <sub>PLUSD</sub>	53, 61, 64, 69, 78, 83, 87, 95, 98, 101, 102, 106, 109, 115, 122, 126, 130, 133, 136, 144, 145, 148, 152, 160, 163, 167, 177, 181, 184, 193	Output buffer power supply
GND	2, 7, 13, 19, 25, 31, 37, 43, 49, 50, 99, 100, 118, 128, 146, 147	Ground
<b>Analog Input Signals</b>		
DMUXDelAdjCtrl	194	In-phase DMUX clock delay cell control signal
DMUXDelAdjCtrlB	195	Inverted phase DMUX clock delay cell control signal
ADCDelAdjCtrl	47	In-phase stand-alone delay cell control signal
ADCDelAdjCtrlB	48	Inverted phase stand-alone delay cell control signal
SwiAdj	121	Swing adjust function control signal
DIODE	6	Die junction temperature monitoring signal
<b>ECL Input Signals</b>		
ClkIn	21	In-phase input clock signal
ClkInB	20	Inverted phase input clock signal
I[0...9]	9, 12, 15, 18, 24, 27, 30, 33, 36, 39	In-phase input data
I[0...9]B	8, 11, 14, 17, 23, 26, 29, 32, 35, 38	Inverted phase input data
SyncReset	4	In-phase synchronous reset
SyncResetB	3	Inverted phase synchronous reset
ADCDelAdjIn	44	In-phase input of the stand-alone delay cell
ADCDelAdjInB	45	Inverted phase input of the stand-alone delay cell

**Table 1.** Pin Description (Continued)

<b>Output Data</b>		
A[0...9] B[0...9] C[0...9] D[0...9] E[0...9] F[0...9] G[0...9] H[0...9]	179, 180, 182, 183, 185, 186, 187, 188, 190, 191 56, 57, 59, 60, 62, 63, 65, 66, 67, 68 165, 166, 168, 169, 170, 171, 173, 174, 175, 176 71, 72, 74, 75, 76, 77, 79, 80, 81, 82 150, 151, 153, 154, 156, 157, 158, 159, 161, 162 85, 86, 88, 89, 90, 91, 93, 94, 96, 97 131, 132, 134, 135, 137, 138, 139, 140, 142, 143 104, 105, 107, 108, 110, 111, 113, 114, 116, 117	Output data
RefA to RefH	178, 55, 164, 70, 149, 84, 129, 103	Reference outputs (tied to the common mode voltage of each port)
DR	125	In-phase Data Ready Signal (centered in the output data, frequency = output data frequency/2)
DRB	124	Inverted phase Data Ready Signal (centered in the output data, frequency = output data frequency /2)
<b>TTL Input Signals</b>		
AsyncReset	192	Asynchronous reset (active high)
ClkInType	51	Input clock type: DR mode = Logic 1 DR/2 mode = Logic 0
RatioSel	120	DMUX ratio selection: 1:4 mode = Logic 1 1:8 mode = Logic 0
NbBit	52	Number of bits selection 10 bits = Logic 1 8 bits = Logic 0
BIST	54	Built-in self-test mode (active low)
<b>Other Output Signals</b>		
ADCDeAdjOUT	41	In-phase output of the stand-alone delay cell
ADCDeAdjOUTB	42	Inverted phase output of the stand-alone delay cell

Figure 1. Pinout Top View

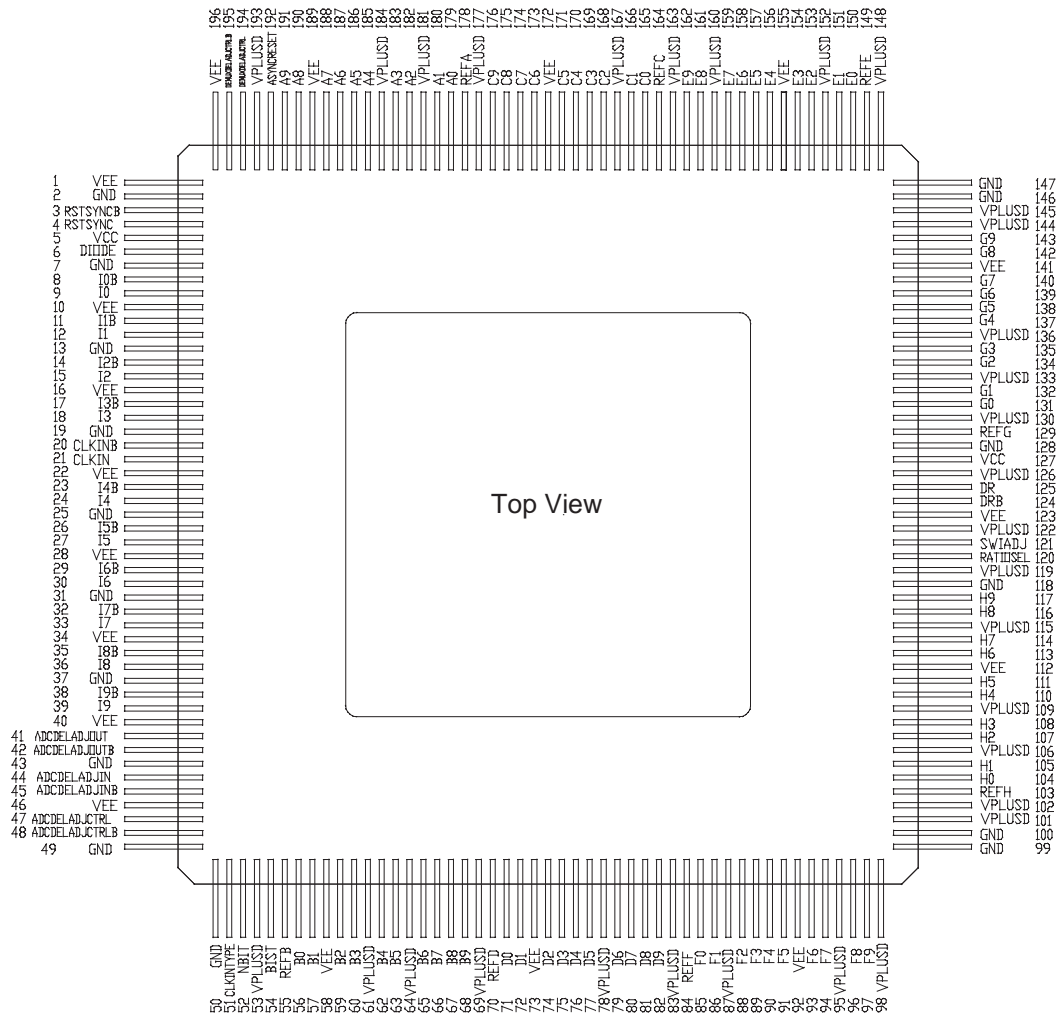
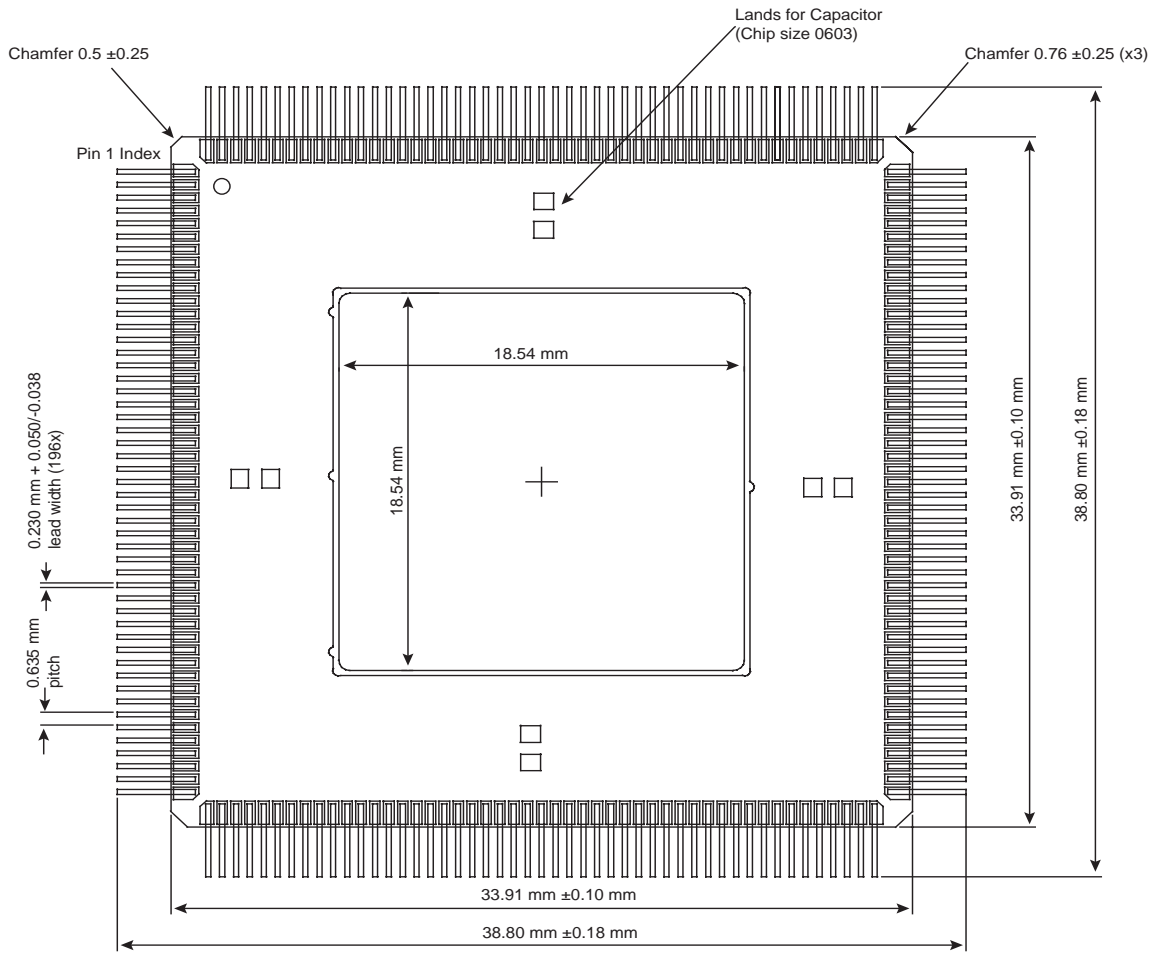
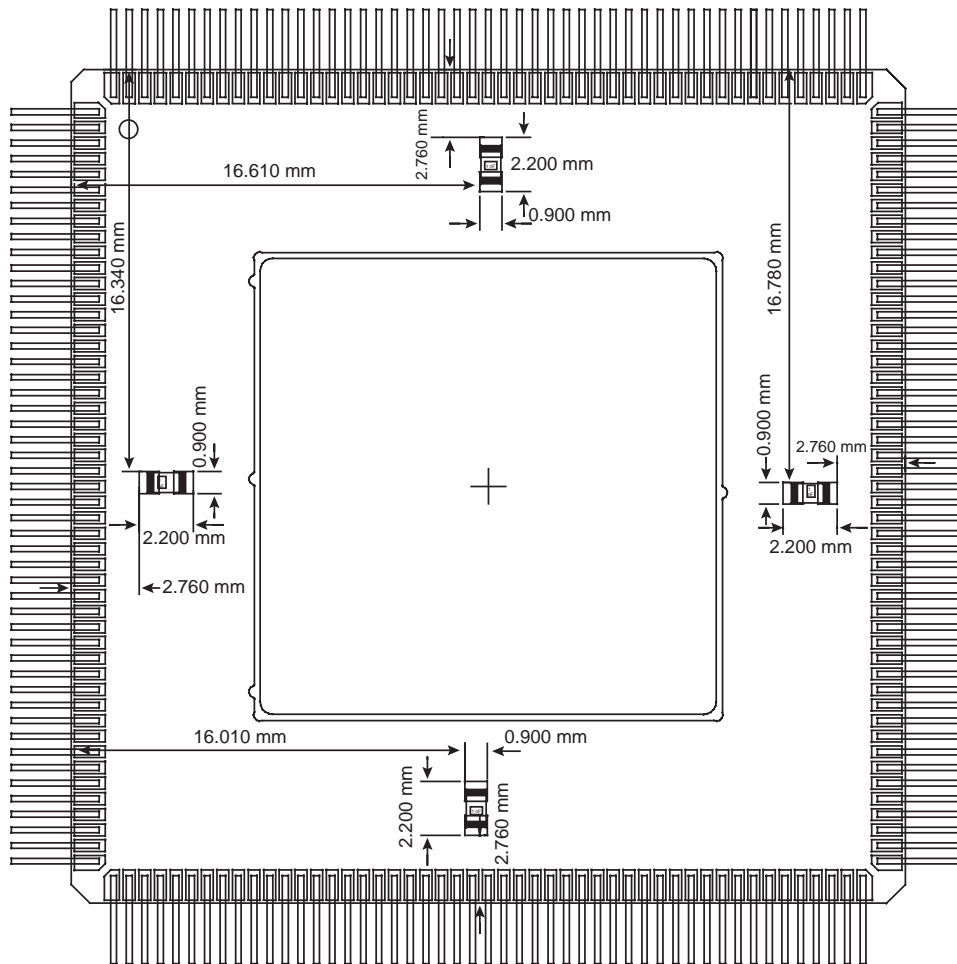


Figure 2. CQFP 196 Package Top View



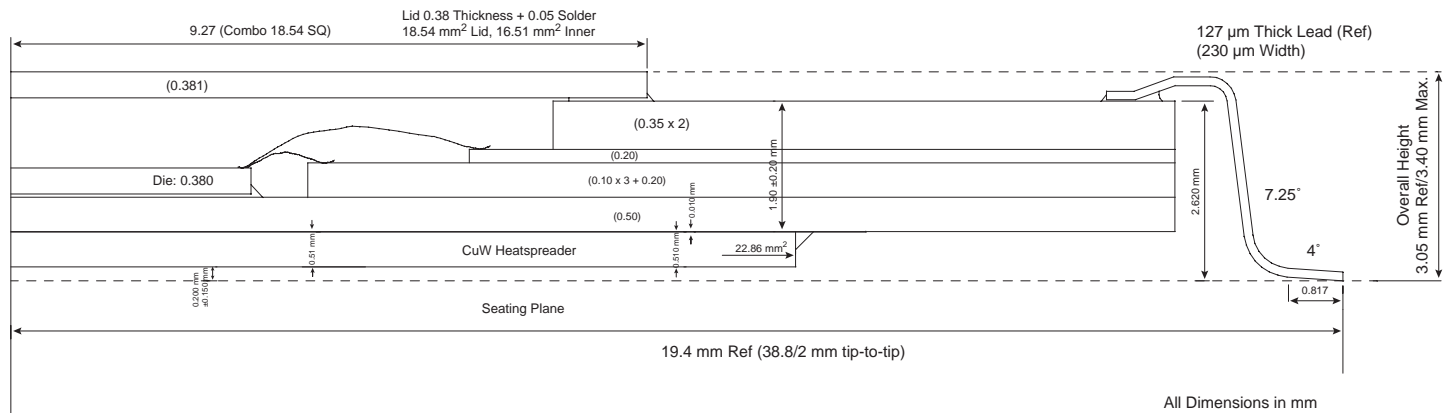
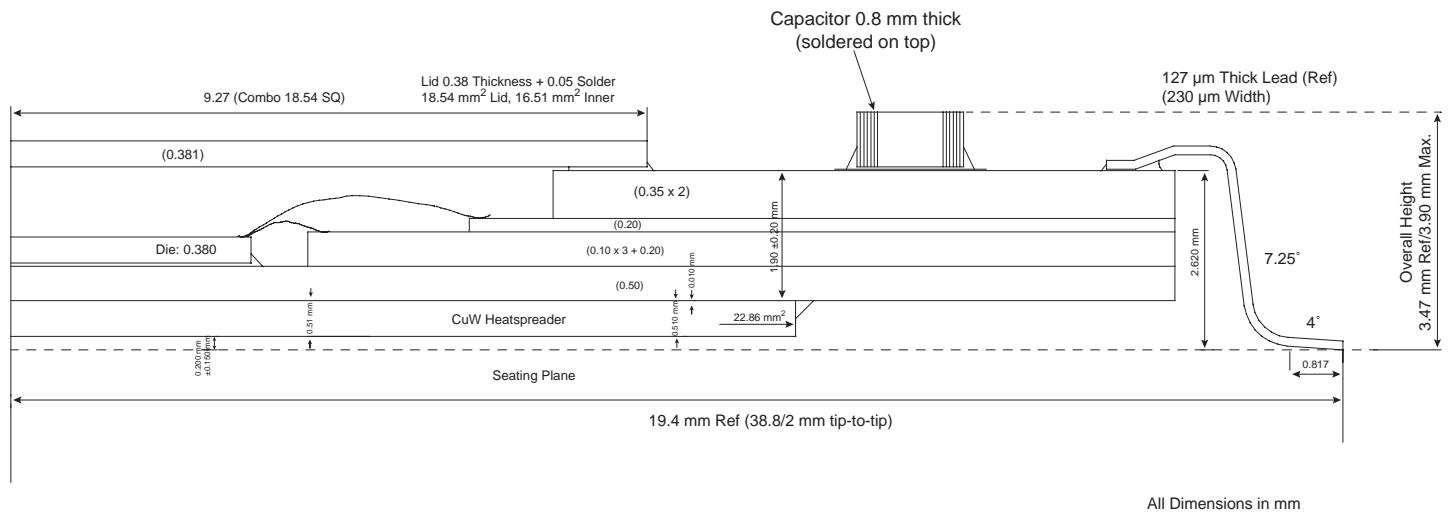
Note: Package: black Al<sub>2</sub>O<sub>3</sub> ceramic  
 Leads: Kovar, Ni and Au plating  
 Lid: Kovar, Ni and Au plating  
 Heatspreader on bottom: CuW with Ni and Au plating

**Figure 3. CQFP 196 On-package Capacitor Location**



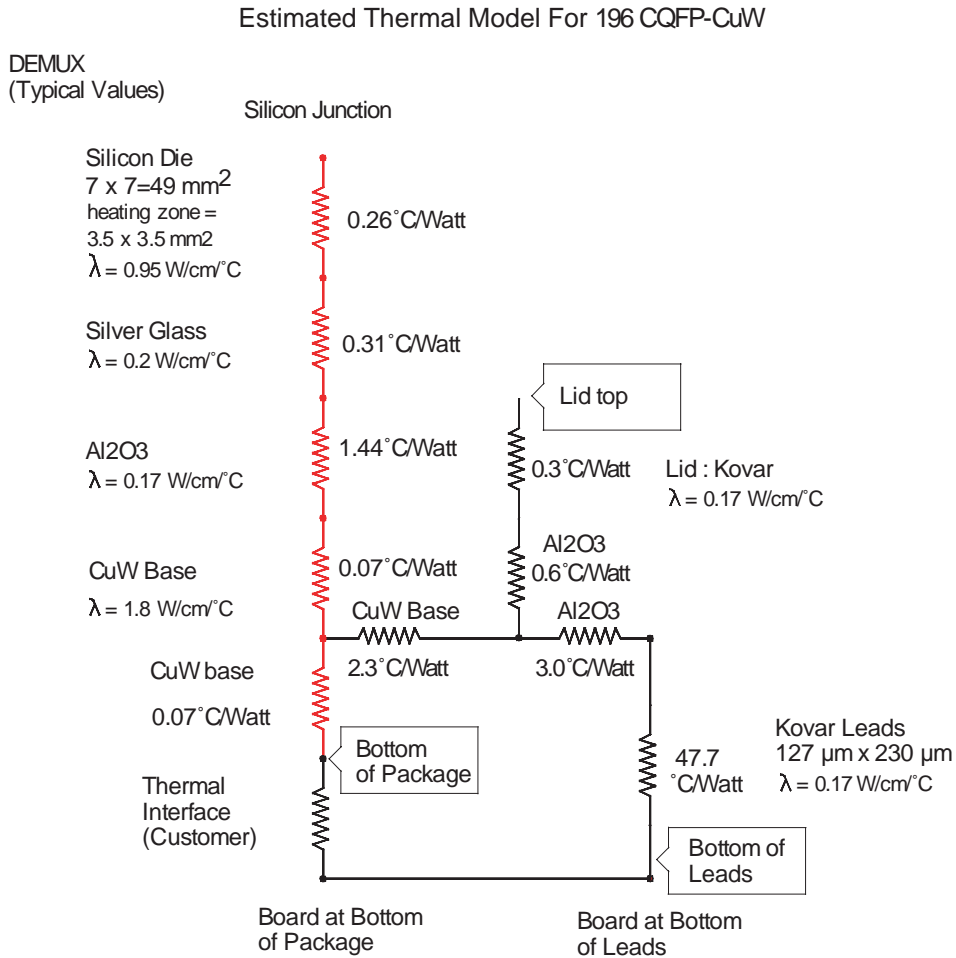
Note: The on-package decoupling capacitors are an option only. Their use will be confirmed after full characterization.

Figure 4. Detailed Cross Section of DEMUX in CQFP196 Package



Note: The on-package decoupling capacitors are an option only. Their use will be confirmed after full characterization of the packaged device.

**Figure 5. Thermal Characteristics**



Thermal Resistance Junction to bottom of case =  
 $0.26 + 0.31 + 1.44 + 0.07 + 0.07 = 2.15^\circ\text{C/Watt}$   
 (customer thermal interface excluded)



**Ordering Information**

**Table 2.** Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
TS81102G0CFS	CQFP 196	“C” grade 0°C < Tc; Tj < 90°C	Standard	
TS81102G0VFS	CQFP 196	“V” grade -40°C < Tc; Tj < 110°C	Standard	
TS81102G0MFS	CQFP 196	“M” grade -55°C < Tc; Tj < 125°C	Standard	
TS81102G0MFS9Nxy	CQFP 196	“M” grade -55°C < Tc; Tj < 125°C	<ul style="list-style-type: none"> <li>▪ ESA/SCC9000 screening</li> <li>▪ Non ESA/SCC qualified</li> <li>▪ x = B or C for respectively level B or C of ESA/SCC9000</li> <li>▪ y = 1, 2 or 3 for respectively Lot Acceptance Test 1, 2 or 3</li> </ul>	Please contact Marketing



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