4-Mbit (128 K × 36) Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the need to use $\overline{OE}$
- Byte write capability
- 128 K × 36 common I/O architecture
- 3.3 V power supply (V_{DD})
- 2.5 V / 3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 2.8 ns (for 200-MHz device)
- Clock enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self-timed writes
- Asynchronous output enable ($\overline{OE}$)
- Available in Pb-free 100-pin TQFP package, Pb-free and non Pb-free 119-ball BGA package
- Burst capability – linear or interleaved burst order
- "ZZ" sleep mode option

Functional Description

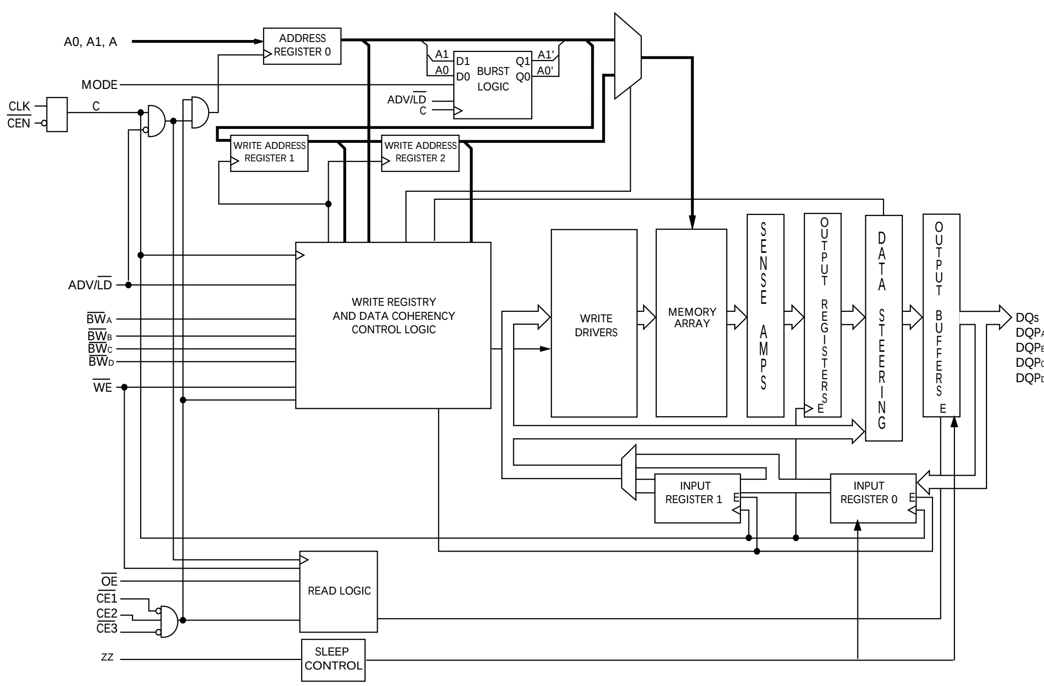
The CY7C1350G is a 3.3 V, 128 K × 36 synchronous-pipelined burst SRAM designed specifically to support unlimited true back-to-back read/write operations without the insertion of wait states. The CY7C1350G is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of the SRAM, especially in systems that require frequent write/read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal, which, when deasserted, suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 2.8 ns (200-MHz device).

Write operations are controlled by the four byte write select ($\overline{BW}_{[A:D]}$) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. In order to avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Logic Block Diagram



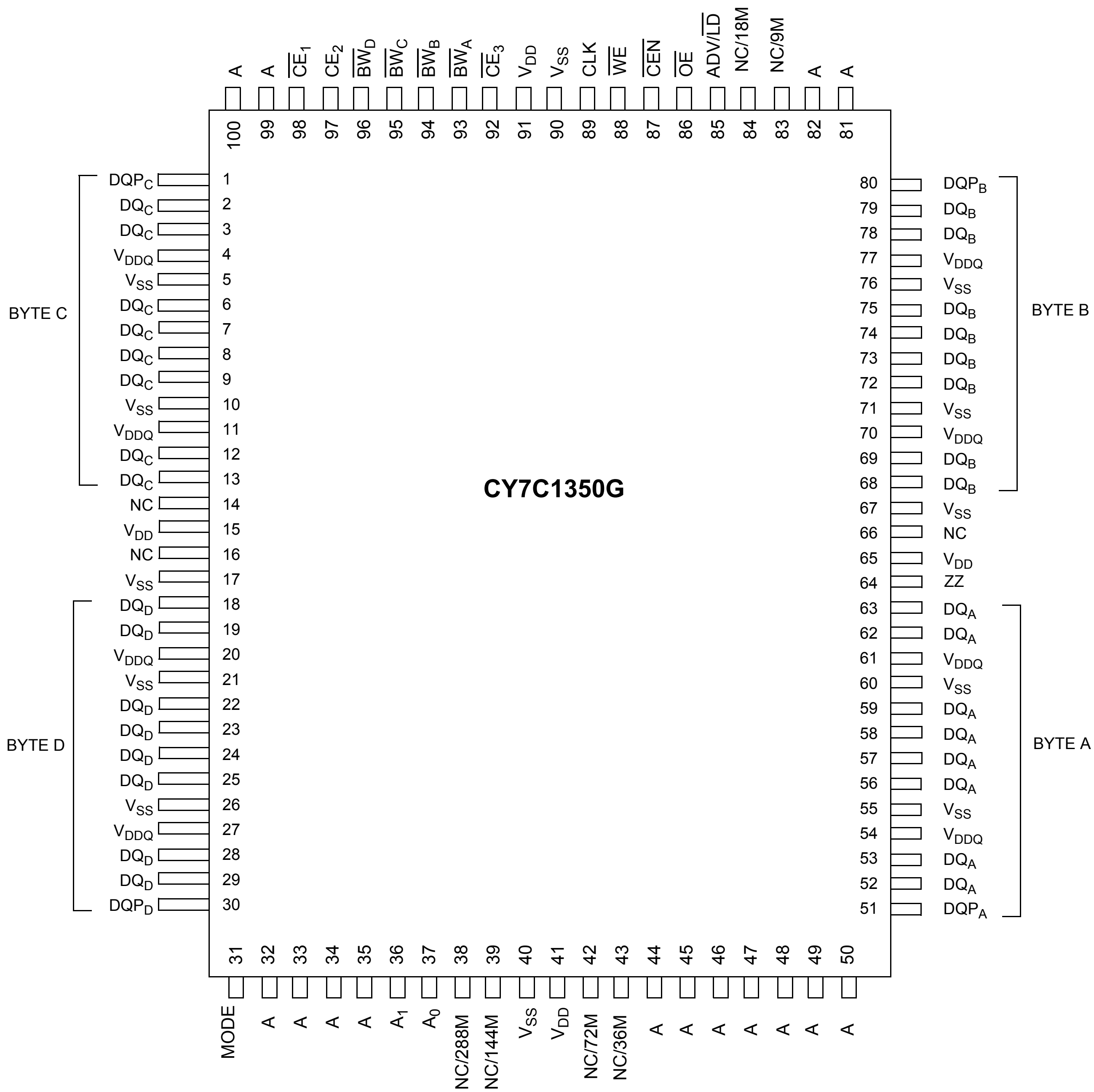
Contents

Selection Guide

Description	200 MHz	133 MHz	Unit
Maximum access time	2.8	4.0	ns
Maximum operating current	265	225	mA
Maximum CMOS standby current	40	40	mA

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Configurations *(continued)*

Figure 2. 119-Ball BGA (14 × 22 × 2.4 mm) pinout

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW_C}$	NC/9M	$\overline{BW_B}$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{WE}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW_D}$	NC	$\overline{BW_A}$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the 128 K address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_{[A:D]}$	Input-synchronous	**Byte write inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-synchronous	**Advance/load input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input-synchronous	**Clock enable input, active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input-asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQs	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the address during the clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tristate condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:D]}$	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:D]}$ is controlled by $\overline{BW}_{[A:D]}$ correspondingly.
MODE	Input strap pin	**Mode input. Selects the burst order of the device**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**.
NC	–	**No Connects**. Not internally connected to the die. 9M, 18M, 36M, 72M, 144M and 288M are address expansion pins in this device and will be used as address pins in their respective densities.

Functional Overview

The CY7C1350G is a synchronous-pipelined burst SRAM designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.8 ns (200-MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If clock enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). $\overline{BW}_{[A:D]}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, (3) the write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus, provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will tristate following the next clock rise.

Burst Read Accesses

The CY7C1350G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Accesses section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the address inputs is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and $DQP_{[A:D]}$. In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQs and $DQP_{[A:D]}$ (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}_{[A:D]}$ signals. The CY7C1350G provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}_{[A:D]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1350G is a common I/O device, data should not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and $DQP_{[A:D]}$ inputs. Doing so will tristate the output drivers. As a safety precaution, DQs and $DQP_{[A:D]}$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1350G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Accesses section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}_{[A:D]}$ inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	ZZ $\geq V_{DD} - 0.2$ V	–	40	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to snooze current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit snooze current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for part CY7C1350G is as follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L–H	Tristate
Continue deselect cycle	None	X	L	H	X	X	X	L	L–H	Tristate
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L–H	Data out (Q)
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L–H	Data out (Q)
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L–H	Tristate
Dummy read (continue burst)	Next	X	L	H	X	X	H	L	L–H	Tristate
Write cycle (begin burst)	External	L	L	L	L	L	X	L	L–H	Data in (D)
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L–H	Data in (D)
NOP/WRITE ABORT (begin burst)	None	L	L	L	L	H	X	L	L–H	Tristate
WRITE ABORT (continue burst)	Next	X	L	H	X	H	X	L	L–H	Tristate
IGNORE CLOCK EDGE (stall)	Current	X	L	X	X	X	X	H	L–H	–
SNOOZE MODE	None	X	H	X	X	X	X	X	X	Tristate

Notes
1. X ="Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{CE}$ stands for all chip enables active. $\overline{BW}_X$ = L signifies at least one byte write select is active, $\overline{BW}_X$ = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See Write Cycle Descriptions table.
3. When a write cycle is detected, all DQs are tri-stated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device will power-up deselected and the DQs in a tristate condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_{[A:D]}$ = tristate when $\overline{OE}$ is inactive or when the device is deselected, and DQs and $DQP_{[A:D]}$ = data when $\overline{OE}$ is active.

Partial Truth Table for Read/Write

The Partial Truth Table for read or write for part CY7C1350G is as follows. [8, 9, 10]

Function	$\overline{WE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	X	X	X	X
Write – no bytes written	L	H	H	H	H
Write byte A – (DQ_A and DQP_A)	L	H	H	H	L
Write byte B – (DQ_B and DQP_B)	L	H	H	L	H
Write bytes A, B	L	H	H	L	L
Write byte C – (DQ_C and DQP_C)	L	H	L	H	H
Write bytes C, A	L	H	L	H	L
Write bytes C, B	L	H	L	L	H
Write bytes C, B, A	L	H	L	L	L
Write byte D – (DQ_D and DQP_D)	L	L	H	H	H
Write bytes D, A	L	L	H	H	L
Write bytes D, B	L	L	H	L	H
Write bytes D, B, A	L	L	H	L	L
Write bytes D, C	L	L	L	H	H
Write bytes D, C, A	L	L	L	H	L
Write bytes D, C, B	L	L	L	L	H
Write all bytes	L	L	L	L	L

Notes

8. X ="Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{CE}$ stands for all chip enables active. $\overline{BW}_X$ = L signifies at least one byte write select is active, $\overline{BW}_X$ = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See Write Cycle Descriptions table.
10. Table only lists a partial listing of the byte write combinations. Any combination of BW_X is valid. Appropriate write will be done on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ....–65 °C to +150 °C

Ambient temperature with power applied ....–55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .... –0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ....–0.5 V to $+V_{DD}$

DC voltage applied to outputs in tristate .... –0.5 V to V_{DDQ} + 0.5 V

DC input voltage ....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ....> 2001 V

Latch up current ....> 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [11, 12]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL}= 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL}=1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage [11]	V_{DDQ} = 3.3 V		2.0	V_{DD} + 0.3 V	V
		V_{DDQ} = 2.5 V		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage [11]	V_{DDQ} = 3.3 V		–0.3	0.8	V
		V_{DDQ} = 2.5 V		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5-ns cycle, 200 MHz	–	265	mA
			7.5-ns cycle, 133 MHz	–	225	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}	5-ns cycle, 200 MHz	–	110	mA
			7.5-ns cycle, 133 MHz	–	90	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	All speeds	–	40	mA

Notes

11. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
12. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [11, 12]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX} = $1/t_{CYC}$	5-ns cycle, 200 MHz	–	95	mA
			7.5-ns cycle, 133 MHz	–	75	mA
I_{SB4}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speeds	–	45	mA

Capacitance

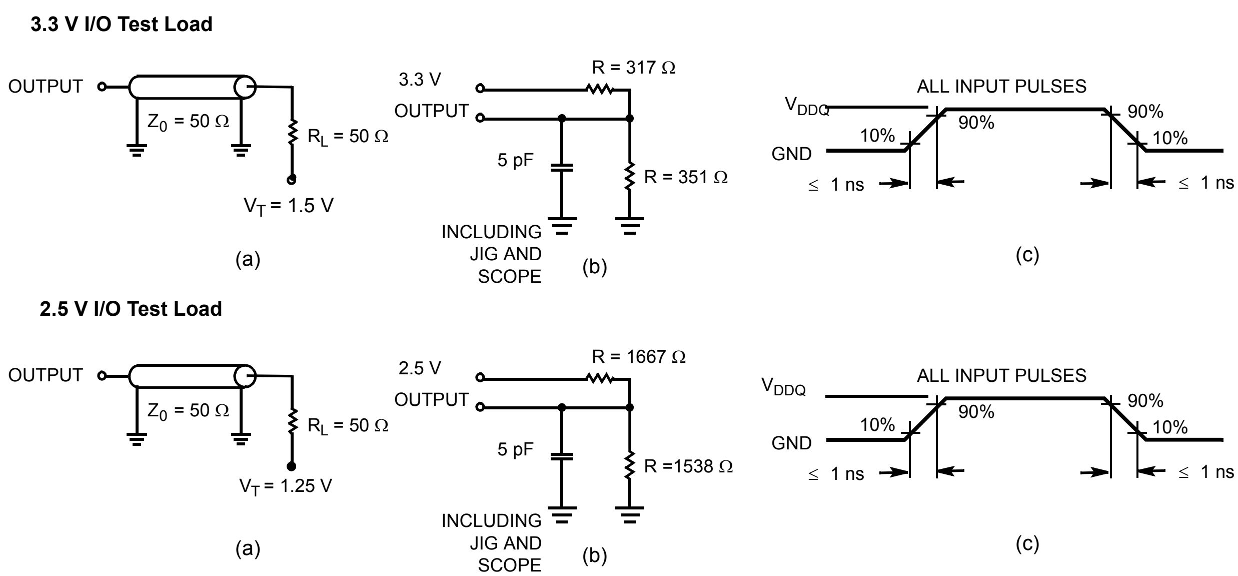
Parameter [13]	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 3.3 V	5	5	pF
C_{CLK}	Clock input capacitance		5	5	pF
$C_{I/O}$	Input/Output capacitance		5	7	pF

Thermal Resistance

Parameter [13]	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	14.0	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note

13. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range

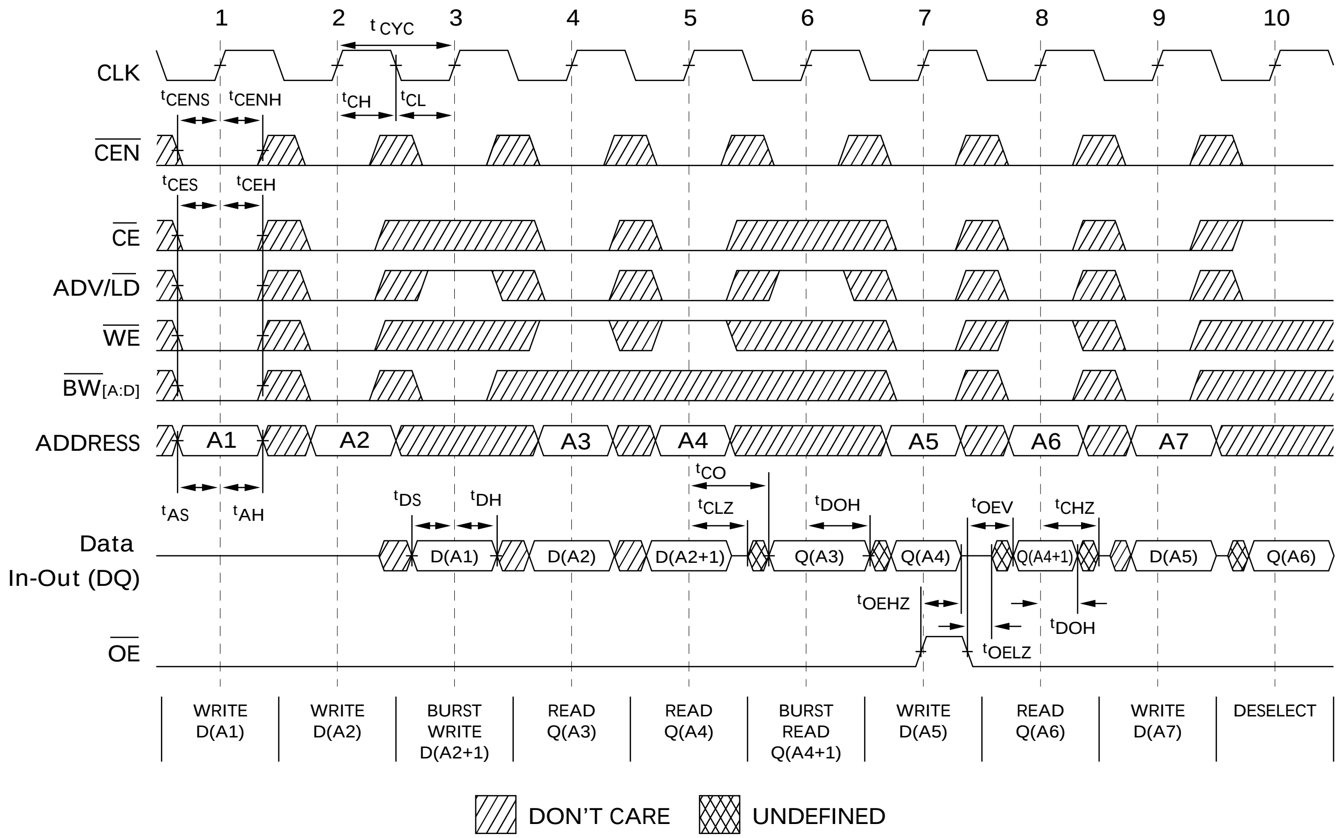
Parameter [14, 15]	Description	-200		-133		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [16]	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	5.0	–	7.5	–	ns
t_{CH}	Clock HIGH	2.0	–	3.0	–	ns
t_{CL}	Clock LOW	2.0	–	3.0	–	ns
Output Times						
t_{CO}	Data output valid after CLK rise	–	2.8	–	4.0	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	1.5	–	ns
t_{CLZ}	Clock to low Z [17, 18, 19]	0	–	0	–	ns
t_{CHZ}	Clock to high Z [17, 18, 19]	–	2.8	–	4.0	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	2.8	–	4.0	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [17, 18, 19]	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [17, 18, 19]	–	2.8	–	4.0	ns
Setup Times						
t_{AS}	Address setup before CLK rise	1.2	–	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.2	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BW}_X$ setup before CLK rise	1.2	–	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.2	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.2	–	1.5	–	ns
t_{CES}	Chip enable setup before CLK rise	1.2	–	1.5	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.5	–	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BW}_X$ hold after CLK rise	0.5	–	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

Notes

14. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
15. Test conditions shown in (a) of Figure 3 on page 11 unless otherwise noted.
16. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a Read or Write operation can be initiated.
17. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 3 on page 11. Transition is measured ±200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve tristate prior to low Z under the same system conditions.
19. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 4. Read/Write Timing [20, 21, 22]



Notes

20. For this waveform ZZ is tied LOW.
21. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
22. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms *(continued)*

Figure 5. NOP, STALL, and DESELECT Cycles [23, 24, 25]

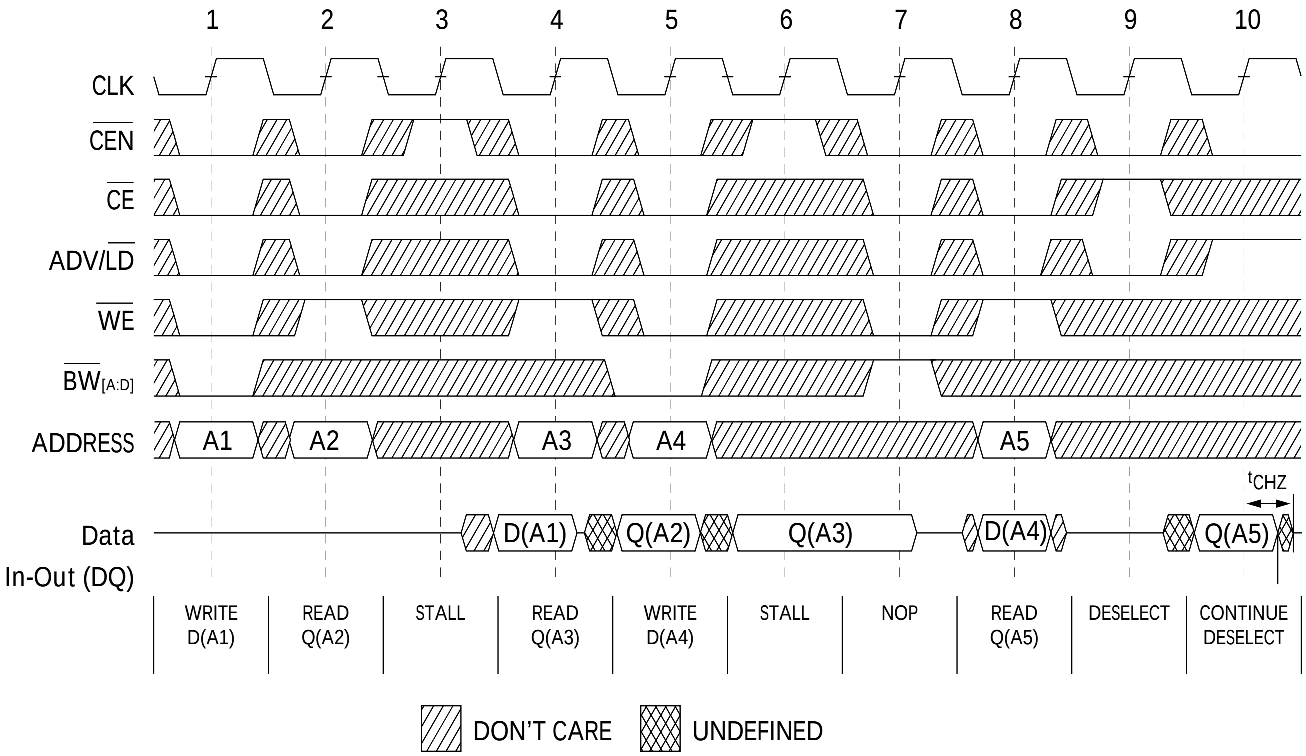
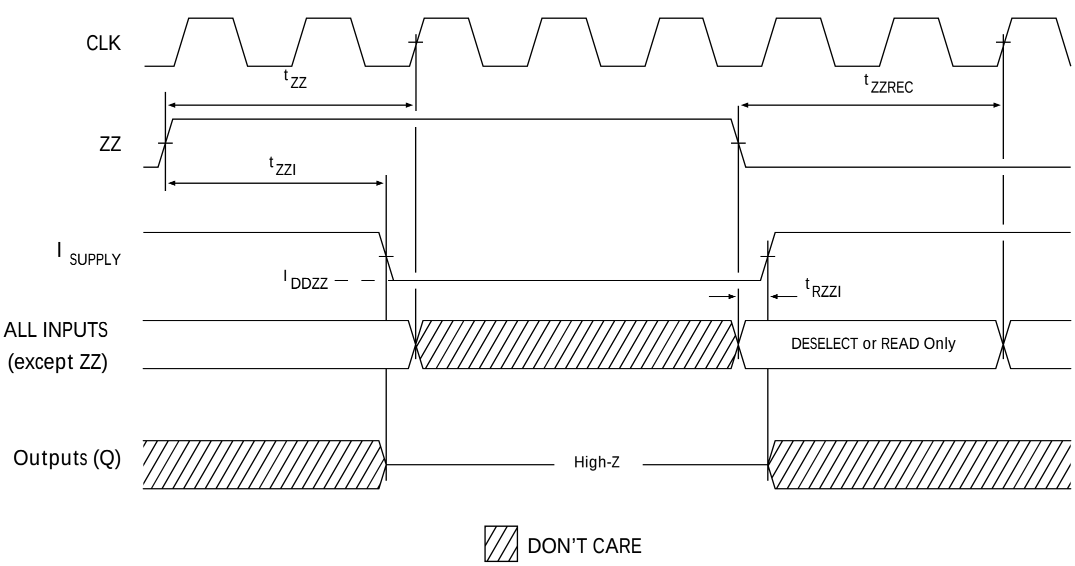


Figure 6. ZZ Mode Timing [26, 27]



Notes
23. For this waveform ZZ is tied LOW.
24. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
25. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
26. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
27. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

The following table contains only the list of parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1350G-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1350G-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial
	CY7C1350G-133BGXC	51-85115	119-ball BGA (14 × 22 × 2.4 mm) Pb-free	Commercial
200	CY7C1350G-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1350G-200AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions

CY 7 C 1350 G - XXX XX X X

Temperature Range: X = C or I
C = Commercial; I = Industrial

Pb-free

Package Type: XX = A or BG
A = 100-pin TQFP; BG = 119-ball BGA

Speed Grade: XXX = 133 MHz or 200 MHz

Process Technology: G ≥ 90 nm

Part Identifier: 1350 = PL, 128 Kb × 36 (4 Mb)

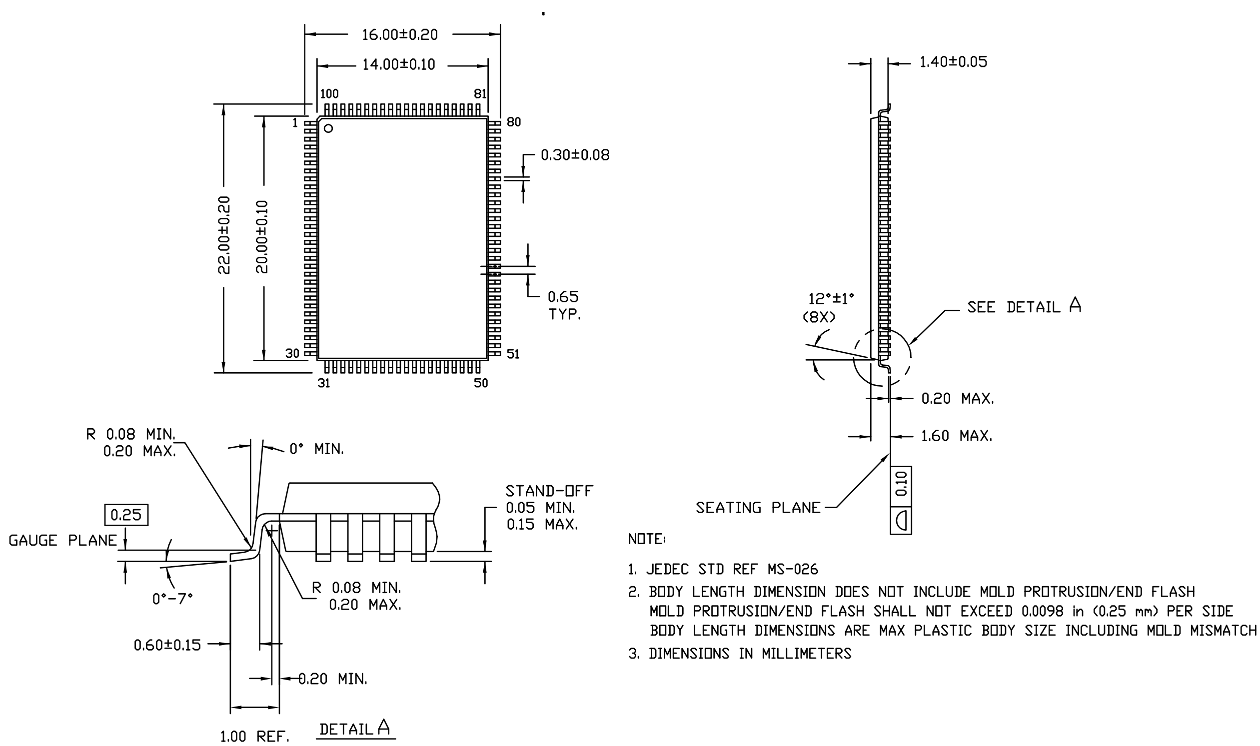
Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagrams

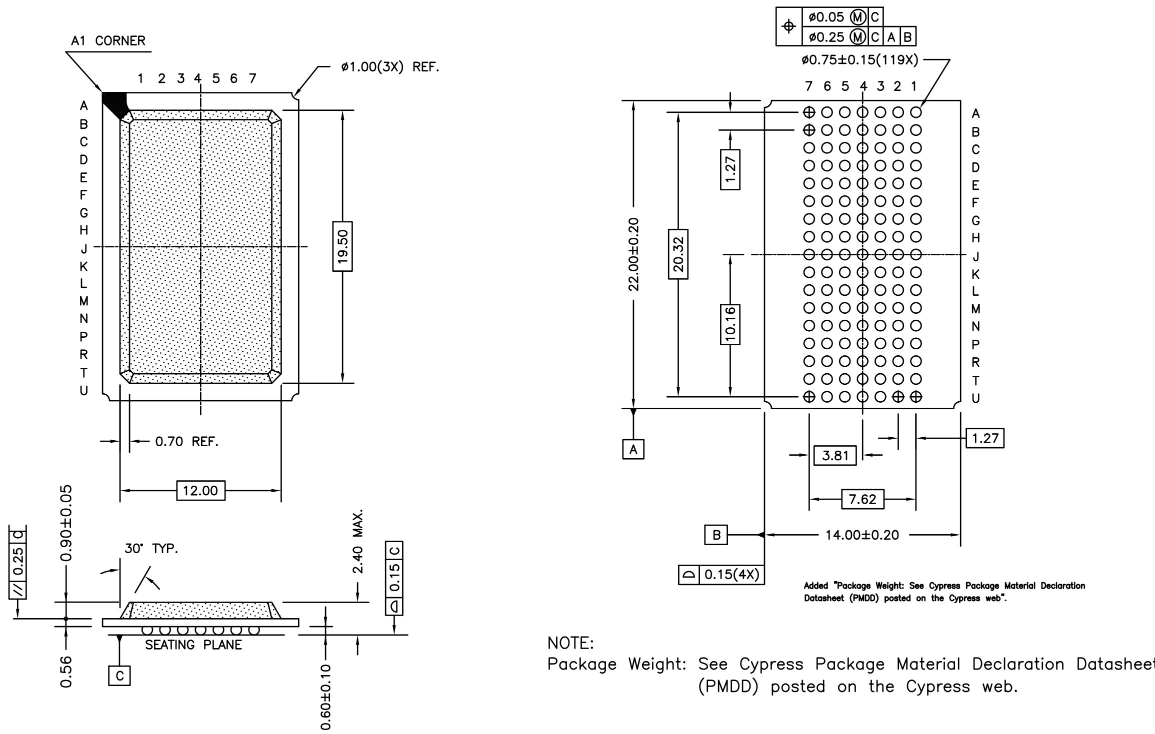
Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *D

Package Diagrams

Figure 8. 119-ball BGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
BGA	ball grid array
$\overline{CE}$	chip enable
$\overline{CEN}$	clock enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
I/O	input/output
JEDEC	joint electron devices engineering council
NoBL	No Bus Latency
$\overline{OE}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nm	nanometer
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1350G, 4-Mbit (128 K × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 38-05524				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224380	See ECN	RKF	New data sheet.
*A	276690	See ECN	VBL	Updated Ordering Information (Changed TQFP package to Pb-free TQFP package, added comment of BGA Pb-free package availability below the table).
*B	332895	See ECN	SYT	Changed status from Preliminary to Final. Updated Features (Removed 225 MHz and 100 MHz frequencies related information). Updated Selection Guide (Removed 225 MHz and 100 MHz frequencies related information). Updated Pin Configurations (Modified Address Expansion balls in the pinouts for 119-ball BGA Package as per JEDEC standards). Updated Electrical Characteristics (Updated test conditions for V_{OL} and V_{OH} parameters, removed 225 MHz and 100 MHz frequencies related information). Updated Thermal Resistance (Replaced TBD's for Θ_{JA} and Θ_{JC} to their respective values). Updated Switching Characteristics (Removed 225 MHz and 100 MHz frequencies related information). Updated Ordering Information (By removing Shaded Parts, changed the package name for 100-pin TQFP from A100RA to A101, removed comment on the availability of BGA Pb-free package).
*C	351194	See ECN	PCI	Updated Ordering Information (Updated part numbers).
*D	419264	See ECN	RXU	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court". Updated Electrical Characteristics (Updated Note 12 (Changed test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$), changed "Input Load Current except ZZ and MODE" to "Input Leakage Current except ZZ and MODE"). Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). Updated Package Diagrams.
*E	419705	See ECN	RXU	Updated Features (Added 100 MHz frequency related information). Updated Selection Guide (Added 100 MHz frequency related information). Updated Electrical Characteristics (Added 100 MHz frequency related information). Updated Switching Characteristics (Added 100 MHz frequency related information).
*F	480368	See ECN	VKN	Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated Ordering Information (Updated part numbers).
*G	2896584	03/20/2010	NJY	Updated Ordering Information (Removed obsolete part numbers). Updated Package Diagrams.
*H	3053085	10/08/2010	NJY	Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*I	3211361	03/31/2011	CS	Updated Ordering Information (Added CY7C1350G-133BGXC part number).
*J	3353361	08/24/2011	PRIT	Updated Functional Description (Updated Note as "For best practices recommendations, refer to SRAM System Design Guidelines." and referred the note in same place in this section). Updated Package Diagrams.

Document History Page *(continued)*

Document Title: CY7C1350G, 4-Mbit (128 K × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 38-05524				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*K	3590312	05/10/2012	NJY / PRIT	Updated Features (Removed 250 MHz, 166 MHz and 100 MHz frequencies related information). Updated Functional Description (Removed the Note "For best practices recommendations, refer to SRAM System Design Guidelines."). Updated Selection Guide (Removed 250 MHz, 166 MHz and 100 MHz frequencies related information). Updated Functional Overview (Removed 250 MHz, 166 MHz and 100 MHz frequencies related information). Updated Electrical Characteristics (Removed 250 MHz, 166 MHz and 100 MHz frequencies related information). Updated Switching Characteristics (Removed 250 MHz, 166 MHz and 100 MHz frequencies related information).
*L	3753416	09/24/2012	PRIT	Updated Package Diagrams (spec 51-85115 (Changed revision from *C to *D)).

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5