July 1999

FAIRCHILD SEMICONDUCTOR™

FDC6308P

Dual P-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V - 12V).

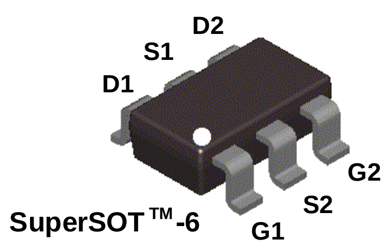
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

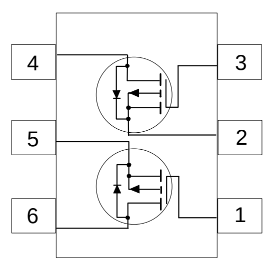
Applications

- Load switch
- Battery protection
- Power management

Features

- -1.7 A, -18 V. $R_{DS(ON)}$ = 0.18 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.30 Ω @ V_{GS} = -2.5 V
- Extended V_{GSS} range (±12V) for battery applications.
- Low gate charge (3nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current - Continuous	(Note 1a)	-1.7	A
	- Pulsed		-5	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.308	FDC6308P	7''	8mm	3000 units

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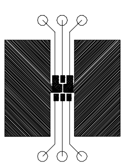
Electrical Characteristics
T_A = 25°C unless otherwise noted

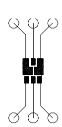
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C		-15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.6	-1.1	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C		2.7		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -1.7 A V_{GS} = -4.5 V, I_D = -1.7 A @125°C V_{GS} = -2.5 V, I_D = -1.4 A		0.143 0.22 0.25	0.18 0.28 0.30	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2.5			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.7 A		4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V f = 1.0 MHz		265		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -1 A V_{GS} = -4.5 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Turn-On Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
t_f	Turn-Off Fall Time			3	9	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -1.7 A V_{GS} = -4.5 V		3	5	nC
Q_{gs}	Gate-Source Charge			0.7		nC
Q_{gd}	Gate-Drain Charge			0.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.8 A (Note 2)		-0.8	-1.2	V

Notes:

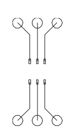
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 in² pad of 2 oz. copper.



c) 180 °C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Typical Characteristics

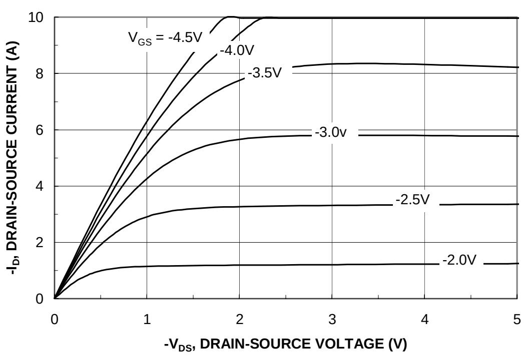


Figure 1. On-Region Characteristics.

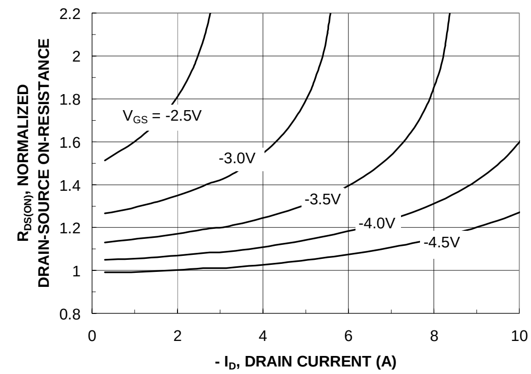


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

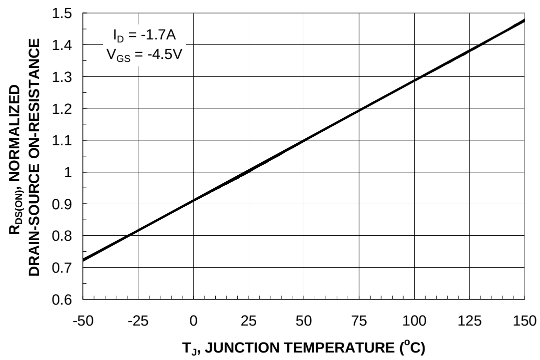


Figure 3. On-Resistance Variation with Temperature.

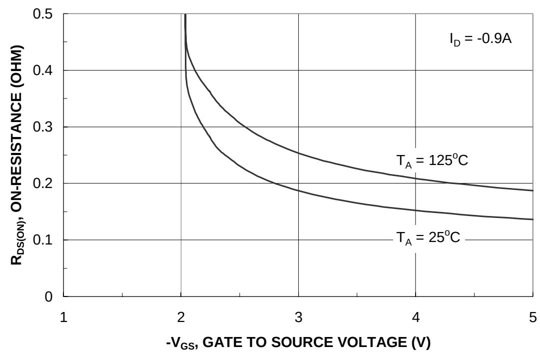


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

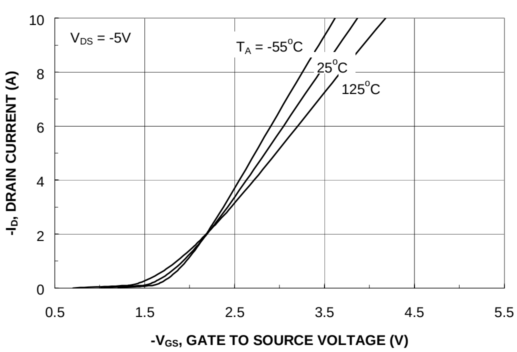


Figure 5. Transfer Characteristics.

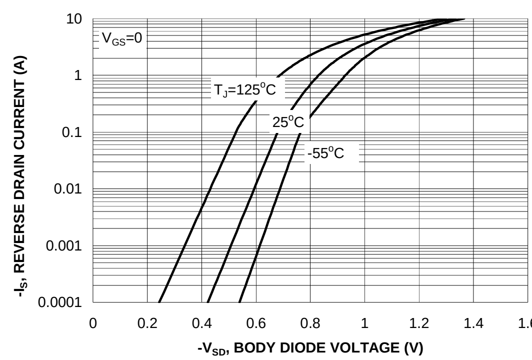


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

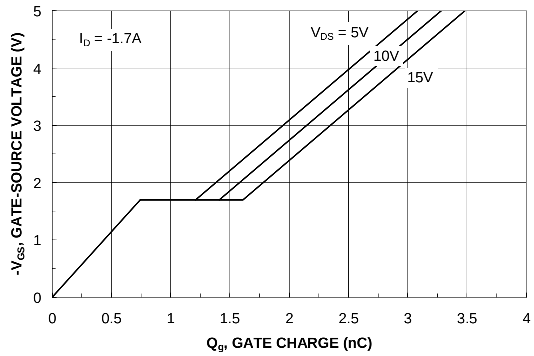


Figure 7. Gate-Charge Characteristics.

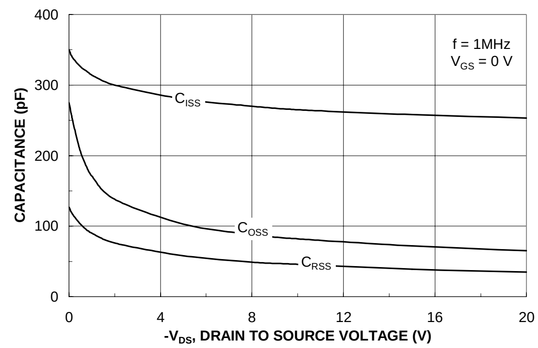


Figure 8. Capacitance Characteristics.

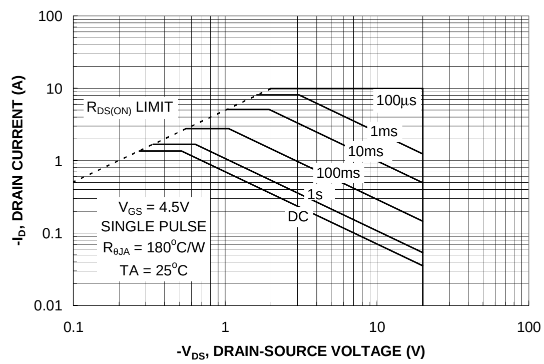


Figure 9. Maximum Safe Operating Area.

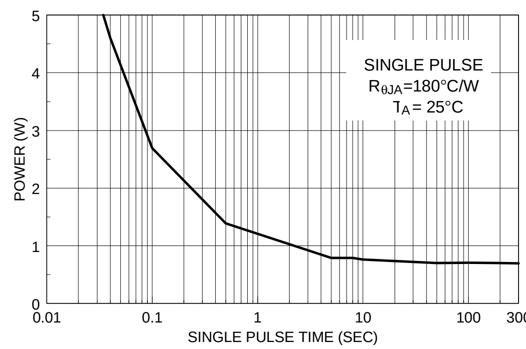


Figure 10. Single Pulse Maximum Power Dissipation.

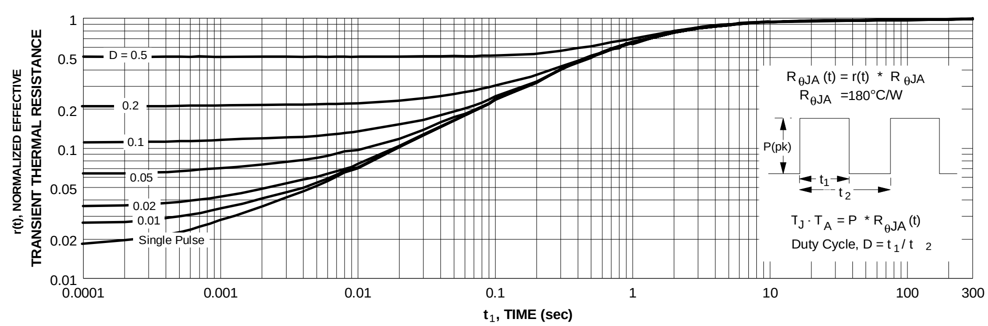


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient themal response will change depending on the circuit board design.

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