To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC108

Dual J-K Flip-Flops (with Preset, Common Clear and Common Clock)

ADE-205-433 (Z)
1st. Edition
Sep. 2000

Description

This flip-flop is edge sensitive to the clock input and change state on the negative transition of the clock pulse. Each flip-flop has independent J, K, and preset inputs and Q and $\overline{Q}$ outputs. Two flip-flops are controlled by a common clear and a common clock. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

Features

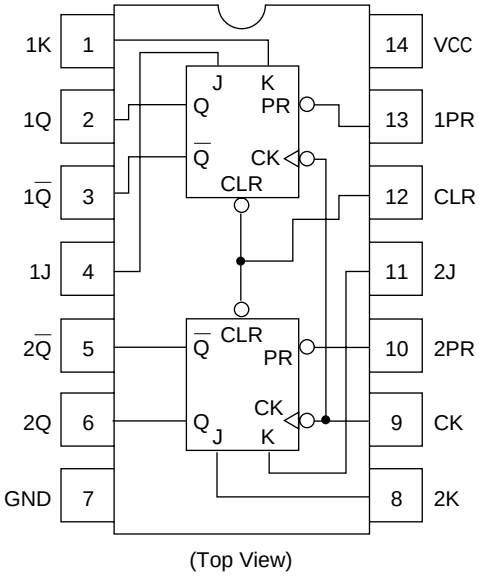
- High Speed Operation: t_{pd} (Clock to Q) = 20 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μA max (Ta = 25°C)

Function Table

Inputs					Output	
Preset	**Clear**	**Clock**	**J**	**K**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*[1]	H*[1]
H	H	↓	L	L	No change	
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	No change	
H	H	H	X	X	No change	
H	H	↑	X	X	No change	

Note: 1. Q and $\overline{Q}$ will remain HIGH as long as preset and Clear are Low, but Q and $\overline{Q}$ are unpredictable, if Preset and Clear go HIGH simultaneously.

Pin Arrangement



(Top View)

DC Characteristics

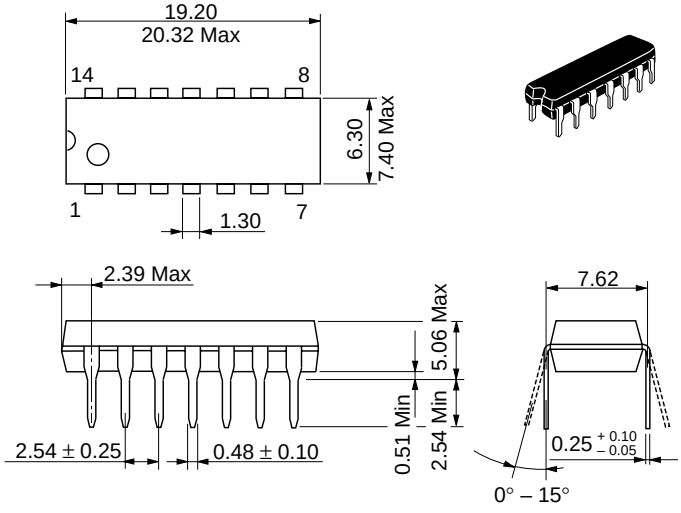
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	2.0	—	20	µA	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	150	—	190	ns	Clock to Q or $\overline{Q}$
		4.5	—	20	30	—	38		
		6.0	—	—	26	—	33		
		2.0	—	—	140	—	175	ns	Clear to Q or $\overline{Q}$
		4.5	—	18	28	—	35		
		6.0	—	—	24	—	30		
		2.0	—	—	140	—	175	ns	Preset to Q or $\overline{Q}$
		4.5	—	16	28	—	35		
		6.0	—	—	24	—	30		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	2	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	–1	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	–2	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

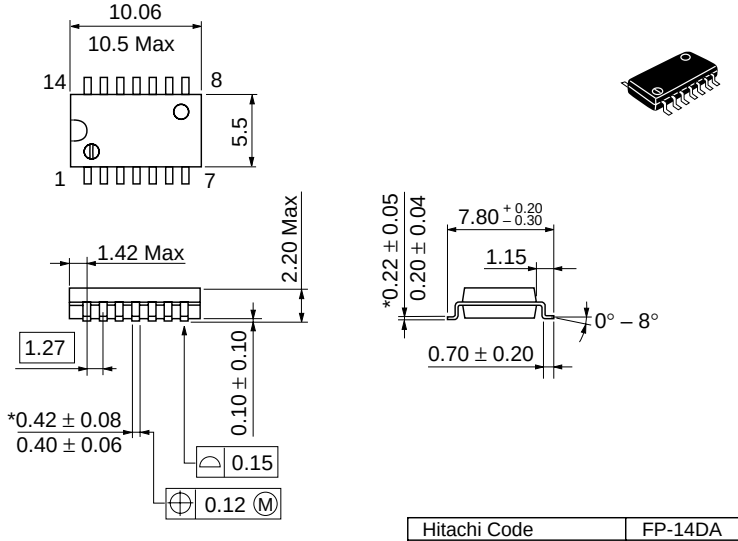
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

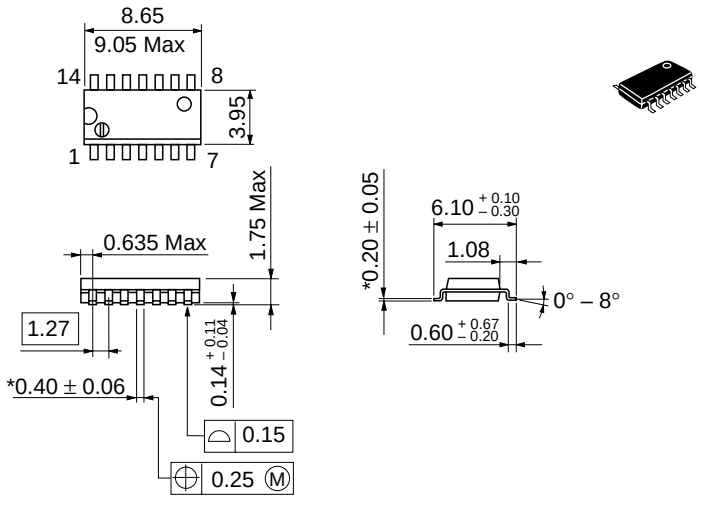
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

*Pd plating

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