Ordering number : ENN7938

SANYO Semiconductors
DATA SHEET

LC875270B
LC875262B
LC875246B

CMOS IC
ROM 72K/64K/48K-byte, RAM 2K-byte on-chip
8-bit 1-chip Microcontroller

Overview

The LC87F5270B/LC875262B/LC875246B is 8-bit single chip microcontroller with the following one-chip features :

- CPU : Operable at a minimum bus cycle time of 100ns
- On-chip ROM Capacity : LC875270B 72K-bytes
  : LC875262B 64K-bytes
  : LC875246B 48K-bytes
- On-chip RAM Capacity : 2K-bytes
- Two high performance 16-bit timer/counters (can be divided into 8-bit timers)
- Four 8-bit timers with prescalers
- Timer for use as date/time clock
- Two synchronous serial I/O ports (with automatic block transmit/receive function)
- One asynchronous/synchronous serial I/O port
- 12-bit PWM × 2
- 12-channel × 8-bit AD converter
- High speed 8-bit parallel interface
- High speed clock counter
- System clock divider
- 21-source 10-vectored interrupt system

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Features

■Read Only Memory (ROM)
- 73728 × 8-bits (LC875270B)
- 65536 × 8-bits (LC875262B)
- 49152 × 8-bits (LC875246B)

■Random Access Memory (RAM) : 2048 × 9-bit

■ Minimum Bus Cycle Time
- 100ns (10MHz)

  Note : Bus cycle time indicates the speed to read ROM.

■Minimum Instruction Cycle Time
- 300ns (10MHz)

■Ports
- Input/output ports

Input/output programmable for each bit individually	61 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn)
Data direction programmable in two bits	16 (PEn, PFn)
Data direction programmable in nibble units	8 (P0n)
• Input ports	2 (XT1, XT2)
• PWM output ports	2 (PWM0, PWM1)
• Oscillator pins	2 ($\overline{CF1}$, CF2)
• Reset pin	1 ($\overline{RES}$)
• Power supply	8 (V_{SS}1 to 4, V_{DD}1 to 4)

■Timer
- Timer 0 : 16-bit timer/counter with capture register
  - Mode 0 : Two 8-bit timers with programmable 8-bit prescaler and 8-bit capture register
  - Mode 1 : 8-bit timer with 8-bit programmable prescaler and 8-bit capture register + 8-bit counter with 8-bit capture register
  - Mode 2 : 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  - Mode 3 : 16-bit counter with 16-bit capture register
- Timer 1 : PWM/16-bit timer/counter with toggle output
  - Mode 0 : 8-bit timer (with toggle output) + 8-bit timer/counter (with toggle output)
  - Mode 1 : Two 8-bit PWM
  - Mode 2 : 16-bit timer/counter (with toggle output) Toggle output is also possible by using the lower order 8-bits.
  - Mode 3 : 16-bit timer (with toggle output) The lower order 8-bits can be used as PWM output.
- Timer 4 : 8-bit timer with 6-bit prescaler
- Timer 5 : 8-bit timer with 6-bit prescaler
- Timer 6 : 8-bit timer with 6-bit prescaler
- Timer 7 : 8-bit timer with 6-bit prescaler
- Base timer
  1. Clock for the base timer is selectable from sub-clock (32.768kHz crystal oscillation), system clock or programmable prescaler output of timer 0.
  2. There can be five separate interrupt sources.

■High speed clock counter
1. Maximum of 20MHz possible (when using a 10MHz main clock).
2. Real-time output

■Serial interface
- SIO 0 : 8-bit synchronous serial interface
  1. LSB first/MSB first-function available
  2. An internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3. Consecutive automatic data communication (1 to 256-bits)
- SIO 1 : 8-bit asynchronous/synchronous serial interface
  Mode 0 : Synchronous 8-bit serial I_O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1 : Asynchronous serial I_O (half duplex, 8 data bits, 1 stop bit, baud-rate 8 to 2048 tCYC)
  Mode 2 : Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3 : Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO2 : 8-bit synchronous serial interface
  1. LSB-first
  2. Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3. Consecutive automatic data communication (1 to 32-bytes)

■AD converter
- 12-channel % 8-bit AD converter

■PWM
- 2 channel % synchronous variable 12-bit PWM

■Parallel interface
- RS, $\overline{RD}$, $\overline{WR}$, $\overline{CS0}$ to $\overline{CS2}$ outputs (polarity can be toggled)
- Read/write possible in 1 tCYC

■Remote receiver circuit (share with P73/INT3/T0IN terminal)
- Noise rejection function (The filtering time of the noise rejection filter (1tCYC/32 tCYC/128 tCYC) can be switched by program.)

■Watchdog timer
- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

■Interrupts
- 21-source and 10-vectored interrupt function :
  1. Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting possible. During interrupt handling, an equal or lower level interrupt request is refused.
  2. If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1/SIO2
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

• Priority Level : X > H > L
• For equal priority levels, vector with lowest address takes precedence.

■Subroutine stack levels
- A maximum of 1024 levels (set stack inside RAM)

■Multiplication and division
- 16-bits × 8-bits (5 instruction-cycle times)
- 24-bits × 16-bits (12 instruction-cycle times)
- 16-bits ÷ 8-bits (8 instruction-cycle times)
- 24-bits ÷ 16-bits (12 instruction-cycle times)

■Oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Crystal oscillation circuit used for the system clock

■System clock divider
- Operable on the lowest power consumption
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

■Standby function
- HALT mode

  The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.
- HOLD mode

  The HOLD mode stops program execution and all oscillation circuits : CF, RC and Crystal oscillations.
  This mode can be released by the following conditions.
  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$)
  2. Supply the selected level to at lease one of INT0, INT1, INT2, INT4 INT5.
  3. Supply an interrupt condition to Port 0.
- X'tal HOLD mode

  The X'tal HOLD mode stops program execution and all peripheral circuits except for the base timer.
  The crystal oscillator maintains its state at HOLD mode inception.
  This mode can be released by the following conditions.
  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$).
  2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5
  3. Supply an interrupt condition to Port 0.
  4. Supply an interrupt condition to the base timer circuit.

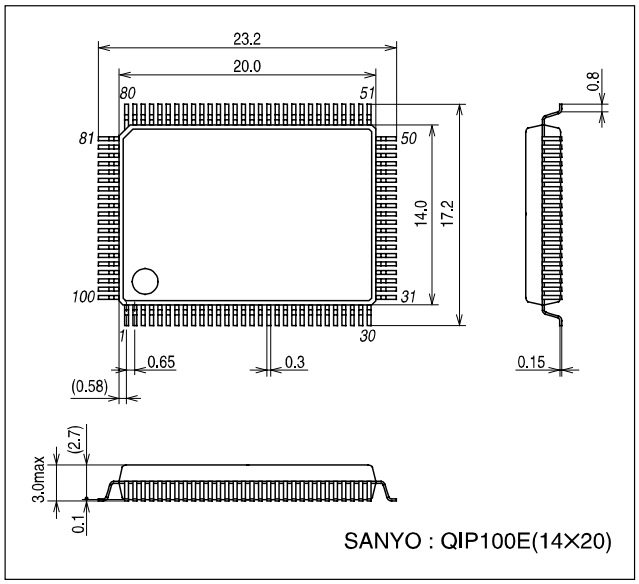
■Shipping form
- QIP100E
- SQFP100
- TQFP100

■Development tools
- Evaluation (EVA) chip : LC876093
- Emulator : EVA62S + ECB876600A + SUB875200 + POD100QFP or POD100SQFP2
- Flash ROM version : LC87F52C8A

Package Dimensions

unit : mm

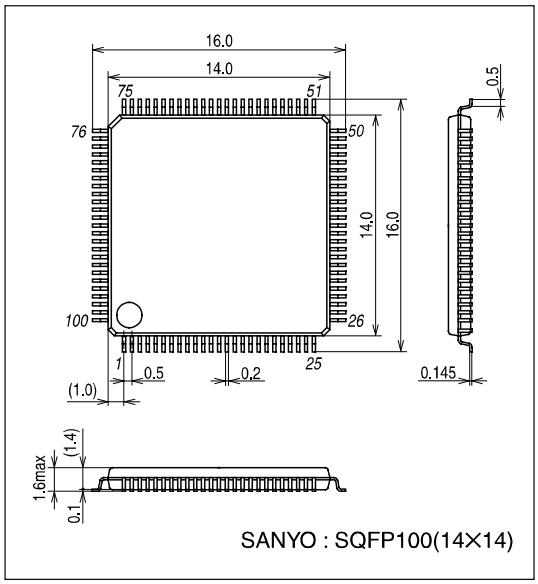
3151A



Package Dimensions

unit : mm

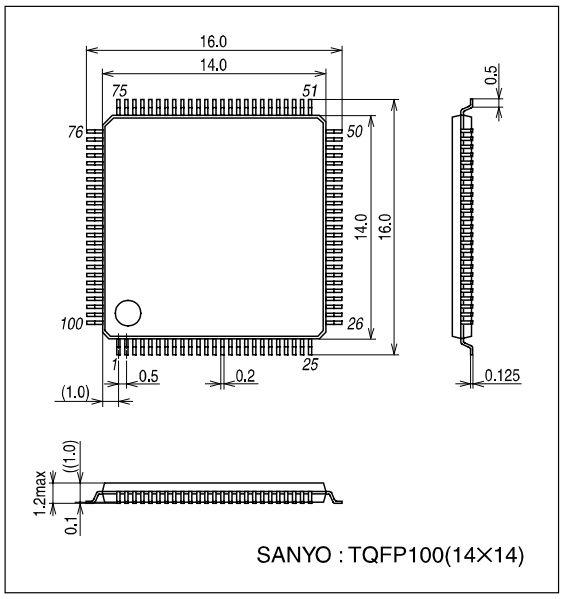
3181C



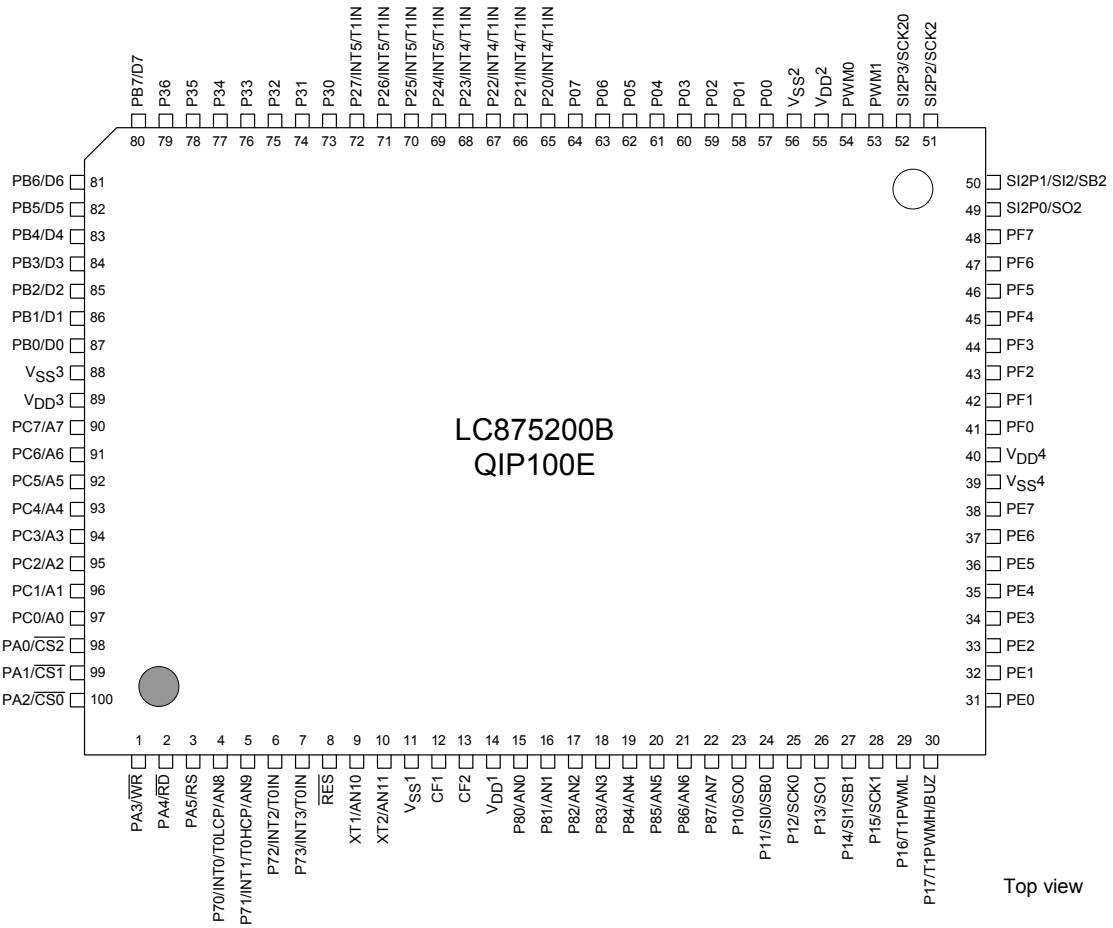
Package Dimensions

unit : mm

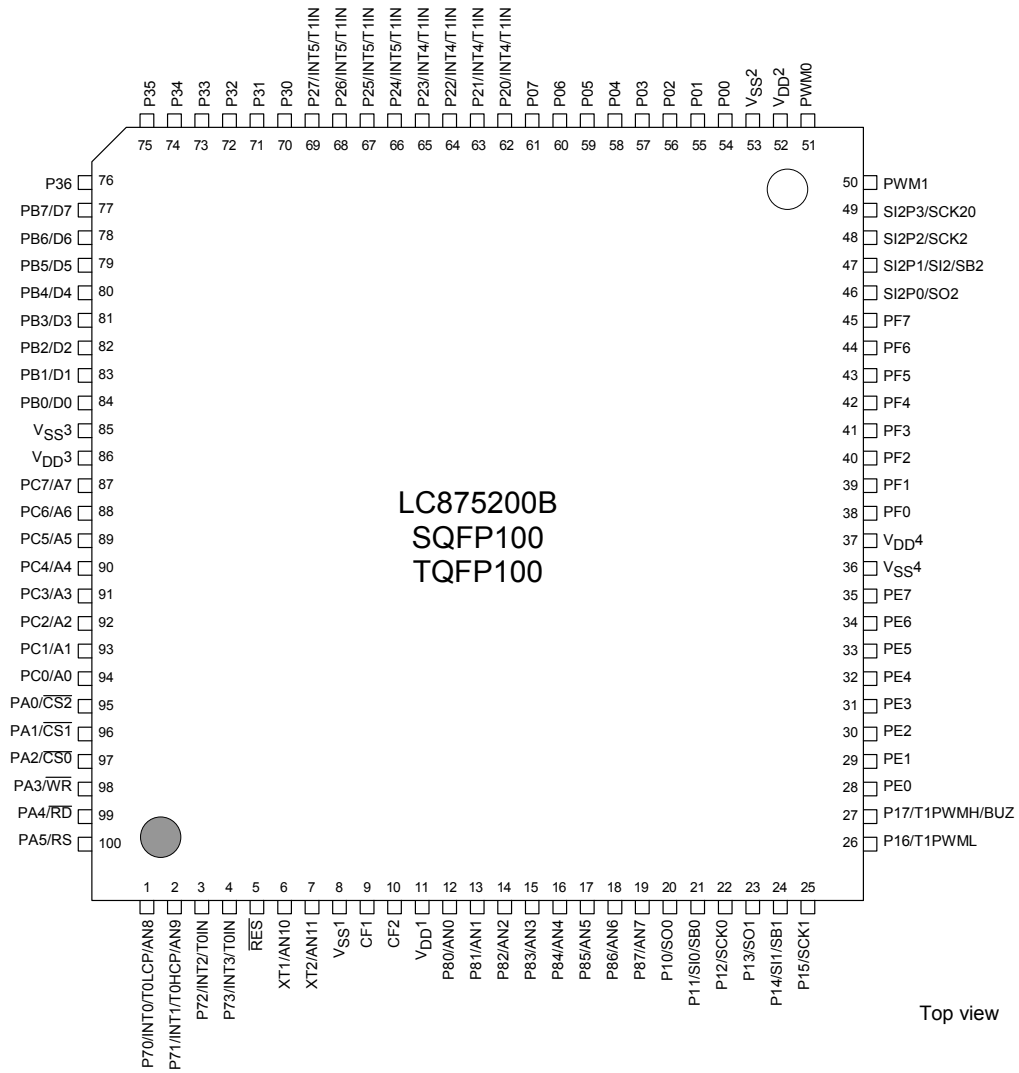
3274



Pin Assignment



Top view

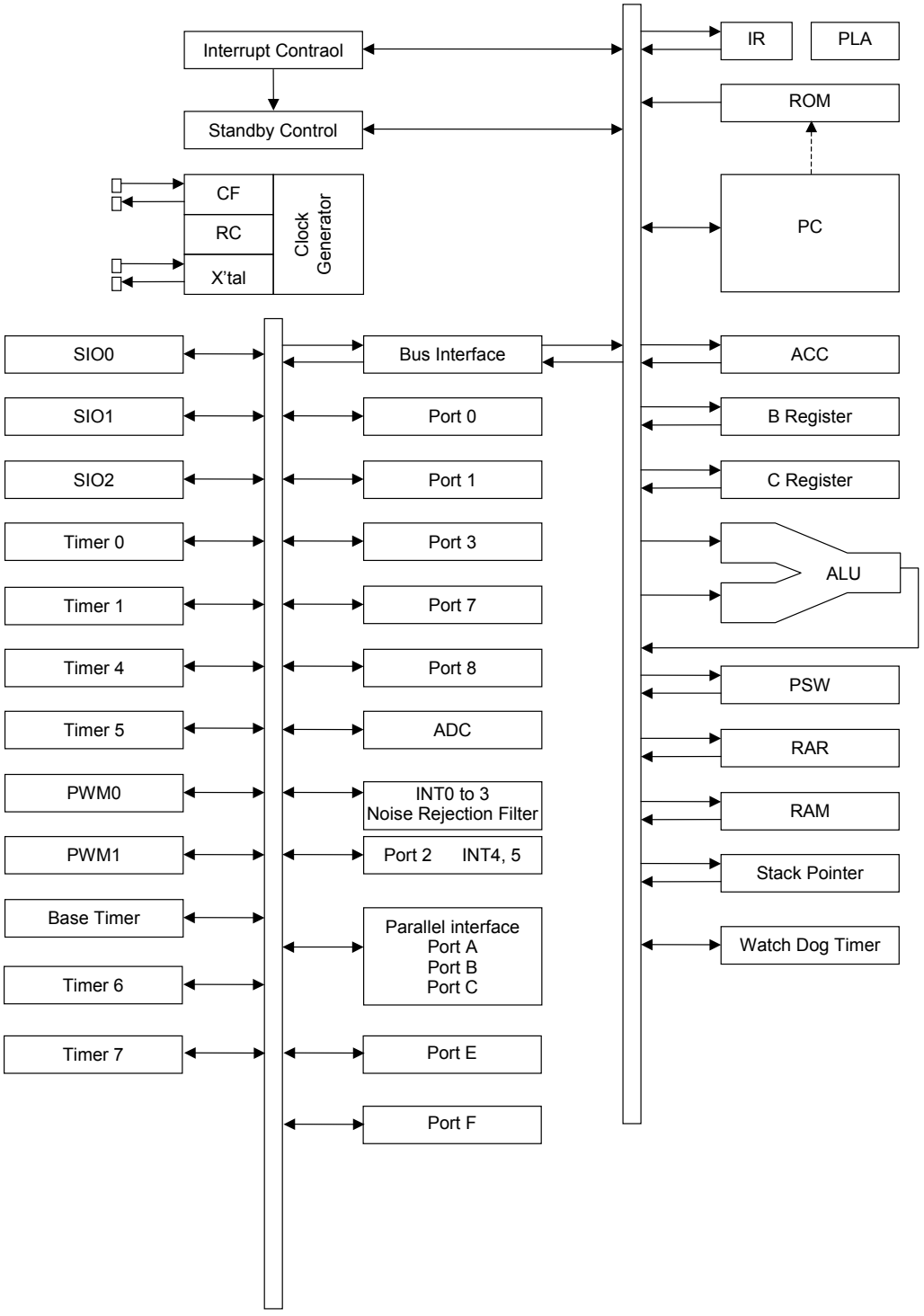

LC875200B
SQFP100
TQFP100
Top view
1 P70/INT0/T0LCP/AN8
2 P71/INT1/T0HCP/AN9
3 P72/INT2/T0IN
4 P73/INT3/T0IN
5 RES
6 XT1/AN10
7 XT2/AN11
8 VSS1
9 CF1
10 CF2
11 VDD1
12 P80/AN0
13 P81/AN1
14 P82/AN2
15 P83/AN3
16 P84/AN4
17 P85/AN5
18 P86/AN6
19 P87/AN7
20 P10/SO0
21 P11/SI0/SB0
22 P12/SCK0
23 P13/SO1
24 P14/SI1/SB1
25 P15/SCK1
26 P16/T1PWML
27 P17/T1PWMH/BUZ
28 PE0
29 PE1
30 PE2
31 PE3
32 PE4
33 PE5
34 PE6
35 PE7
36 VSS4
37 VDD4
38 PF0
39 PF1
40 PF2
41 PF3
42 PF4
43 PF5
44 PF6
45 PF7
46 SI2P0/SO2
47 SI2P1/SI2/SB2
48 SI2P2/SCK2
49 SI2P3/SCK20
50 PWM1
51 PWM0
52 VDD2
53 VSS2
54 P00
55 P01
56 P02
57 P03
58 P04
59 P05
60 P06
61 P07
62 P20/INT4/T1IN
63 P21/INT4/T1IN
64 P22/INT4/T1IN
65 P23/INT4/T1IN
66 P24/INT5/T1IN
67 P25/INT5/T1IN
68 P26/INT5/T1IN
69 P27/INT5/T1IN
70 P30
71 P31
72 P32
73 P33
74 P34
75 P35
76 P36
77 PB7/D7
78 PB6/D6
79 PB5/D5
80 PB4/D4
81 PB3/D3
82 PB2/D2
83 PB1/D1
84 PB0/D0
85 VSS3
86 VDD3
87 PC7/A7
88 PC6/A6
89 PC5/A5
90 PC4/A4
91 PC3/A3
92 PC2/A2
93 PC1/A1
94 PC0/A0
95 PA0/CS2
96 PA1/CS1
97 PA2/CS0
98 PA3/WR
99 PA4/RD
100 PA5/RS

PAD Coordinate Values

QIP	NAME	SQFP/TQFP
1	PA3/$\overline{WR}$	98
2	PA4/$\overline{RD}$	99
3	PA5/RS	100
4	P70/INT0/T0LCP/AN8	1
5	P71/INT1/T0HCP/AN9	2
6	P72/INT2/T0IN	3
7	P73/INT3/T0IN	4
8	$\overline{RES}$	5
9	XT1/AN10	6
10	XT2/AN11	7
11	$V_{SS}1$	8
12	CF1	9
13	CF2	10
14	$V_{DD}1$	11
15	P80/AN0	12
16	P81/AN1	13
17	P82/AN2	14
18	P83/AN3	15
19	P84/AN4	16
20	P85/AN5	17
21	P86/AN6	18
22	P87/AN7	19
23	P10/SO0	20
24	P11/SI0/SB0	21
25	P12/SCK0	22
26	P13/SO1	23
27	P14/SI1/SB1	24
28	P15/SCK1	25
29	P16/T1PWML	26
30	P17/T1PWMH/BUZ	27
31	PE0	28
32	PE1	29
33	PE2	30
34	PE3	31
35	PE4	32
36	PE5	33
37	PE6	34
38	PE7	35
39	$V_{SS}4$	36
40	$V_{DD}4$	37
41	PF0	38
42	PF1	39
43	PF2	40
44	PF3	41
45	PF4	42
46	PF5	43
47	PF6	44
48	PF7	45
49	SI2P0/SO2	46
50	SI2P1/SI2/SB2	47

QIP	NAME	SQFP/TQFP
51	SI2P2/SCK2	48
52	SI2P3/SCK20	49
53	PWM1	50
54	PWM0	51
55	$V_{DD}2$	52
56	$V_{SS}2$	53
57	P00	54
58	P01	55
59	P02	56
60	P03	57
61	P04	58
62	P05	59
63	P06	60
64	P07	61
65	P20/INT4/T1IN	62
66	P21/INT4/T1IN	63
67	P22/INT4/T1IN	64
68	P23/INT4/T1IN	65
69	P24/INT5/T1IN	66
70	P25/INT5/T1IN	67
71	P26/INT5/T1IN	68
72	P27/INT5/T1IN	69
73	P30	70
74	P31	71
75	P32	72
76	P33	73
77	P34	74
78	P35	75
79	P36	76
80	PB7/D7	77
81	PB6/D6	78
82	PB5/D5	79
83	PB4/D4	80
84	PB3/D3	81
85	PB2/D2	82
86	PB1/D1	83
87	PB0/D0	84
88	$V_{SS}3$	85
89	$V_{DD}3$	86
90	PC7/A7	87
91	PC6/A6	88
92	PC5/A5	89
93	PC4/A4	90
94	PC3/A3	91
95	PC2/A2	92
96	PC1/A1	93
97	PC0/A0	94
98	PA0/$\overline{CS2}$	95
99	PA1/$\overline{CS1}$	96
100	PA2/$\overline{CS0}$	97

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$
$V_{SS}3$, $V_{SS}4$</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$
$V_{DD}3$, $V_{DD}4$</td><td>-</td><td>Power terminal (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Pull-up resistor provided/not provided (specified in nibble units)
• HOLD release input
• Port 0 interrupt input</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P10 : SIO0 data output
P11 : SIO0 data input, bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input, bus input/output
P15 : SIO1 clock input/output
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P20 to P23 : INT4 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input
P24 to P27 : INT5 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input

• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P36</td><td>I/O</td><td>• 7-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)</td><td>Yes</td></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P70 : INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71 : INT1 input/HOLD release input/Timer 0H capture input
P72 : INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input
P73 : INT3 input with noise filter/Timer 0 event input/Timer 0H capture input

• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>• AD converter input port : AN8 (P70), AN9 (P71)</td><td>No</td></tr>
</table>

Continued on next page.

Continued from preceding page.

Pin name	I/O	Function	Option
Port 8 P80 to P87	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Other functions P80 to P87 : AD converter input port	No
Port A PA0 to PA5	I/O	• 6-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PA0 : Parallel interface output $\overline{CS2}$ PA1 : Parallel interface output $\overline{CS1}$ PA2 : Parallel interface output $\overline{CS0}$ PA3 : Parallel interface output $\overline{WR}$ PA4 : Parallel interface output $\overline{RD}$ PA5 : Parallel interface output RS	Yes
Port B PB0 to PB7	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PB0 to PB7 : Parallel interface data input/output, address output	Yes
Port C PC0 to PC7	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PC0 to PC7 : Parallel interface address output	Yes
Port E PE0 to PE7	I/O	• 8-bit input/output port • Data direction programmable in two bits • Pull-up resistor provided/not provided (specified by bit)	No
Port F PF0 to PF7	I/O	• 8-bit input/output port • Data direction programmable in two bits Pull-up resistor provided/not provided (specified by bit)	No
SIO2 Port SI2P0 to SI2P3	I/O	• 4-bit input/output port • Data direction programmable for each bit individually • Other functions SI2P0 : SIO2 data output SI2P1 : SIO2 data input, bus input/output SI2P2 : SIO2 clock input/output SI2P3 : SIO2 clock output	No
PWM0	O	PWM0 output port	No
PWM1	O	PWM1 output port	No
$\overline{RES}$	I	Reset terminal	No
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Other function AN10 : AD converter input port General input port When not in use, connect terminal to $V_{DD}1$.	No
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other function AN11 : AD converter input port General input port When not in use, set as oscillation and leave terminal open	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

Port Output Configuration

Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

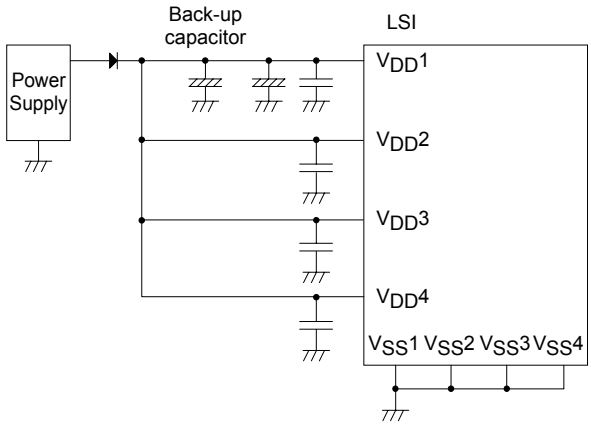
Terminal	Option applies to :	Option	Output Format	Pull-up resistor
P00 to P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17 P20 to P27 P30 to P36	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PA0 to PA5 PB0 to PB7(*) PC0 to PC7	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PE0 to PE7 PF0 to PF7(*)	-	None	CMOS	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
P80 to P87	-	None	Nch-open drain	None
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	None	CMOS	None
SI2P1	-	None	CMOS (When used as general port) Nch-open drain (When used for SIO2 data)	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 : Programmable pull-up resistor of Port 0 is specified in nibble units (P00 to P03, P04 to P07).

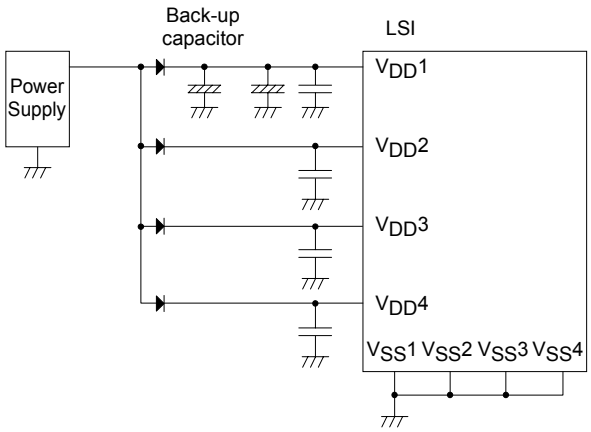
(*) When in parallel interface mode, PB0 to PB7 output format is CMOS, regardless of any selected option.

Note : To reduce V_{DD} signal noise and to increase the duration of the backup battery supply, $V_{SS}1$, $V_{SS}2$, $V_{SS}3$ and $V_{SS}4$ should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output "H" level is supplied from the back-up capacitor.



Example 2 : During backup in hold mode, output is not held high and its value in unsettled.



Absolute Maximum Ratings / Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter		Symbol	Pins	Conditions	Limits				
					V_{DD}[V]	min	typ	max	unit
Supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$	$V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$		-0.3		+7.0	V
Input voltage		V_I(1)	XT1, XT2, CF1			-0.3		V_{DD}+0.3	V
Output voltage		V_O(1)	PWM0, PWM1			-0.3		V_{DD}+0.3	V
Input/Output voltage		V_{IO}(1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1			-0.3		V_{DD}+0.3	V
High level output current	Peak output current	IOPH(1)	• Ports 0, 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH(2)	P71 to P73	For each pin.		-5			mA
	Total output current	ΣIOAH(1)	P71 to P73	Total of all pins		-5			mA
		ΣIOAH(2)	• Port 1 • PWM0, PWM1 • Port 3 • SI2P00 to SI2P03	Total of all pins		-30			mA
		ΣIOAH(3)	Ports 0, 2	Total of all pins		-20			mA
		ΣIOAH(4)	Port B	Total of all pins		-20			mA
		ΣIOAH(5)	Ports A, C	Total of all pins		-20			mA
Low level output current	Peak output current	IOPL(1)	• P02 to P07 • Ports 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	For each pin.				20	mA
		IOPL(2)	P00, P01	For each pin.				30	mA
		IOPL(3)	Ports 7, 8	For each pin.				5	mA
	Total output current	ΣIOAL(1)	Port 7	Total of all pins				15	mA
		ΣIOAL(2)	Port 8	Total of all pins				15	mA
		ΣIOAL(3)	• Port 1 • PWM0, PWM1 • Port 3 • SI2P00 to SI2P03	Total of all pins				50	mA
		ΣIOAL(4)	Ports 0, 2	Total of all pins				70	mA
		ΣIOAL(5)	Port B	Total of all pins				40	mA
		ΣIOAL(6)	Ports A, C	Total of all pins				40	mA
		ΣIOAL(7)	Port E	Total of all pins				40	mA
		ΣIOAL(8)	Port F	Total of all pins				40	mA
Maximum power consumption		Pd max	QIP100E	Ta = -30 to +70°C				523	mW
			SQFP100					416	mW
			TQFP100					398	mW
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	°C

Recommended Operating Range / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Operating supply voltage range	$V_{DD}(1)$	$V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$	0.294µs≤tCYC≤200µs		4.5		6.0	V
			0.588µs≤tCYC≤200µs		2.5		6.0	
HOLD voltage	VHD	$V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$	RAM and register data are kept in HOLD mode.		2.0		6.0	
Input high voltage	$V_{IH}(1)$	• Ports 1, 2 • SI2P00 to 03 • P71 to P73 • P70 port input /interrupt		2.5 to 6.0	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	• Ports 0, 8, 3 • Ports A, B, C, E, F		2.5 to 6.0	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 70 Watchdog timer		2.5 to 6.0	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 6.0	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}(1)$	• Ports 1, 2 • SI2P00 to 03 • P71 to P73 • P70 port input/interrupt		2.5 to 6.0	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$	• Ports 0, 8, 3 • Ports A, B, C, E, F		2.5 to 6.0	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(5)$	Port 70 Watchdog timer		2.5 to 6.0	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(6)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 6.0	V_{SS}		$0.25V_{DD}$	
Operation cycle time	tCYC			4.5 to 6.0	0.294		200	µs
				2.5 to 6.0	0.588		200	
External system clock frequency	FEXCF(1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = 50±5%	4.5 to 6.0	0.1		10	MHz
			• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = 50±5%	2.5 to 6.0	0.1		5	
			• Leave CF2 pin open • System clock divider set to 1/2	4.5 to 6.0	0.2		20.4	
			• Leave CF2 pin open • System clock divider set to 1/2	2.5 to 6.0	0.1		10	
Oscillation frequency range	FmCF(1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5 to 6.0		10		
	FmCF(2)	CF1, CF2	5MHz ceramic resonator oscillation Refer to figure 1	2.5 to 6.0		5		
	FmRC		RC oscillation	2.5 to 6.0	0.3		2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 6.0		32.768		kHz

Note 1 : The oscillation parameters are shown on Tables 1 and 2.

Electrical Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Input high current	$I_{IH}(1)$	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00 to SI2P03 • $\overline{RES}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN} = V_{DD}$ (Including the off-leak current of the output Tr.)	2.5 to 6.0			1	μA
	$I_{IH}(2)$	XT1, XT2	• Using as an input port • $V_{IN} = V_{DD}$	2.5 to 6.0			1	
	$I_{IH}(3)$	CF1	$V_{IN} = V_{DD}$	2.5 to 6.0			15	
Input low current	$I_{IL}(1)$	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C, E, F • SI2P00 to SI2P03 • $\overline{RES}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN} = V_{SS}$ (Including the off-leak current of the output Tr.)	2.5 to 6.0	-1			
	$I_{IL}(2)$	XT1, XT2	• Using as an input port • $V_{IN} = V_{SS}$	2.5 to 6.0	-1			
	$I_{IL}(3)$	CF1	$V_{IN} = V_{SS}$	2.5 to 6.0	-15			
Output high voltage	$V_{OH}(1)$	• Ports 0, 1, 2, 3 • Ports B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	I_{OH} = -1.0mA	4.5 to 6.0	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH} = -0.1mA	2.5 to 6.0	V_{DD}-0.5			
	$V_{OH}(3)$	Port A	I_{OH} = -5.0mA	4.5 to 6.0	V_{DD}-1			
	$V_{OH}(4)$		I_{OH} = -0.4mA	2.5 to 6.0	V_{DD}-0.5			
	$V_{OH}(5)$	Ports 71, 72, 73	I_{OH} = -0.4mA	4.5 to 6.0	V_{DD}-1			
Output low voltage	$V_{OL}(1)$	• Ports 0, 1, 2, 3 • Ports B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	I_{OL} = 10mA	4.5 to 6.0			1.5	
	$V_{OL}(2)$		I_{OL} = 1.6mA	4.5 to 6.0			0.4	
	$V_{OL}(3)$		I_{OL} = 1mA	2.5 to 6.0			0.4	
	$V_{OL}(4)$	P00, P01	I_{OL} = 30mA	4.5 to 6.0			1.5	
	$V_{OL}(5)$	Ports 7, 8	I_{OL} = 1mA	2.5 to 6.0			0.4	
	$V_{OL}(6)$							
	$V_{OL}(7)$	Port A	I_{OL} = 15mA	4.5 to 6.0			1.5	
	$V_{OL}(8)$		I_{OL} = 2mA	2.5 to 6.0			0.4	
Pull-up resistor	Rpu	• Ports 0, 1, 2, 3 • Port 7 • Ports A, B, C, E, F	$V_{OH} = 0.9V_{DD}$	2.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{RES}$ • Port 1 • Port 2 • Port 7 • SIP00 to SIP03		2.5 to 6.0		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : $V_{IN} = V_{SS}$ • f = 1MHz • Ta = 25°C	2.5 to 6.0		10		pF

Serial Input/Output Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter			Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0 (P12), SI2P2	Refer to figure 6	2.5 to 6.0	2			tCYC
		Low level pulse width	tSCKL(1)				1			
			tSCKLA(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)				4(SIO0) 5(SIO2)			
		Cycle	tSCK(2)	SCK1 (P15)	Refer to figure 6	2.5 to 6.0	2			
		Low level pulse width	tSCKL(2)				1			
		High level pulse width	tSCKH(2)				1			
	Output clock	Cycle	tSCK(3)	SCK0 (P12), SI2P2 SI2P3	• CMOS output • Refer to figure 6	2.5 to 6.0	4/3			
		Low level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)		SCK0 (P12) SIO0			3/4		
					SI2P2, SI2P3 SIO2			1		
		High level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)		SCK0 (P12) SIO0			2		
					SI2P2, SI2P3 SIO2			7/4		
		Cycle	tSCK(4)	SCK1 (P15)	• CMOS output • Refer to figure 6	2.5 to 6.0	2			tCYC
		Low level pulse width	tSCKL(4)					1/2		tSCK
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SB0 (P11), SB1 (P14), SI2P1 SI0 SI1	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 6	2.5 to 6.0	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdD0	SO0 (P10), SO1 (P13), SB0 (O11), SB1 (P14), SI2P0, SI2P1	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.5 to 6.0			1/3tCYC +0.05	

Parallel Input/Output Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Note : If Port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.
Refer to figures 8 and 9 for parallel output timing.

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Write cycle, Read cycle	tC(1)			2.5 to 6.0		1		tCYC
Address set-up time	tsA(1)	• $\overline{WR}$ (PA3), PB0 to PB7 • $\overline{RD}$ (PA4), PC0 to PC7	From address set-up until control signal changes	2.5 to 6.0	1/3tCYC -30ns			tCYC & ns
	tsA(2)	$\overline{RD}$ (PA4), PC0 to PC7		2.5 to 6.0	2/3tCYC -30ns			
Address hold time	thA(1)	$\overline{RD}$ (PA4), PC0 to PC7	From change of $\overline{RD}$ until address change	2.5 to 6.0	1/6tCYC			
	thA(2)	$\overline{WR}$ (PA3), PC0 to PC7	From change of $\overline{WR}$ until address change	2.5 to 6.0	5			ns

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
RS set-up time	tsRS(1)	$\overline{WR}$ (PA3), RS (PA5), $\overline{CS}$ (PAX)	From change of RS, $\overline{CS}$ until change in $\overline{WR}$	2.5 to 6.0	1/6tCYC -15ns			tCYC & ns
	tsRS(2)	$\overline{RD}$ (PA4), RS (PA5)	From change of RS until change in $\overline{RD}$	2.5 to 6.0	1/6tCYC -15ns			
	tsRS(3)	$\overline{RD}$ (PA4), RS (PA5)		2.5 to 6.0	1/3tCYC -15ns			
$\overline{CS}$ set-up time	tsCS(1)	$\overline{RD}$ (PA4), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{RD}$	2.5 to 6.0	1/3tCYC -15ns			
	tsCS(2)	$\overline{WR}$ (PA3), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{WR}$	2.5 to 6.0	2/3tCYC -15ns			
RS hold time	thRS(1)	$\overline{WR}$ (PA3), RS (PA5)	From change in $\overline{WR}$ until change in RS	2.5 to 6.0	0			ns
	thRS(2)	$\overline{RD}$ (PA4), RS (PA5), $\overline{CS}$ (PAX)	From change in $\overline{RD}$ until change in RS, $\overline{CS}$	2.5 to 6.0	1/6tCYC			tCYC & ns
	thRS(3)	$\overline{RD}$ (PA4), RS (PA5), $\overline{CS}$ (PAX)		2.5 to 6.0	0			ns
$\overline{CS}$ hold time	thCS(1)	$\overline{RD}$ (PA4), RS (PA5)	From change in $\overline{RD}$ until change in $\overline{CS}$	2.5 to 6.0	1/6tCYC			tCYC & ns
	thCS(2)	$\overline{WR}$ (PA3), RS (PA5)	From change in $\overline{WR}$ until change in $\overline{CS}$	2.5 to 6.0	0			ns
$\overline{WR}$ 'H' pulse width	tWRH(1)	$\overline{WR}$ (PA3)		2.5 to 6.0	1/6tCYC -5ns	1/6 tCYC		tCYC & ns
	tWRH(2)	$\overline{WR}$ (PA3)		2.5 to 6.0	2/3tCYC -5ns	2/3 tCYC		
$\overline{WR}$ 'L' pulse width	tWRL(1)	$\overline{WR}$ (PA3)		2.5 to 6.0	1/6tCYC -5ns	1/6 tCYC		
	tWRL(2)	$\overline{WR}$ (PA3)		2.5 to 6.0	1/3tCYC -5ns	1/3 tCYC		
$\overline{RD}$ 'H' pulse width	tRDH(1)	$\overline{RD}$ (PA4)		2.5 to 6.0	1/6tCYC -5ns	1/6 tCYC		
	tRDH(2)	$\overline{RD}$ (PA4)		2.5 to 6.0	1/3tCYC -5ns	1/3 tCYC		
$\overline{RD}$ 'L' pulse width	tRDL(1)	$\overline{RD}$ (PA4)		2.5 to 6.0	1/3tCYC -5ns	1/3 tCYC		
	tRDL(2)	$\overline{RD}$ (PA4)		2.5 to 6.0	1/2tCYC -5ns	1/2 tCYC		
Data write maximum delay	tdDT(1)	$\overline{RD}$ (PA4), PB0 to PB7	The time delay allowed, from $\overline{RD}$ leading edge until input data set-up (Note 1)	2.5 to 6.0			1/6tCYC -15ns	
	tdDT(2)	$\overline{RD}$ (PA4), PB0 to PB7		2.5 to 6.0			1/3tCYC -15ns	
Input data set-up time	tsDTR(1)	$\overline{RD}$ (PA4), PB0 to PB7	From input data set-up to $\overline{RD}$ leading edge. (Note 2)	2.5 to 6.0	40			ns
Input data hold time	thDTR(1)	$\overline{RD}$ (PA4), PB0 to PB7	From $\overline{RD}$ leading edge until input data hold	2.5 to 6.0	0			
Output data set-up time	tsDTW(1)	$\overline{RD}$ (PA4), PB0 to PB7	From output data set-up until $\overline{WR}$ leading edge	2.5 to 6.0	1/3tCYC -30ns			tCYC & ns
	tsDTW(2)	$\overline{RD}$ (PA4), PB0 to PB7		2.5 to 6.0	1/3tCYC -30ns			
Output data hold time	thDTW(1)	$\overline{RD}$ (PA4), PB0 to PB7	From $\overline{WR}$ leading edge until output data hold	2.5 to 6.0	0			ns
	thDTW(2)			2.5 to 6.0	0			

Note 1 : Time until incorrect data of low disappears.

Note 2 : Incorrect data of low is not output in the period between tRDL(1) to tdDT(1).

Pulse Input Conditions / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0 (P70), INT1 (P71), INT2 (P72) INT4 (P20 to P23) INT5 (P24 to P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3 (P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3 (P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 6.0	64			
	tPIH(4) tPIL(4)	INT3 (P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 6.0	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.5 to 6.0	200			µs

AD Converter Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0 (P80) to AN7 (P87) AN8 (P70) AN9 (P71) AN10 (XT1) AN11 (XT2)		3.0 to 6.0		8		bit
Absolute precision	ET		(Note 3)	3.0 to 6.0			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32 × tCYC (ADCR2 = 0) (Note 4)	3.0 to 6.0	15.10 (tCYC = 0.588µs)		97.92 (tCYC = 3.06µs)	µs
			AD conversion time = 64 × tCYC (ADCR2 = 1) (Note 4)	3.0 to 6.0	15.10 (tCYC = 0.294µs)		97.92 (tCYC = 1.53µs)	
Analog input voltage range	VAIN			3.0 to 6.0	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN = V_{DD}	3.0 to 6.0			1	µs
	IAINL		VAIN = V_{SS}	3.0 to 6.0	-1			

Note 3 : Absolute precision excludes the quantizing error (±1/2 LSB).

Note 4 : The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

Current Dissipation Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Current drain during basic operation (Note 5)	IDDOP(1)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$ = $V_{DD}4$	• FmCF = 10MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		9	20	mA
	IDDOP(2)		• CF1 = 20MHz by external clock • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • 1/2 divided	2.5 to 6.0		10	21	
	IDDOP(3)		• FmCF = 5MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		5	11	
	IDDOP(4)			2.5 to 4.5		3.5	8	
	IDDOP(5)		• FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : RC oscillation • 1/2 divided	4.5 to 6.0		0.7	5	
	IDDOP(6)			2.5 to 4.5		0.3	3	
	IDDOP(7)		• FmCF = 0Hz (when oscillation stops) • FmX'al = 32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		30	60	µA
	IDDOP(8)			2.5 to 4.5		11	50	
Current drain in HALT mode (Note 5)	IDDHALT(1)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$ = $V_{DD}4$	• HALT mode • FmCF = 10MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		4	10	mA
	IDDHALT(2)		• HALT mode • CF1 = 20MHz by external clock • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		5	10	
	IDDHALT(3)		• HALT mode • FmCF = 5MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		2	5	
	IDDHALT(4)			2.5 to 4.5		1	2.8	
	IDDHALT(5)		• HALT mode • FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : RC oscillation • 1/2 divided	4.5 to 6.0		0.5	2	
	IDDHALT(6)			2.5 to 4.5		0.2	1	
	IDDHALT(7)		• HALT mode • FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		18	50	µA
	IDDHALT(8)			2.5 to 4.5		7	40	
Current drain during HOLD mode	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1 = V_{DD} or leave it open (when using external clock)	4.5 to 6.0		0.01	15	
				2.5 to 4.5		0.005	10	
Current drain during time-base clock HOLD mode	IDDHOLD(2)	$V_{DD}1$	• Time-base clock HOLD mode • CF1 = V_{DD} or leave it open (when using external clock) • FmX'tal = 32.768kHz by crystal oscillation	4.5 to 6.0		13	40	
				2.5 to 4.5		3.5	30	

Note 5 : The current of the output transistors and pull-up MOS transistors are excluded.

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
10MHz	MURATA	CSLS10M0G53-B0	(15pF)	(15pF)	150Ω	4.5 to 6.0V	0.05ms	0.50ms	Internal C1, C2
		CSTCE10M0G52-R0	(10pF)	(10pF)	220Ω	4.5 to 6.0V	0.05ms	0.50ms	Internal C1, C2
5MHz	MURATA	CSTLS5M00G53-B0	(15pF)	(15pF)	470Ω	2.5 to 6.0V	0.07ms	0.70ms	Internal C1, C2
		CSTCR5M00G53-R0	(15pF)	(15pF)	470Ω	2.5 to 6.0V	0.07ms	0.70ms	Internal C1, C2

*The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit Parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	MC-306	18pF	18pF	OPEN	390kΩ	2.5 to 6.0V	1.3s	3s	

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure 4)

Notes : Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

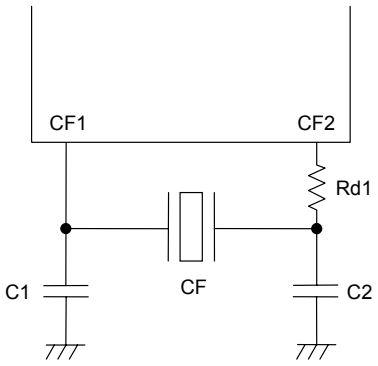


Figure 1 Ceramic oscillation circuit

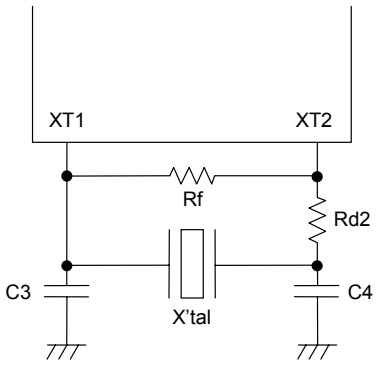


Figure 2 Crystal oscillation circuit

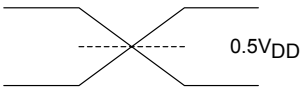
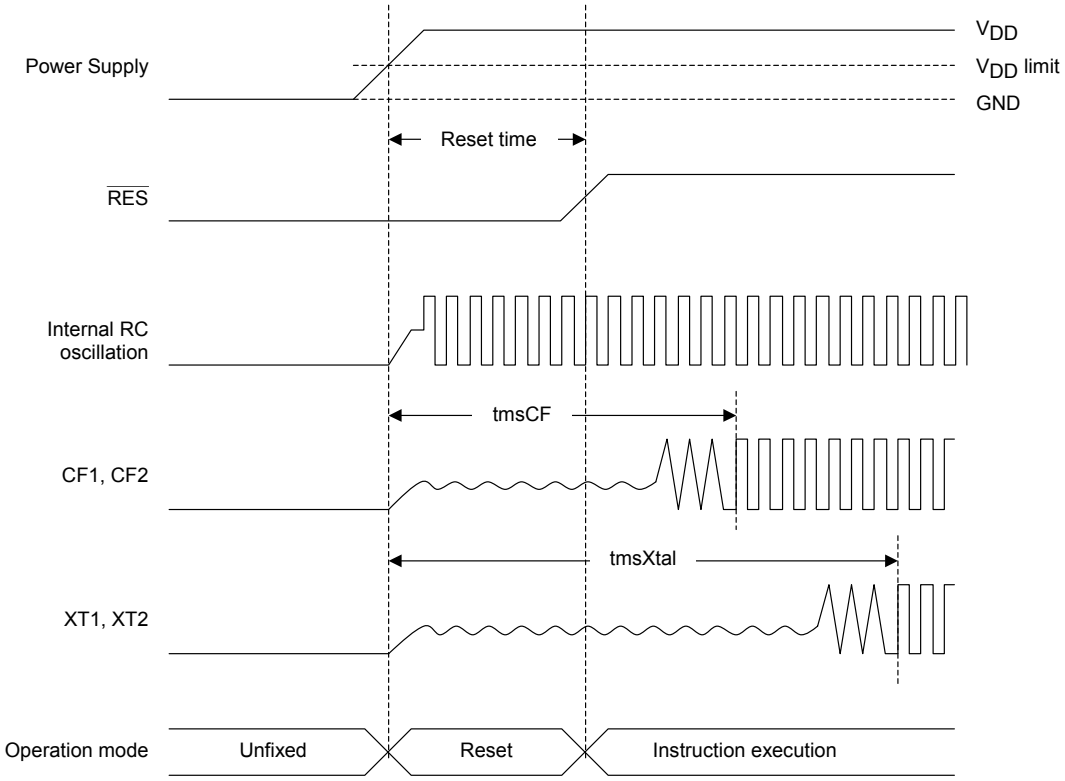
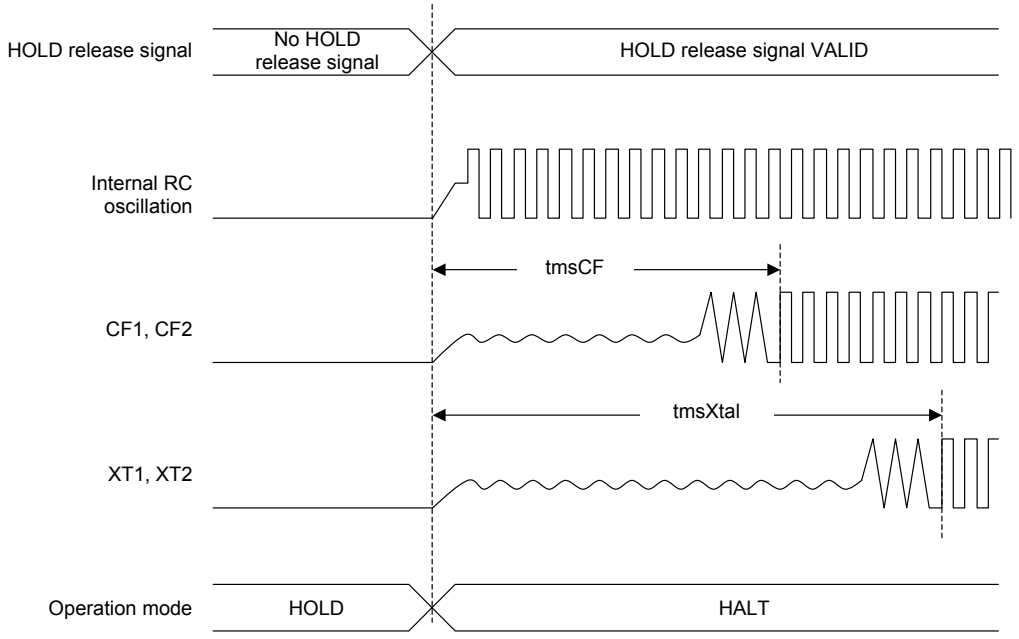


Figure 3 AC timing point

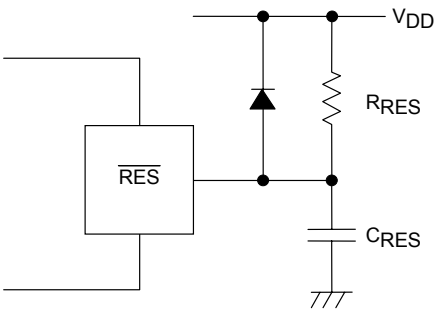


Reset time and oscillation stabilizing time



HOLD release signal and oscillation stabilizing time

Figure 4 Oscillation stabilizing time



(Note)
Select C_{RES} and R_{RES} value to assure that at least 200µs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

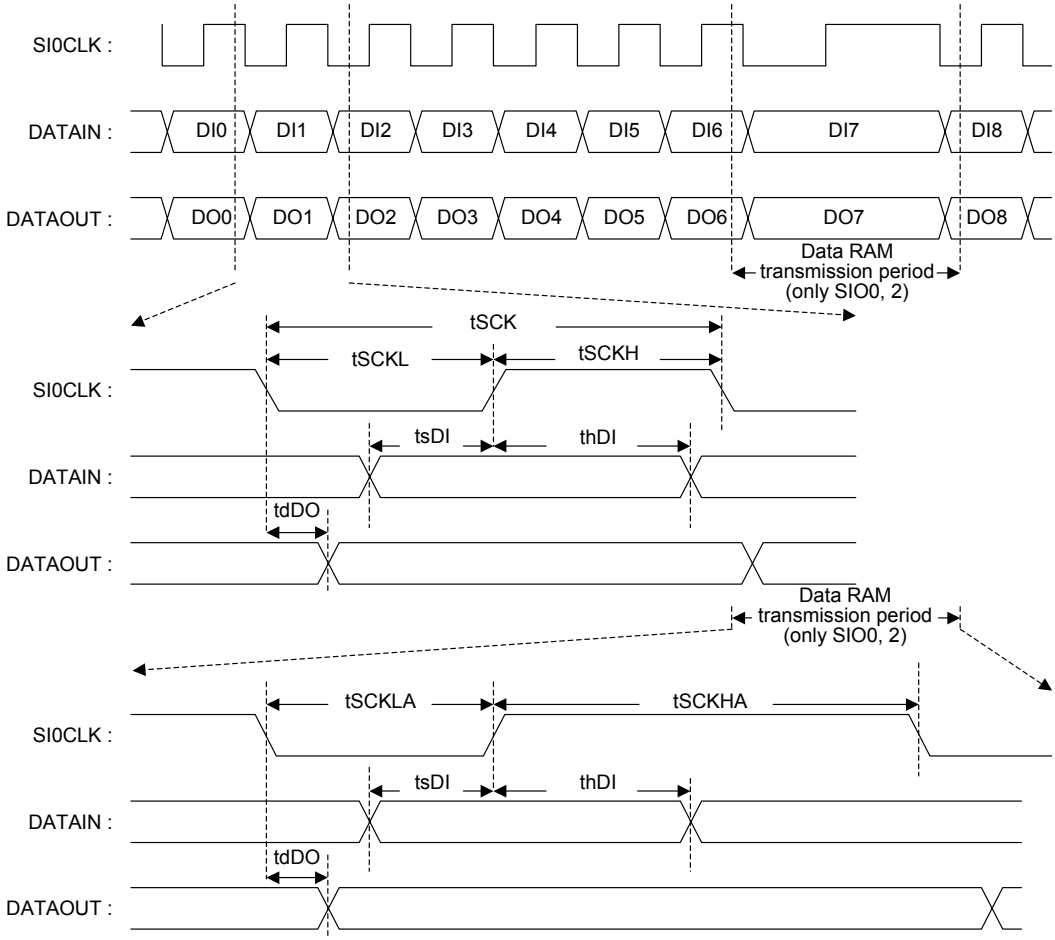


Figure 6 Serial input/output test condition

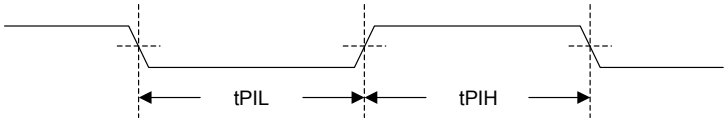
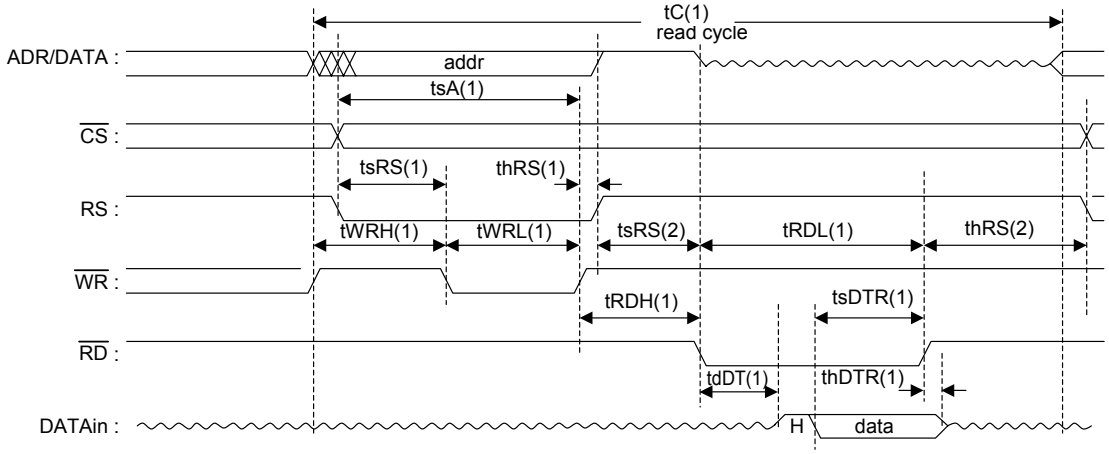


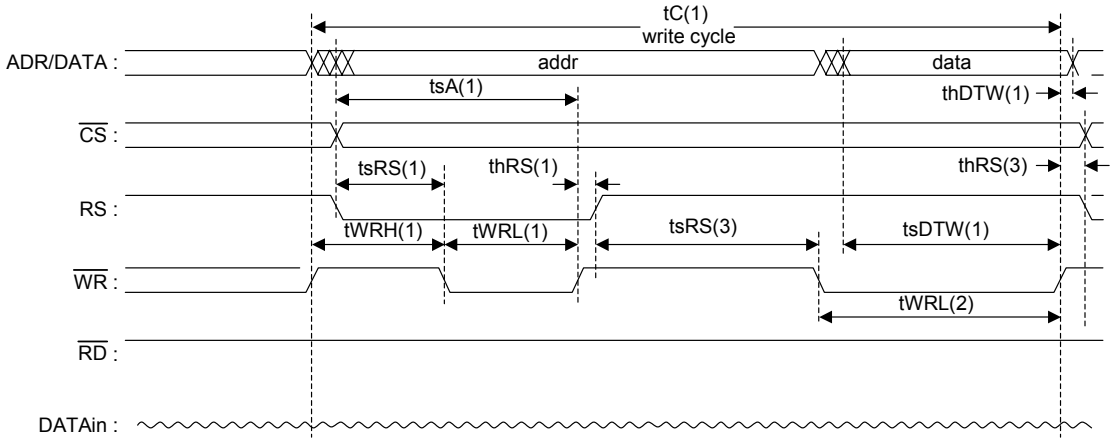
Figure 7 Pulse input timing condition

• Parallel input/output timing waveform : Indirect Setting, Read Mode



Note : If port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

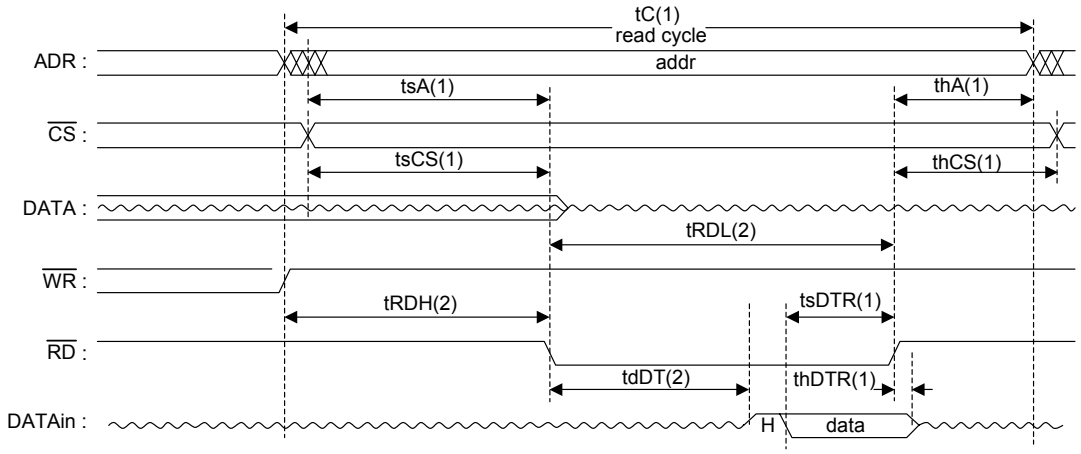
• Parallel input/output timing waveform : Indirect Setting, Write Mode



Note : If port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

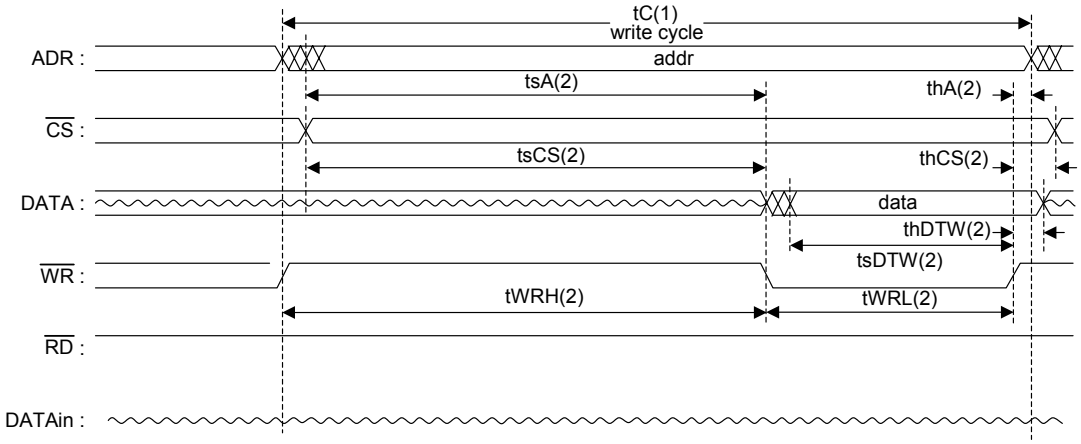
Figure 8 Indirect mode : Parallel timing diagram

• Parallel input/output timing waveform : Direct Setting, Read Mode



Note : If port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

• Parallel input/output timing waveform : Direct Setting, Write Mode



Note : If port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

Figure 9 Direct Mode : Parallel input/output timing diagrams