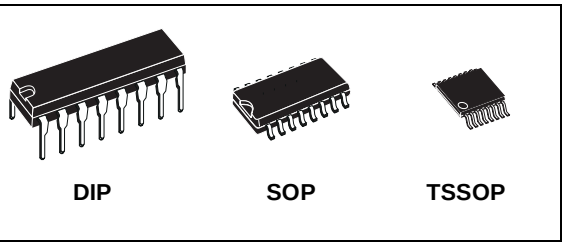
M74HC221A

DUAL MONOSTABLE MULTIVIBRATOR

- HIGH SPEED :
  t_{PD} = 24 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  STAND BY STATE :
  I_{CC}=4µA (MAX.) at T_A=25°C
  ACTIVE STATE :
  I_{CC}=700µA (TYP.) at V_{CC} = 6V
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- WIDE OUTPUT PULSE WIDTH RANGE :
  t_{WOUT} = 150 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH
  74 SERIES 221



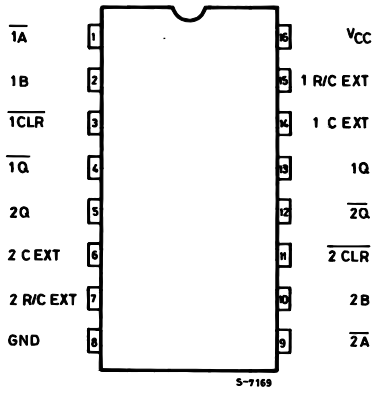
ORDER CODES

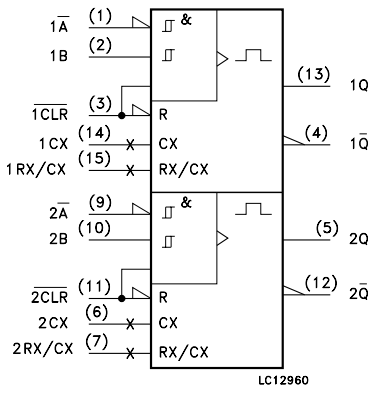
PACKAGE	TUBE	T & R
DIP	M74HC221AB1R	
SOP	M74HC221AM1R	M74HC221ARM13TR
TSSOP		M74HC221ATTR

DESCRIPTION

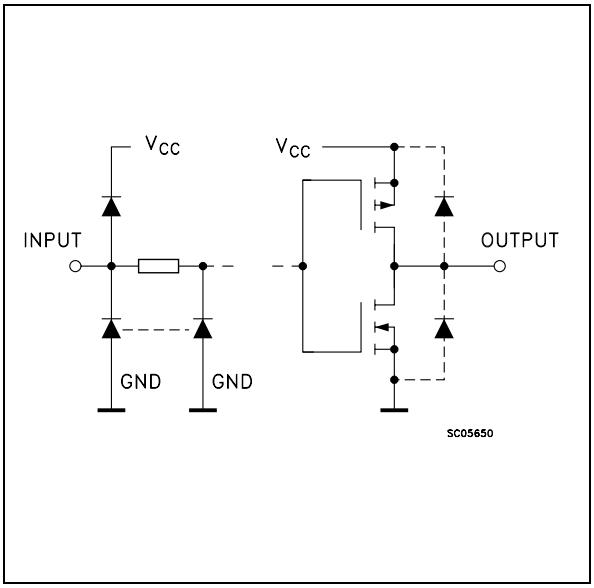
The M74HC221A is an high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.
There are two trigger inputs, A INPUT (negative edge) and B INPUT (positive edge).
Triggering on the B input occurs at a particular voltage threshold and is not related to rise and fall time of the applied pulse. The device may also be trigger by using the $\overline{CLR}$ input (positive edge) because of the Schimtt-trigger input; after triggering the output maintains the MONOSTABLE STATE for the time period determined by the external resistor Rx and capacitor Cx. Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.
Limit for values of Cx and Rx :
Cx : NO LIMIT
Rx : V_{cc} < 3.0V 5KΩ to 1MΩ
$V_{cc} \geq$ 3.0V 1KΩ to 1MΩ
K ≅ 1
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

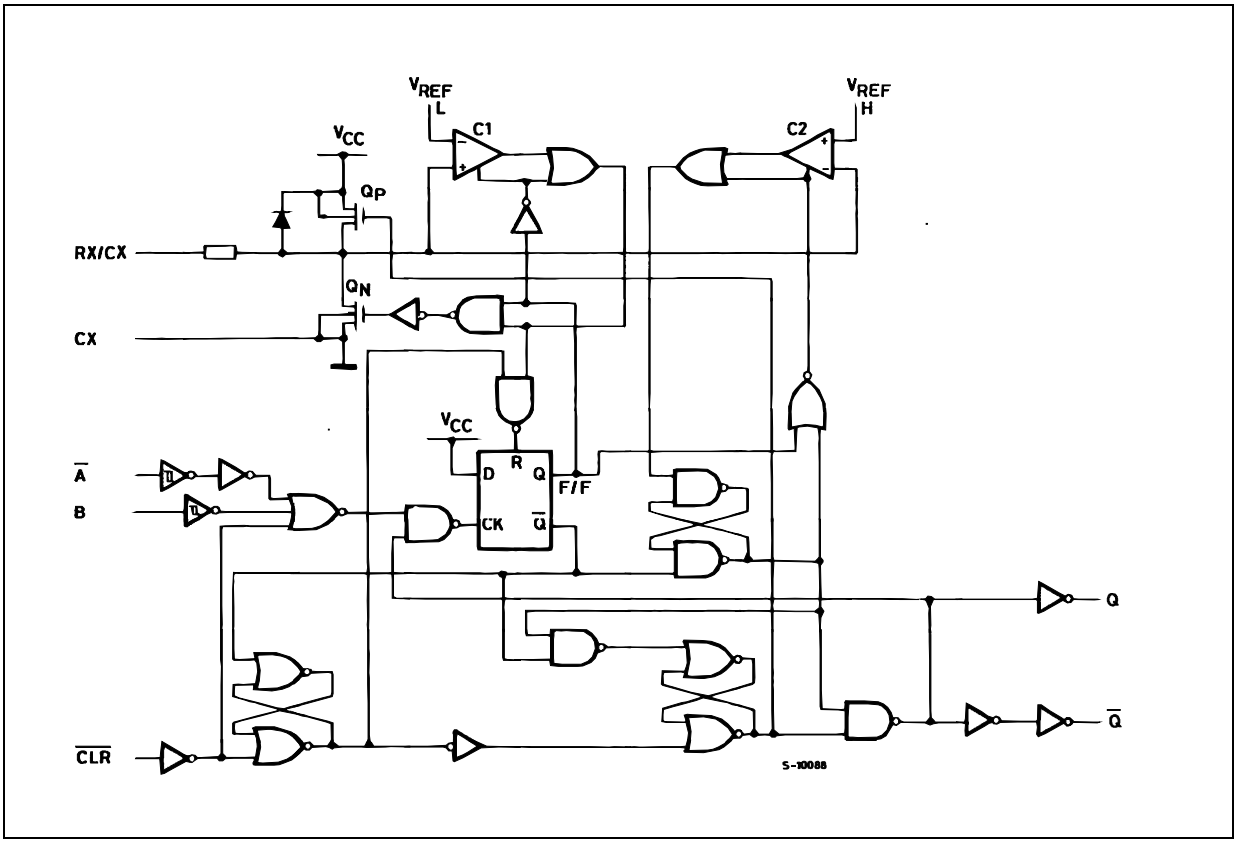
PIN No	SYMBOL	NAME AND FUNCTION
1,9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\ \overline{CLR}$ $2\ \overline{CLR}$	Direct Reset LOW and trigger Action at Positive Edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active Low)
7	$2R_X/C_X$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active High)
14, 6	$1C_X$ $2C_X$	External Capacitor Connection
15	$1R_X/C_X$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
⌜_	H	H	⌜⌟	⌜_	OUTPUT ENABLE
X	L	H	L(*)	H(*)	INHIBIT
H	X	H	L(*)	H(*)	INHIBIT
L	⌞⌜	H	⌜⌟	⌜_	OUTPUT ENABLE
L	H	⌞⌜	⌜⌟	⌜_	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

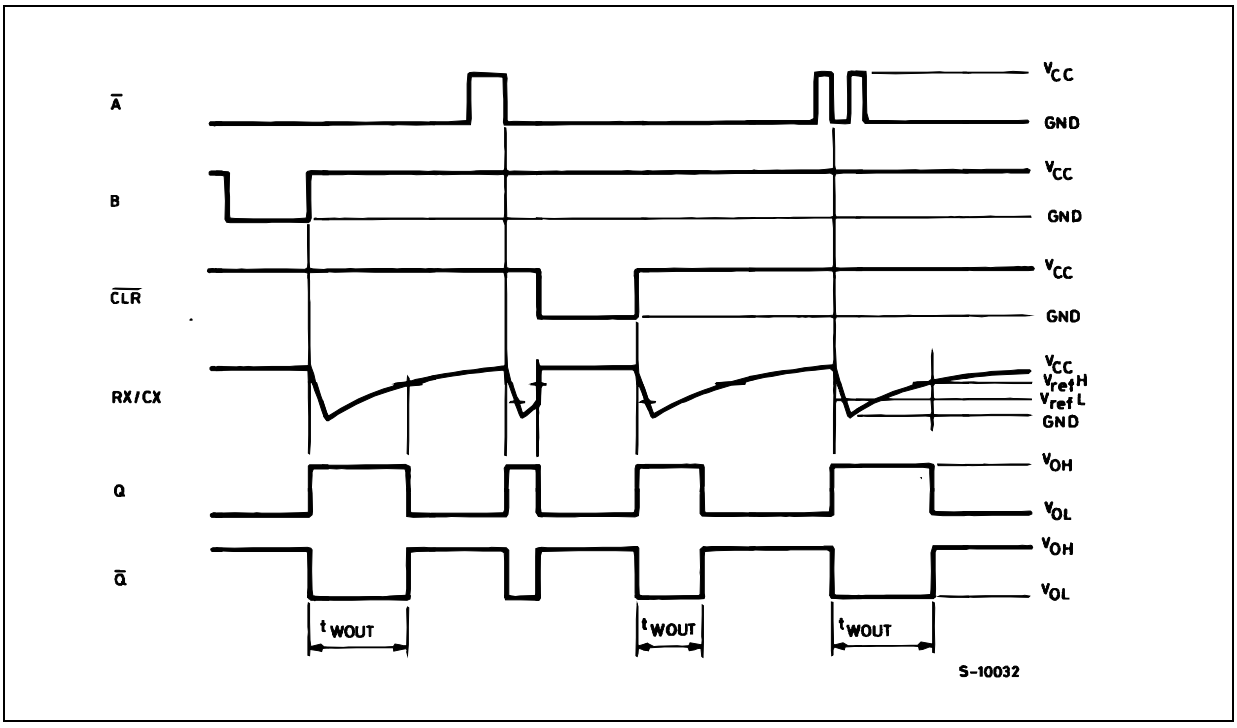
X : Don't Care
(*) : Except for monostable period

SYSTEM DIAGRAM

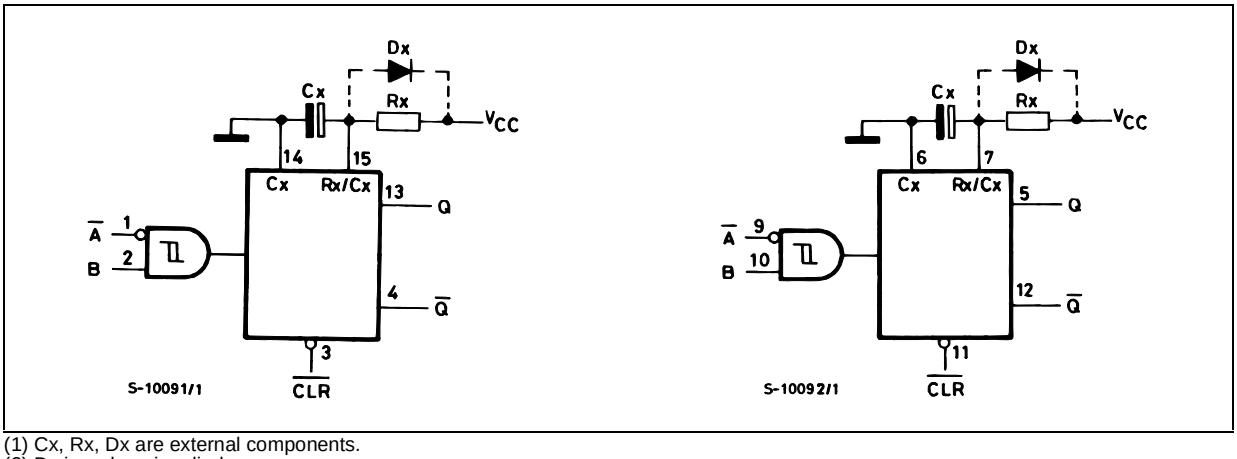


This logic diagram has not be used to estimate propagation delays

TIMING CHART



BLOCK DIAGRAM



(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode.
The external capacitor is charged to Vcc in the stand-by-state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly trough an internal parasitic diode(see figures). If Cx is sufficiently large and Vcc decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and Vcc decrease slowly, the surge current is automatically limited and damage to the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 Vcc can be calculated as follows :
$t_f \geq$ (Vcc - 0.7) x Cx/20mA
In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor,Cx, is fully charged to Vcc in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1 st) A is "LOW" and B has a falling edge;
2 nd) B is "HIGH" and A has a rising edge;
3 rd) A is "LOW" and B is HIGH and C1 has a rising edge;

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn reset the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH} . At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$tW(OUT) = Cx \cdot Rx$$

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quickly to Vcc. This means if CL input goes low the IC becomes waiting state both in operating and non operating state.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ and $\overline{A}$ only)	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns
Cx	External Capacitor		> 100	pF
Rx	External Resistor	Vcc < 3V	5K to 1M	Ω
		Vcc ≥ 3V	1K to 1M	

The Maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_I	R/C Terminal Off State Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA
$I_{CC'}$	Active State Supply Current (1)	2.0	V_I = V_{CC} or GND Pin 7 or 15 V_{IN} = V_{CC}/2		45	200		260		320	µA
		4.5			500	600		780		960	µA
		6.0			0.7	1		1.3		1.6	mA

(1) : Per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

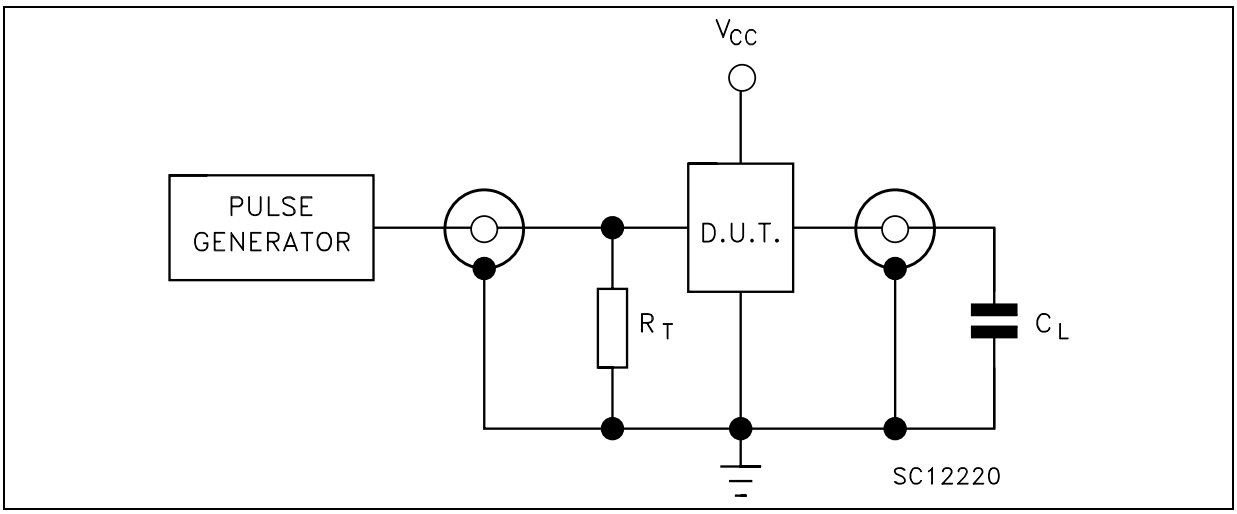
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0			102	210		265		315	ns
		4.5			30	42		53		63	
		6.0			24	36		45		54	
t_{PLH} t_{PHL}	Propagation Delay Time(CLR TRIGGER - Q, $\overline{Q}$)	2.0			102	235		295		355	ns
		4.5			30	47		59		71	
		6.0			24	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0			67	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t_{WOUT}	Output Pulse Width	2.0	Cx = 100 pF Rx = 10KΩ		1.8						µs
		4.5			1.5						
		6.0			1.4						
		2.0	Cx = 0.1µF Rx = 100KΩ		10						ms
		4.5			9.7						
		6.0			9.6						
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		20	
$t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		20	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			174						pF

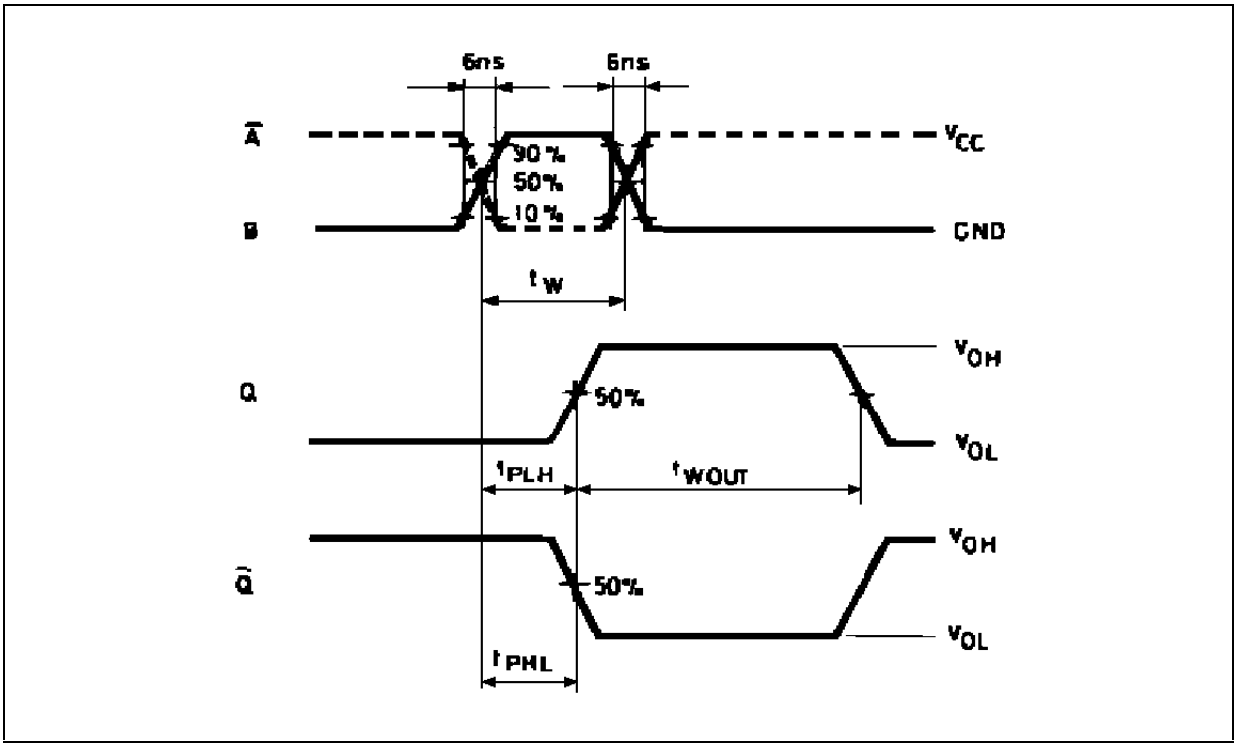
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$' Duty/100 + Ic/2(per monostable) (I_{cc}' : Active Supply current) (Duty : %)

TEST CIRCUIT

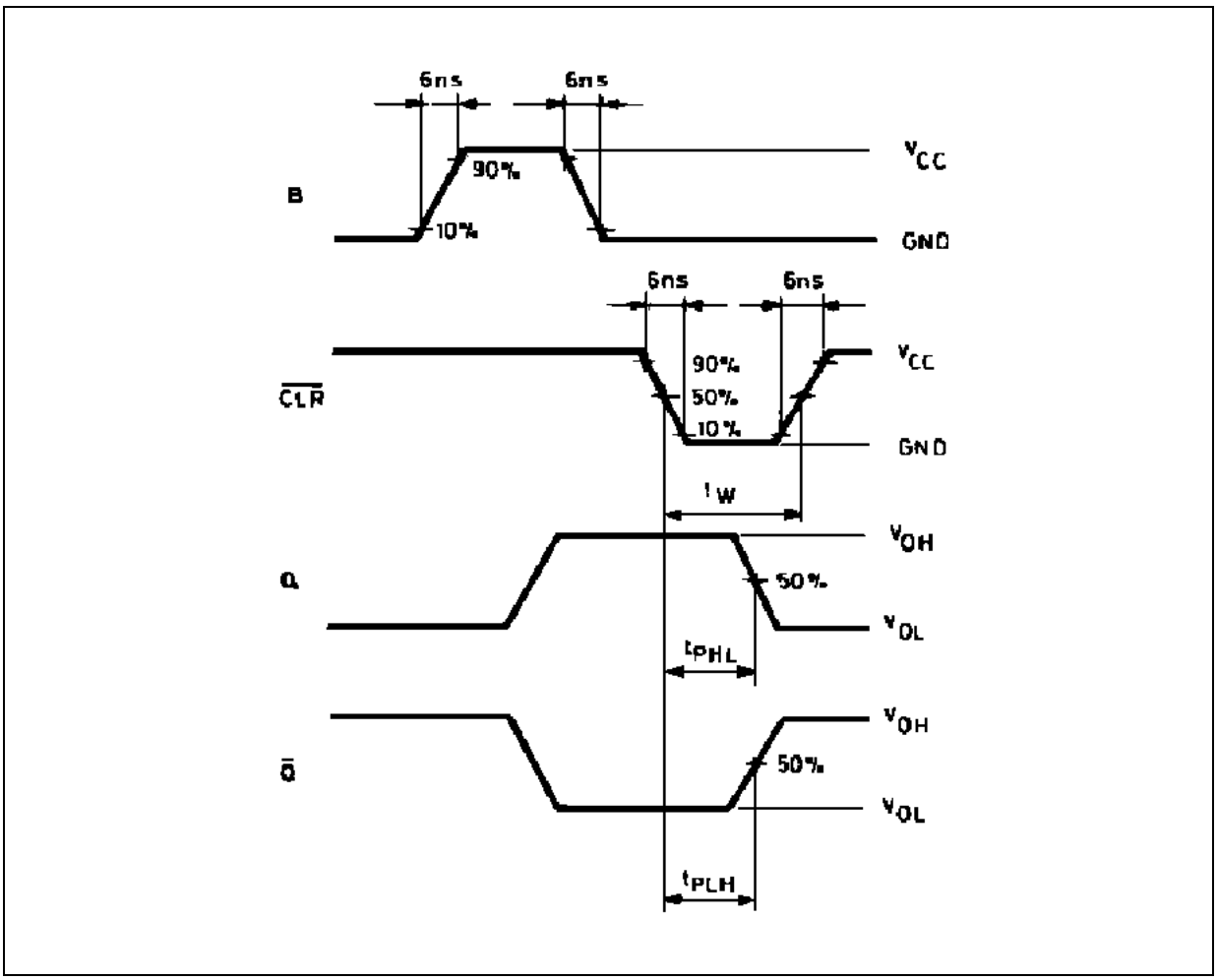


C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

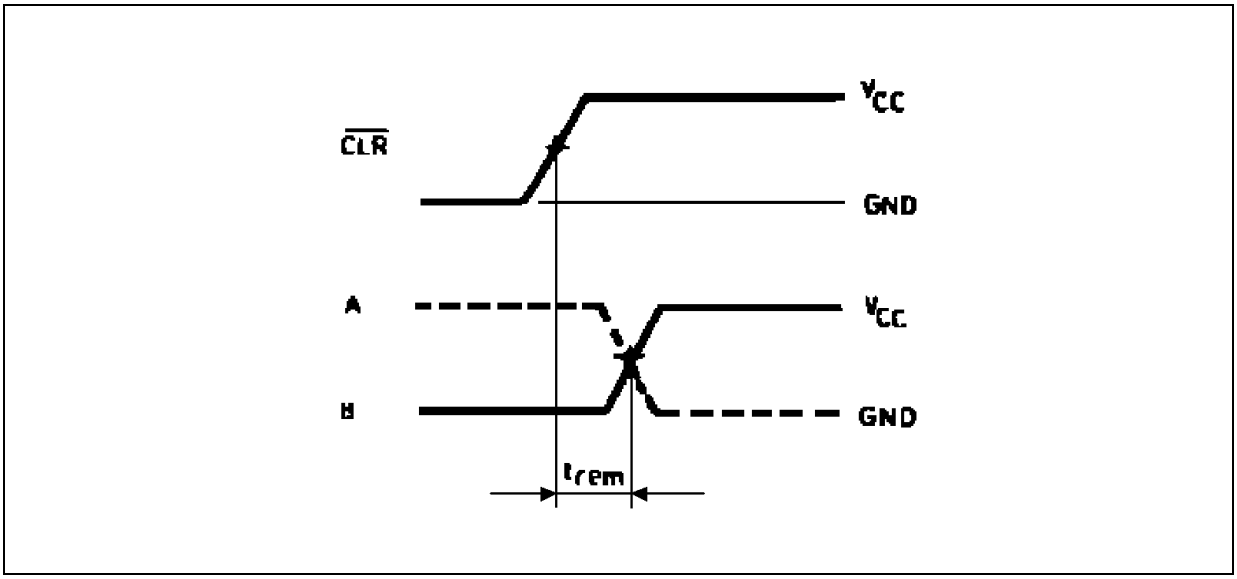
WAVEFORM 1: PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH ($\overline{A}$, B), OUTPUT PULSE WIDTH (f=1MHz; 50% duty cycle)



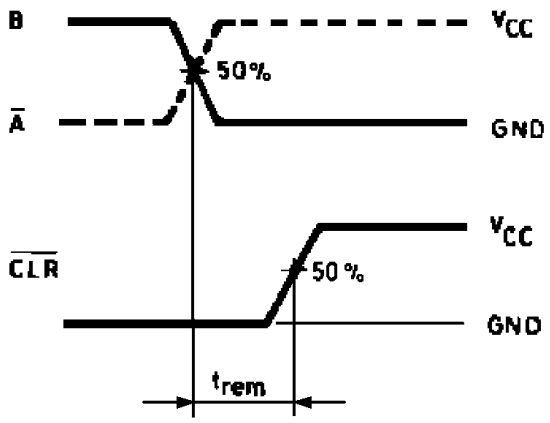
WAVEFORM 2 : MINIMUM PULSE WIDTH ($\overline{CLR}$), PROPAGATION DELAY (f=1MHz; 50% duty cycle)



WAVEFORM 3 : MINIMUM REMOVAL TIME ($\overline{CLR}$ TO A,B) (f=1MHz; 50% duty cycle)

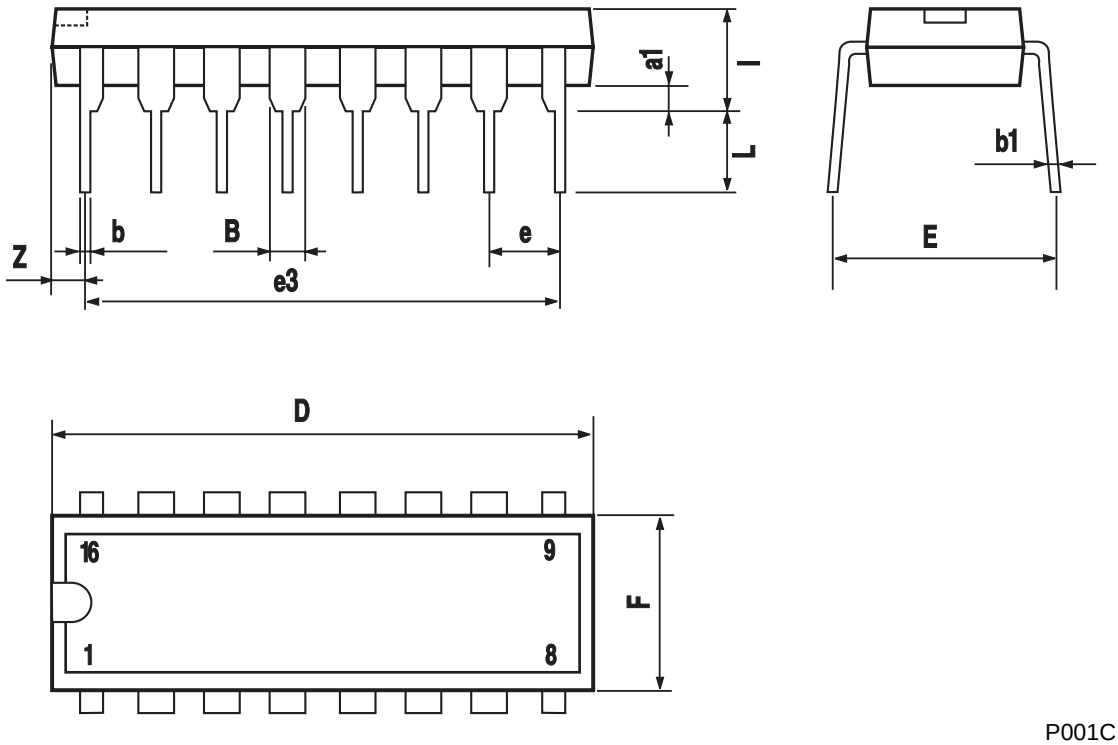


WAVEFORM 4 : MINIMUM REMOVAL TIME ($\overline{CLR}$ TO $\overline{A}$,B) (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

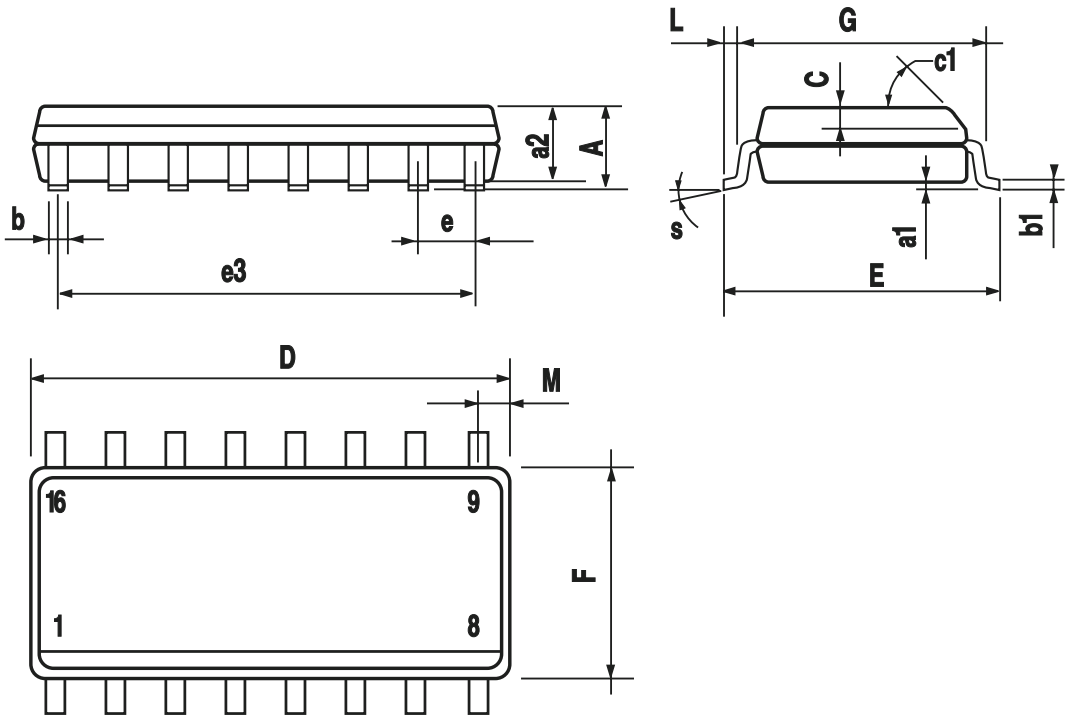
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030