

# NTB65N02R, NTP65N02R

## Power MOSFET 65 A, 24 V N-Channel TO-220, D<sup>2</sup>PAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	$V_{dc}$
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	$V_{dc}$
Thermal Resistance – Junction-to-Case Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Drain Current –	$R_{\theta JC}$ $P_D$	2.0 62.5	$^\circ\text{C}/\text{W}$ W
Continuous @ $T_C = 25^\circ\text{C}$ , Chip Continuous @ $T_C = 25^\circ\text{C}$ , Limited by Package Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	65 58 160	A A A
Thermal Resistance – Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_D$ $I_D$	67 1.86 10	$^\circ\text{C}/\text{W}$ W A
Thermal Resistance – Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_D$ $I_D$	120 1.04 7.6	$^\circ\text{C}/\text{W}$ W A
Operating and Storage Temperature Range	$T_J$ and $T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 V_{dc}$ , $V_{GS} = 10 V_{dc}$ , $I_L = 11 A_{pk}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

### PIN ASSIGNMENT

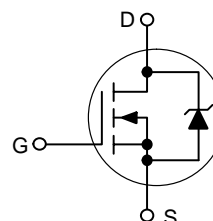
PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain



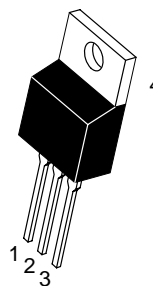
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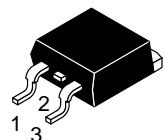
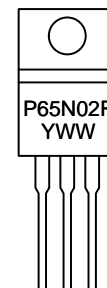
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
24 V	8.4 m $\Omega$ @ 10 V	65 A



### MARKING DIAGRAMS



TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418AA  
STYLE 2



65N02R = Specific Device Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTB65N02R	D <sup>2</sup> PAK	50 Units/Rail
NTB65N02RT4	D <sup>2</sup> PAK	800/Tape & Reel
NTP65N02R	TO-220AB	50 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTB65N02R, NTP65N02R

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	24 –	27.5 25.5	– –	V <sub>dc</sub> mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.5 10	μA <sub>dc</sub>
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	–	–	±100	nA <sub>dc</sub>

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.5 4.1	2.0 –	V <sub>dc</sub> mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> )	R <sub>DS(on)</sub>	– – –	11.2 8.4 8.2	12.5 10.5 –	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> )	g <sub>FS</sub>	–	27	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz)	C <sub>iss</sub>	–	948	1330	pF
Output Capacitance		C <sub>oss</sub>	–	456	640	
Transfer Capacitance		C <sub>rss</sub>	–	160	225	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> , R <sub>G</sub> = 3 Ω)	t <sub>d(on)</sub>	–	7.0	–	ns
Rise Time		t <sub>r</sub>	–	53	–	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	14	–	
Fall Time		t <sub>f</sub>	–	10	–	
Gate Charge	(V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> , V <sub>DS</sub> = 10 V <sub>dc</sub> ) (Note 3)	Q <sub>T</sub>	–	9.5	–	nC
		Q <sub>1</sub>	–	3.0	–	
		Q <sub>2</sub>	–	4.4	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 3) (I <sub>S</sub> = 30 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (I <sub>S</sub> = 15 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 125°C)	V <sub>SD</sub>	– – –	0.88 1.10 0.80	1.2 – –	V <sub>dc</sub>
Reverse Recovery Time	(I <sub>S</sub> = 30 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	–	29.1	–	ns
		t <sub>a</sub>	–	13.6	–	
		t <sub>b</sub>	–	15.5	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.02	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NTB65N02R, NTP65N02R

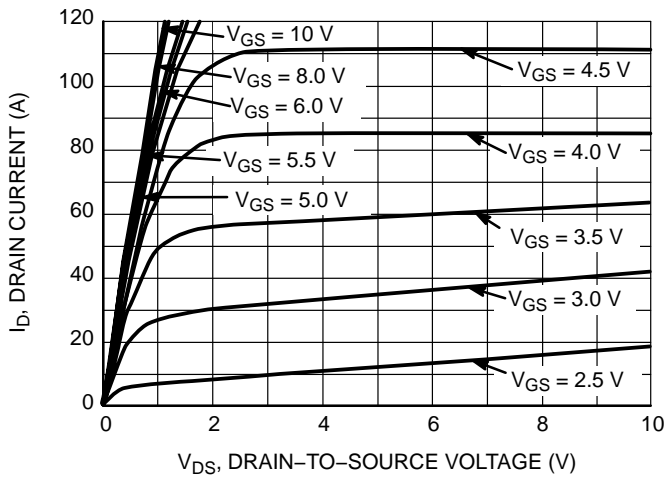


Figure 1. On-Region Characteristics

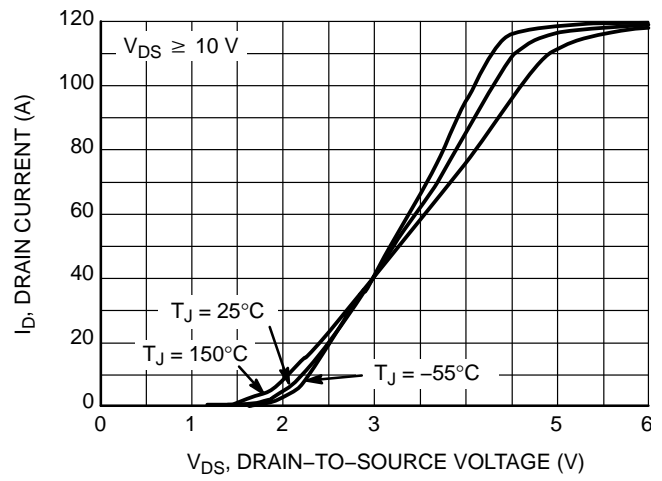


Figure 2. Transfer Characteristics

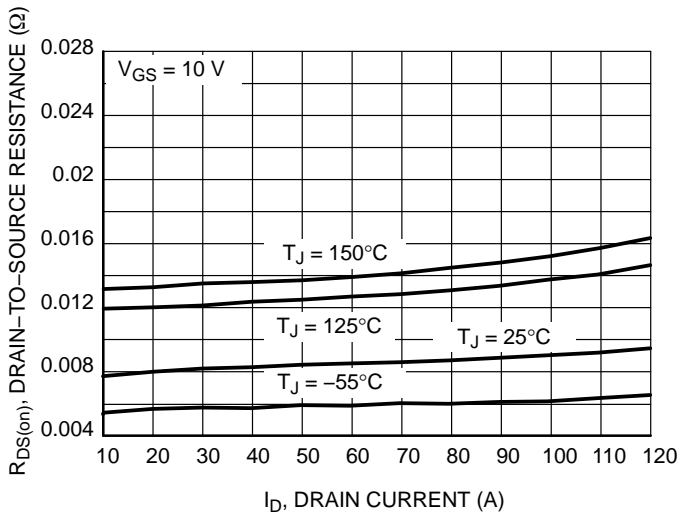


Figure 3. On-Resistance versus Drain Current and Temperature

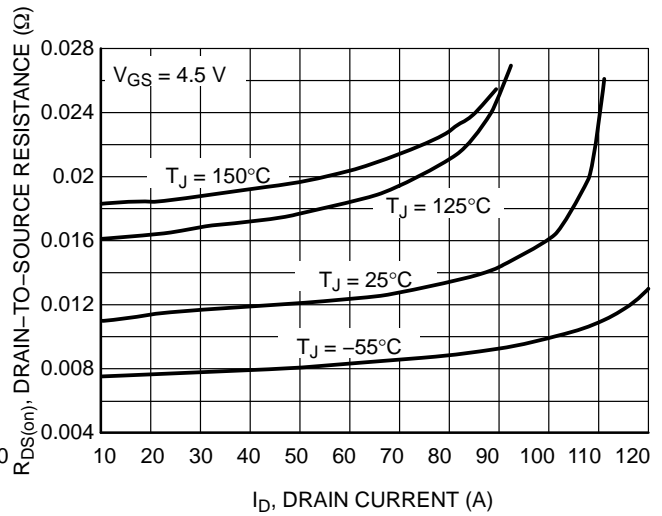


Figure 4. On-Resistance versus Drain Current and Temperature

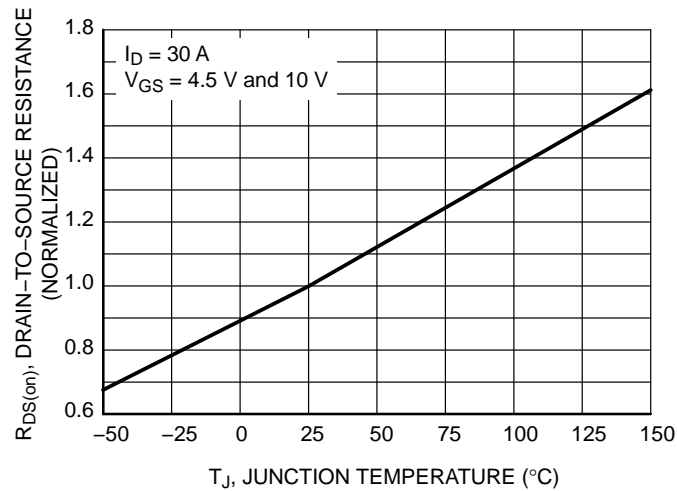


Figure 5. On-Resistance Variation with Temperature

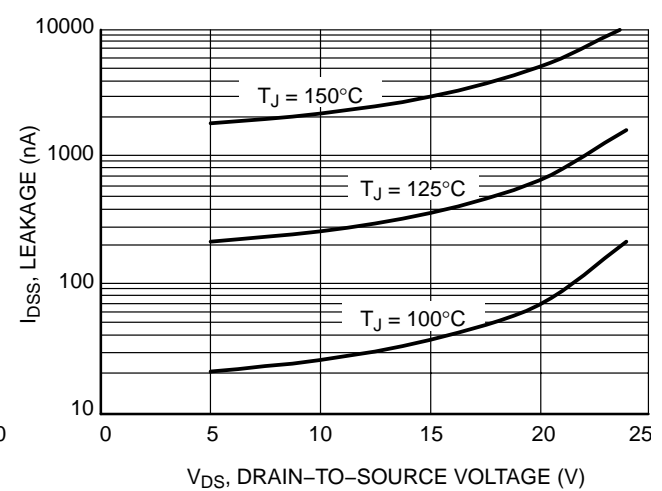
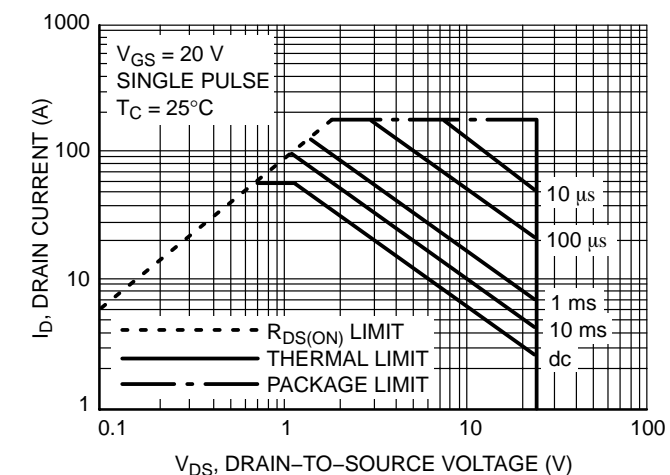
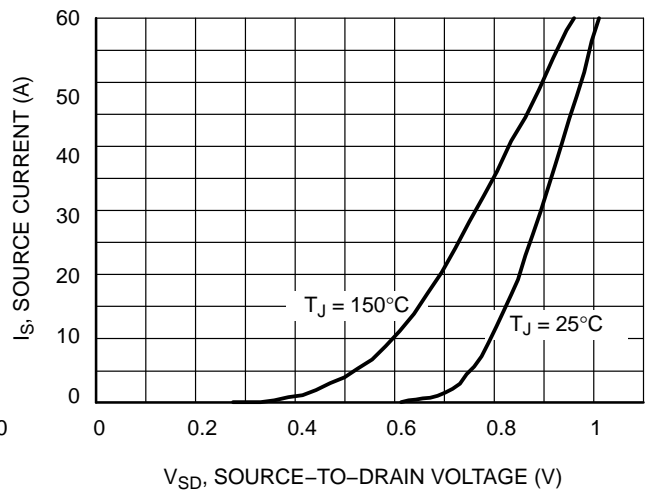
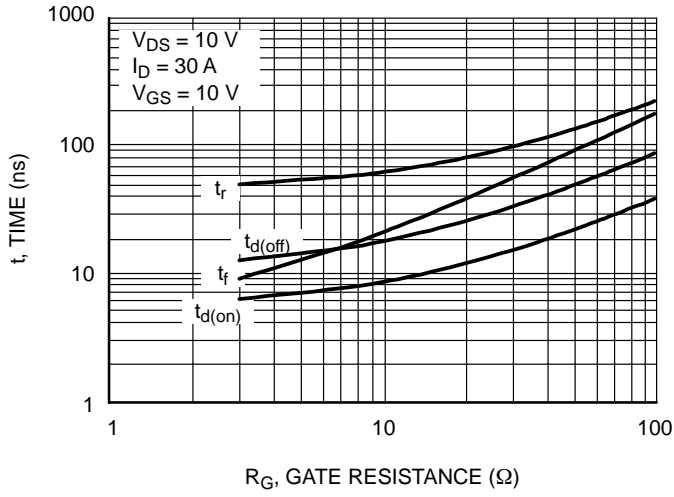
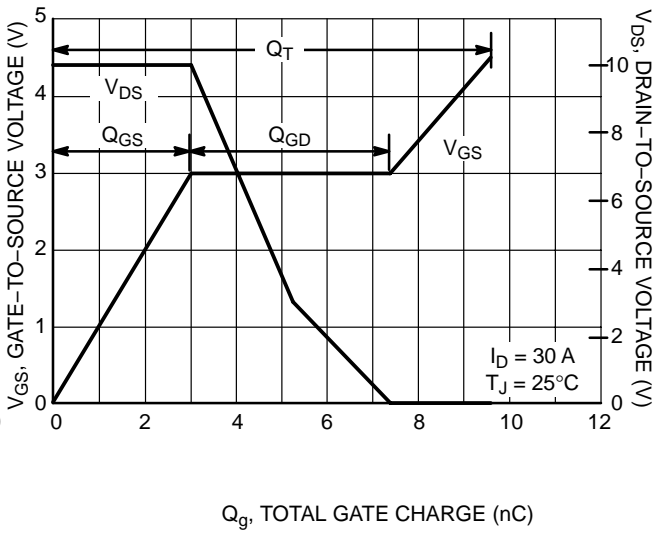
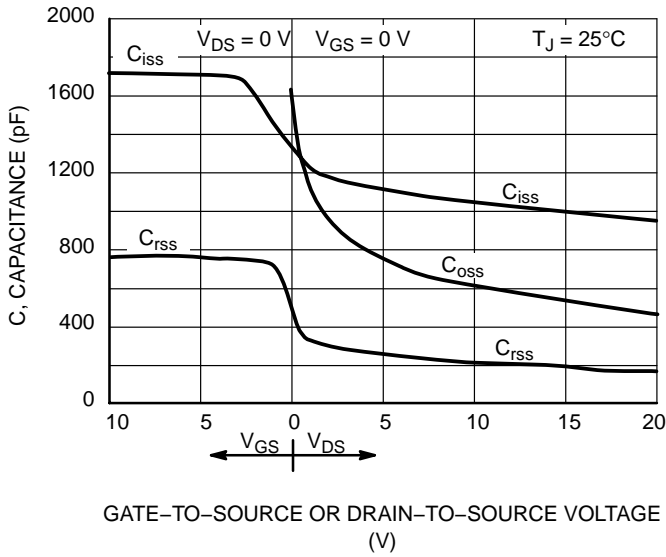


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NTB65N02R, NTP65N02R



# NTB65N02R, NTP65N02R

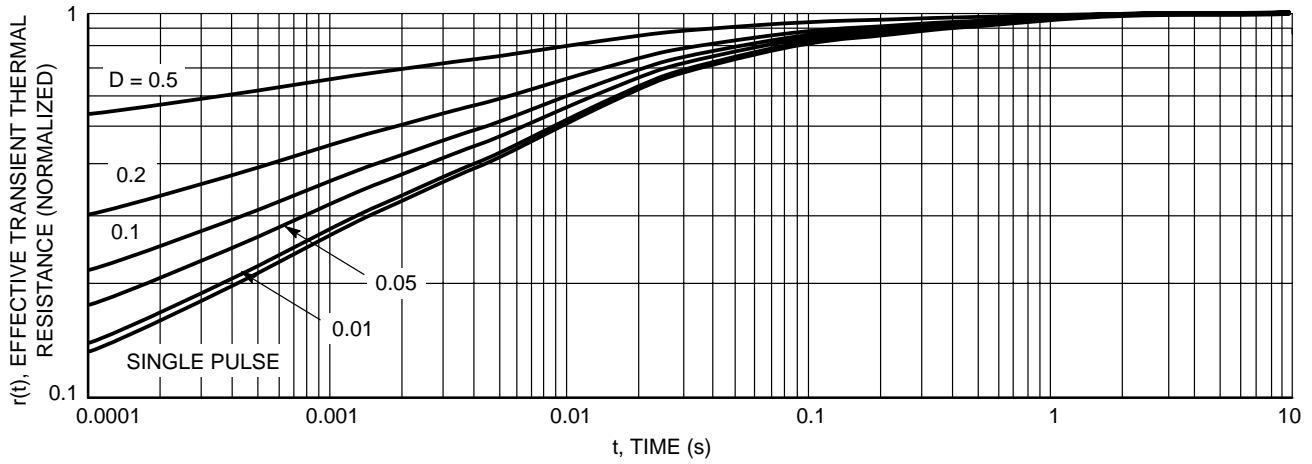
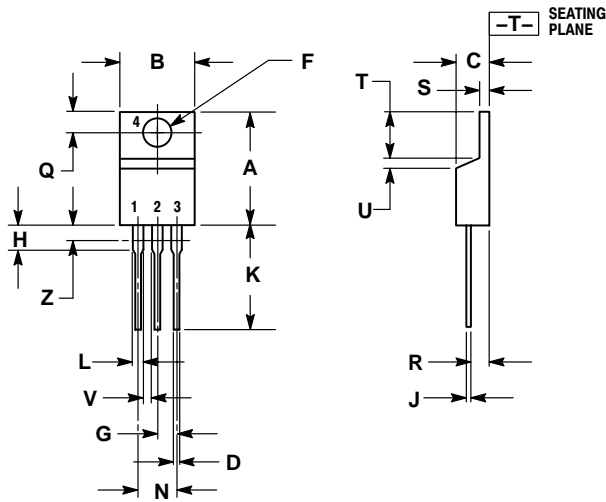


Figure 12. Thermal Response

## PACKAGE DIMENSIONS

TO-220AB  
CASE 221A-09  
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

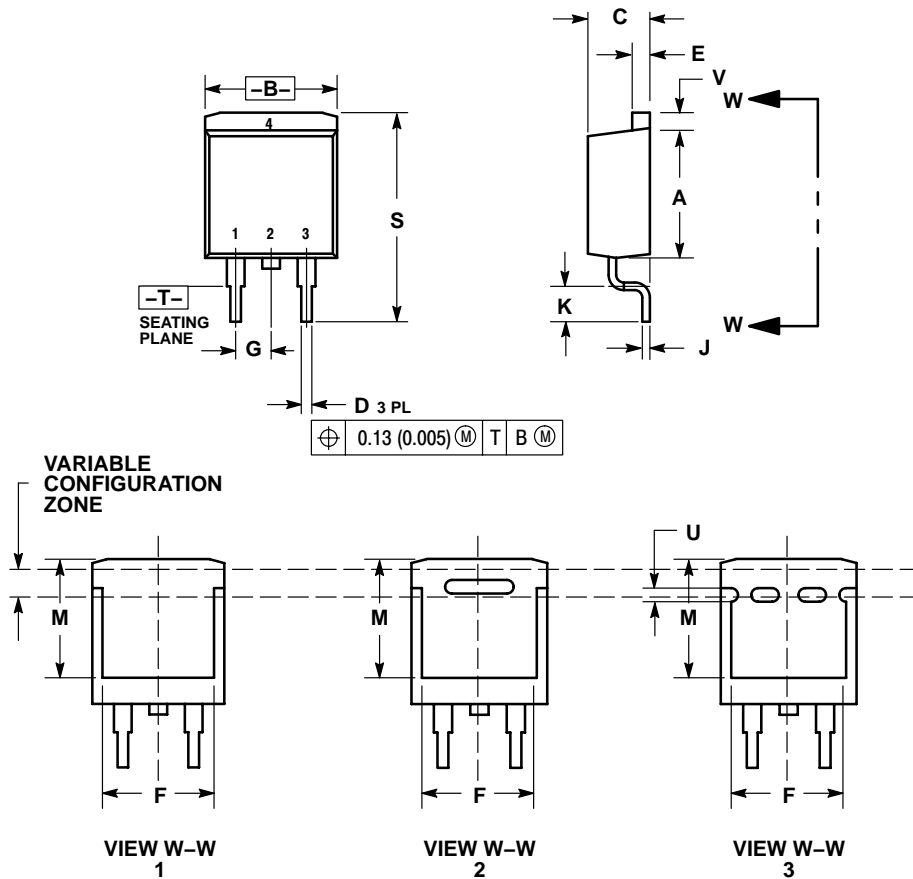
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

# NTB65N02R, NTP65N02R

## PACKAGE DIMENSIONS

D<sup>2</sup>PAK  
CASE 418AA-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	---	7.87	---
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	---	7.11	---
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:

- PIN 1: GATE  
PIN 2: DRAIN  
PIN 3: SOURCE  
PIN 4: DRAIN

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