Low Voltage/Low Power CMOS 16-Bit Microcontrollers

TMP91CW11F

1. Outline and Features

TMP91CW11 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91CW11 is housed in a 100-pin flat package (P-LQFP100-1414-0.50C).

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear ADdress space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (640 ns/ 2 bytes at 25 MHz)
  (800 ns/ 2 bytes at 20 MHz)
  (1.28 ns/ 2 bytes at 12.5 MHz)

(2) Minimum instruction execution time:
- 160 ns (at 25 MHz, V_{CC} = 5 V without external bus)
- 200 ns (at 20 MHz, V_{CC} = 5 V)
- 320 ns (at 12.5 MHz, V_{CC} = 3 V)

(3) Internal RAM: 4 Kbytes
ROM: 128 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (for both programs and data)
- Can simulatneously support 8-/16-bit width external data bus ... Dynamic data bus sizing

(5) 8-bit timer: 2 channels

(6) 8-bit PWM timer: 2 channels

(7) 16-bit timer: 2 channels

(8) General-purpose serial interface: 6 channels
- for UART/8-bit SIO: 2channels
- for UART: 1 channel
- for 8-bit SIO: 2 channels
- for I^2C bus (multi-master)/8-bit SIO: 1 channel

(9) 10-bit AD converter: 8 channels

(10) Watchdog timer

(11) Chip select/wait controller: 3 blocks

(12) Interrupts: 39 interrupts
- 9 CPU interrupts: Sofware interrupt instruction and illegal instruction
- 24 internal interrupts:
- 6 external interrupts:

7-level priority can be set.

(13) Input/output ports 79 pins
- Large current output: 6 pors, LED direct drive

(14) Standby mode
- 4 HALT modes: RUN, IDLE2, IDLE1, STOP

(15) Clock gear function
- High-frequency clock can be changed from fc to fc/16.
- Dual clock Operation

(16) Real Time Counter

(17) Operating voltage
- V_{CC} = 2.7 to 5.5 V

(18) Package: P-LQFP100-1414-0.50C

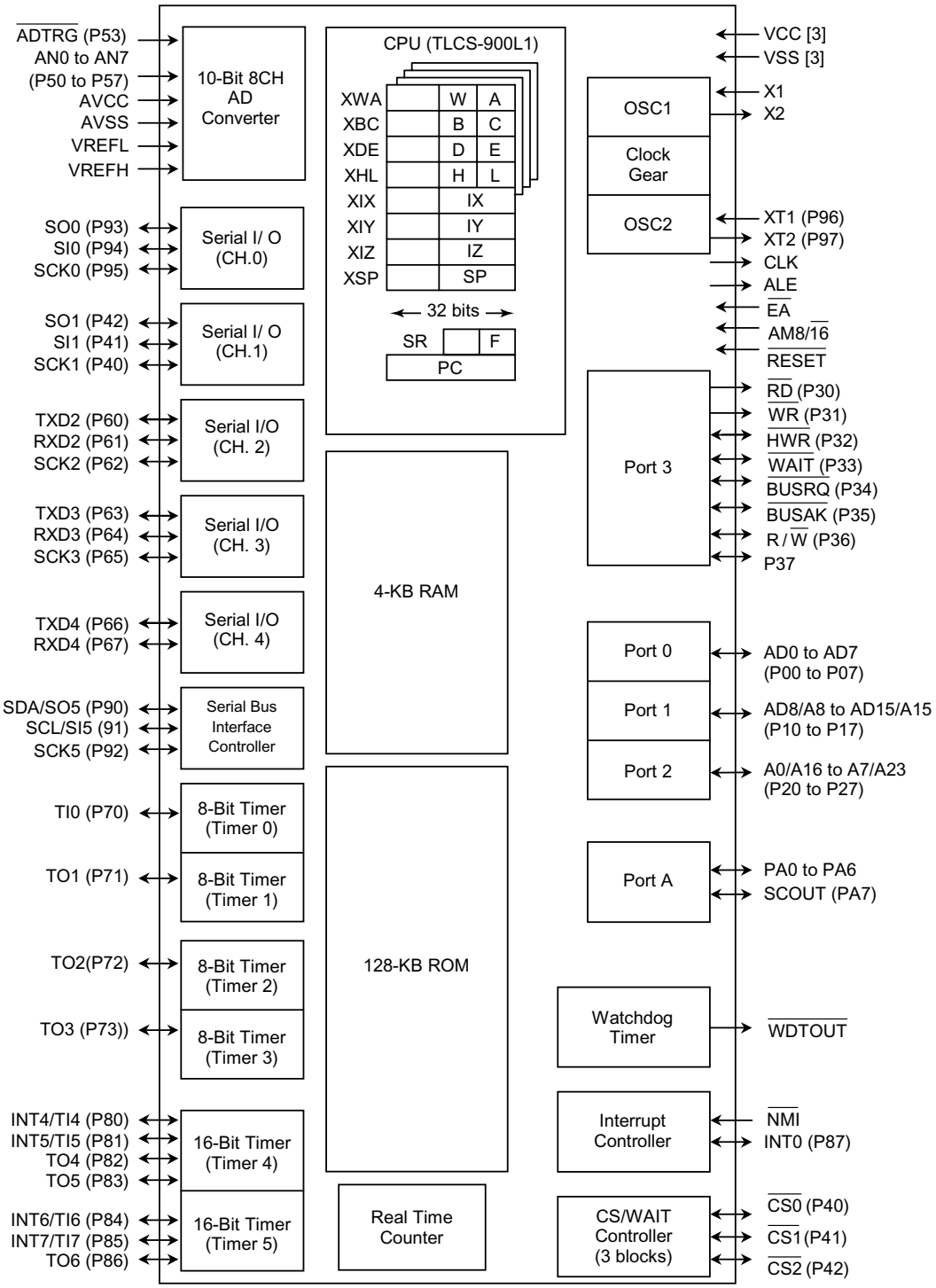


Figure 1.1 TMP91CW11 block diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91CW11F, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of TMP91CW11F.

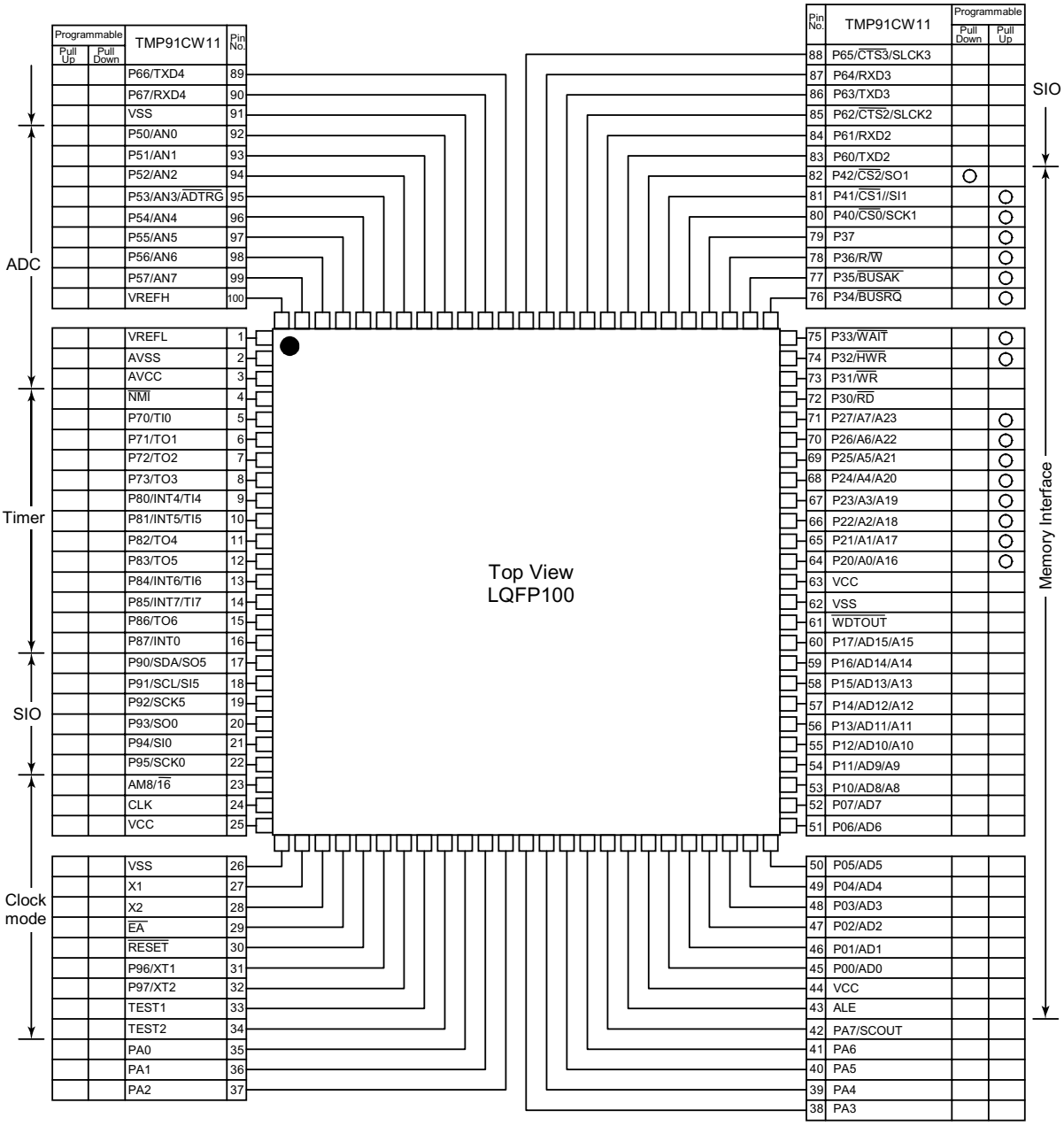


Figure 2.1.1 Pin assignment

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/4)

Pin name	Number of pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows selection of I/O on a bit basis Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port(with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$ SCK1	1	I/O Output I/O	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Serial clock I/O 1

Note: This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.2 Pin names and functions (2/4)

Pin name	Number of pins	I/O	Function
P41	1	I/O	Port 41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip select 1: Outputs 0 if address is within specified address area.
SI1		Input	Serial receive data 1
P42	1	I/O	Port 42: I/O port (with pull-down resistor)
$\overline{CS2}$		Output	Chip select 2: Outputs 0 if address is within specified address area.
SO1		Output	Serial send data 1
P50 to P52	3	Input	Port5: Input port
AN0 to AN2		Input	Analog input: Analog signal input for AD converter
P53	1	Input	Port 53: Input Port
AN3		Input	Analog input = Analog signal input for AD converter
$\overline{ADTRG}$		Input	AD external trigger
P54 to P57	4	Input	Port 5: Input Port
AN4 to AN7		Input	Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60	1	I/O	Port 60: I/O port (Programmable open drain)
TXD2		Output	Serial send data 2
P61	1	I/O	Port 61: I/O port
RXD2		Input	Serial receive data 2
P62	1	I/O	Port 62: I/O port
$\overline{CTS2}$		Input	serial data send enable 2 (Clear To Send)
SCLK2		I/O	Serial Clock I/O 2
P63	1	I/O	Port 63: I/O port
TXD3		Output	Serial send data 3
P64	1	I/O	Port 64: I/O port
RXD3		Input	Serial receive data 3
P65	1	I/O	Port 65: I/O port
$\overline{CTS3}$		Input	Serial data send enable 3 (Clear To Send)
SCLK3		I/O	Serial Clock I/O 3
P66	1	I/O	Port 66: I/O port
TXD4		Output	Serial send data 4
P67	1	I/O	Port 67: I/O port
RXD4		Input	Serial receive data 4
P70	1	I/O	Port 70: I/O port
TI0		Input	Timer input 0: timer 0 input
P71	1	I/O	Port 71: I/O port
TO1		Output	Timer output 1: Timer 0 or 1 output
P72	1	I/O	Port 72: I/O port
TO2		Output	PWM output 2: 8-bit PWM timer 2 output
P73	1	I/O	Port 73: I/O port
TO3		Output	PWM output 3: 8-bit PWM timer 3 output

Table 2.2.3 Pin names and functions (3/4)

Pin name	Number of pins	I/O	Function
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port Timer output4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port Timer output 5: Timer 4 output pin
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 SDA SO5	1	I/O I/O Output	Port 90: I/O port (Programmable open-drain) SBI I^2C bus mode channel data Serial send data 5
P91 SCL SI5	1	I/O I/O Input	Port 91: I/O port (Programmable open-drain) SBI I^2C bus mode clock Serial receive data 5
P92 SCK5	1	I/O I/O	Port 92: I/O port Serial Clock I/O 5
P93 SO0	1	I/O Output	Port 93: I/O port (Programmable open-drain) Serial send data 0
P94 SI0	1	I/O Input	Port 94: I/O port Serial receive data 0
P95 SCK0	1	I/O I/O	Port 95: I/O port Serial clock I/O 0
PA0 to PA5	6	I/O	Port A0 to A5: I/O ports (large current output)
PA6	1	I/O	Port A6: I/O port

Table 2.2.4 Pin names and functions (4/4)

Pin name	Number of pins	I/O	Function
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs system clock or 2 times oscillation clock for synchronizing to external circuit.
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs [System Clock ÷ 2] Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	Fixed to 1.
AM8/ $\overline{16}$	1	Input	Fixed to 1.
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open-Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open-Drain Output)
TEST1/TEST2	2	Output /Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin (All VCC pins are connected to the power supply source.)
VSS	3		GND pin (All Vss pins are connected to the GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: Built-in pull-up/pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

3. Operation

The following describes block by block the functions and basic operation of TMP91CW11.

Notes and restrictions for each block are outlined in 7, "Use Precautions and Restrictions" at the end of this manual.

3.1 CPU

TMP91CW11 incorporates a high-performance 16-bit CPU (900/L1-CPU). For CPU operation, see the "TLCS-900/L1 CPU".

The following describes the unique functions of the CPU used in TMP91CW11; these functions are not covered in the TLCS-900/L1 CPU section.

3.1.1 Reset

When resetting the TMP91CW11 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level for at least 10 system clocks (ten states: 16 μs at 20 MHz), resetting initializes the clock gear to fc/16.

When the reset is accepted, the CPU sets as follows:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H to FFFF02H:

  PC (7 to 0) ← data located at FFFF00H

  PC (15 to 8) ← data located at FFFF01H

  PC (23 to 16) ← data located at FFFF02H
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2 to 0> of the status register (SR) to 111 (sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).

  (Note: As this product does not support a MIN mode, don't write 0 to <MAX>.)
- Clears bits <RFP2 to 0> of the status register to 000 (sets the register bank to 0).

When reset is released, the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.

When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.
- Sets $\overline{\text{WDTOUT}}$ pin to 0. (Resetting enables the watchdog timer.)
- Pulls up the CLK pin to high level.

  (Note: During reset, do not reduce the external voltage level as this can cause malfunction.)
- Sets ALE pin to High Impedance (High-Z).

Note 1: By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

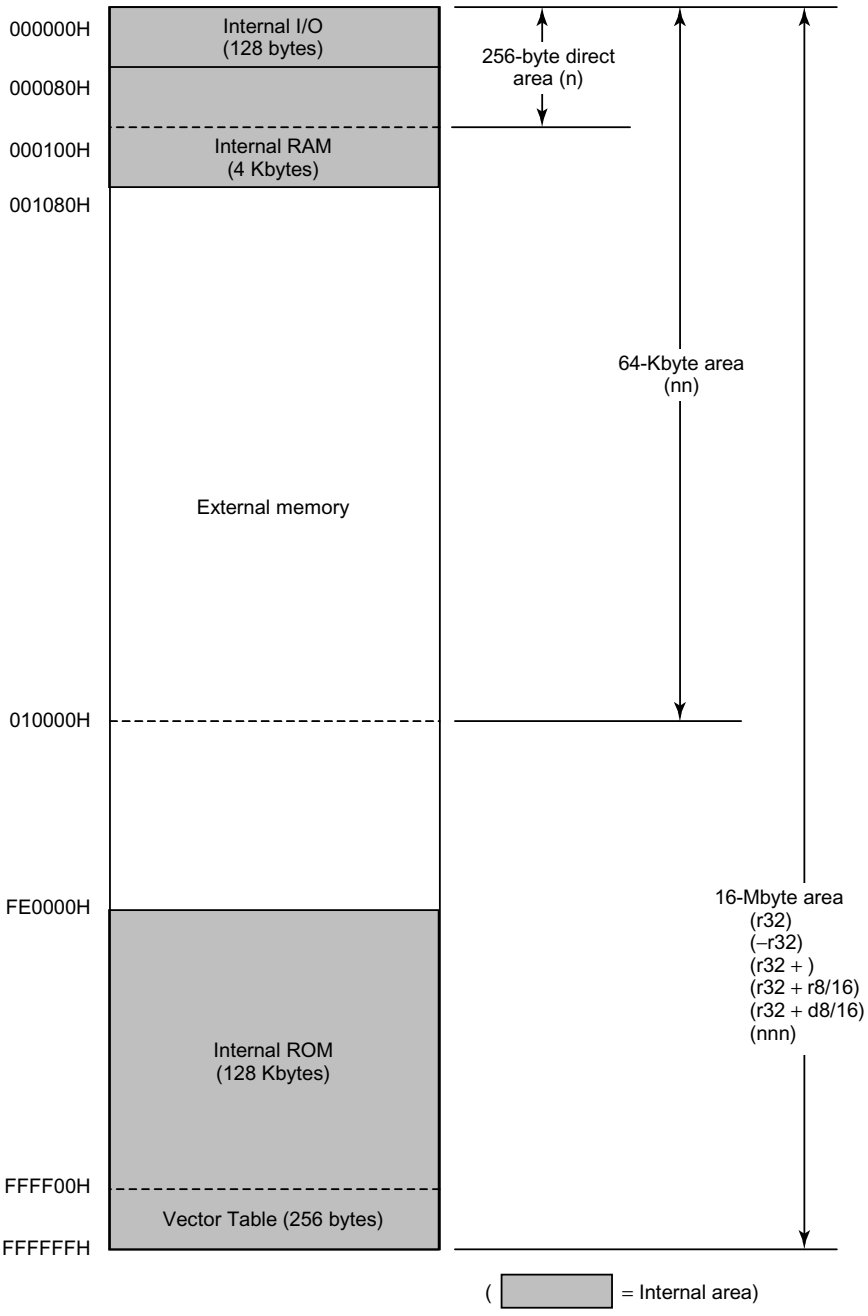
Note 2: The CLK pin is pulled up during reset. When the voltage is put down externally, there is possible to cause malfunctions.

Figure 3.1.1 shows the reset timing chart of TMP91CW11.

3.2 Memory Map

The TMP91CW11 uses an address space of 128 bytes as an internal I/O area, which is allocated to addresses 000000H to 00007FH. The CPU can access this internal I/O area with short instruction code using the direct addressing mode.

Figure 3.2.1 shows the memory map and the access ranges corresponding to the CPU addressing modes.



Note: After reset, the stack pointer XSP is set to 100H.

Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

X used in an expression shows a frequency of clock f_{FPH} selected by SYSCR1 <SYSCK>. If a clock gear or a low speed oscillator is selected, a value of X is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1 <SYSCK, GEAR 2 to 0> = 0000).

Parameter	Symbol	Pin	Rating	Unit
Power Supply voltage	V_{CC}		−0.5 to 6.5	V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT}	P96, P97, PA0 to A5, P60, P91 to 93 (for open-drain)	−0.5 to V_{CC} + 0.5	V
Output Current (per pin)	I_{OUT1} I_{OUT2} I_{OUT3}	Only PA0 to A5 Except PA0 to A5	20 2 −2	mA mA mA
Output Current (total)	ΣI_{OUT1} ΣI_{OUT2} ΣI_{OUT3}	Total PA0 to A5 Total	120 80 −80	mA mA mA
Power Dissipation (Ta = 85°C)	P D		600	mW
Soldering Temperature	Tsolder		260	°C
Storage Temperature	T_{STG}		−65 to 150	°C
Operating Temperature	Topr		−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2) (Vss = 0 V, Ta = – 40 to 85°C)

Parameter		Symbol	Condition		Min	Typ. (note)	Max	Unit
Power Supply Voltage (Avcc = Vcc, Avss = Vss)		VCC	fc = 4 to 25 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input Low Voltage	AD0 to 15	VIL	$V_{cc} \geq 4.5$ V		–0.3		0.8	V
			$V_{cc} < 4.5$ V				0.6	
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VIL1	V_{cc} = 2.7 to 5.5 V				0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, P40 to 41, P87, P90 to 92, P94, P95	VIL2					0.25 V_{CC}	
	$\overline{EA}$, AM8/$\overline{16}$	VIL3					0.3	
	X1	VIL4					0.2 V_{CC}	
Input High Voltage	AD0 to 15	VIH	$V_{cc} \geq 4.5$ V		2.2		V_{cc} + 0.3	
			$V_{cc} < 4.5$ V		2.0			
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VIH1	V_{cc} = 2.7 to 5.5 V		0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, P40 to 41, P87, P90 to 92, P94, P95	VIH2			0.75 V_{CC}			
	$\overline{EA}$, AM8/$\overline{16}$	VIH3			V_{CC} – 0.3			
	X1	VIH4			0.8 V_{CC}			

Note: Typical values are for Ta = 25 °C and Vcc = 5 V unless other wise noted.

4.2 DC Characteristic (2/2) (Vss = 0 V, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output Low Voltage (except PA0 to PA5)	V_{OL}	I OL = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output Low Current (PA0 to 5)	I_{OLA}	VOL = 1.0 V (Vcc = 3 V ± 10%)	7			mA
		VOL = 1.0 V (Vcc = 5 V ± 10%)	16			
Output High Voltage	V_{OH1}	I OH = –400 μA (Vcc = 3 V ± 10%)	2.4			V
	V_{OH2}	I OH = –400 μA (Vcc = 5 V ± 10%)	4.2			
Darlington Drive Current (8 Output Pins max.)	I_{DAR} (Note 2)	V EXT = 1.5 V R EXT = 1.1 kΩ (Vcc = 5 V ± 10% only)	–1.0		–3.5	mA
Input Leakage Current	I_{LI}	$0.0 \le V_{IN} \le V_{CC}$		0.02	±5	μA
Output Leakage Current	I_{LO}	$0.2 \le V_{IN} \le V_{CC} - 0.2$		0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	VIL2 = 0.2 Vcc, VIH 2 = 0.8 Vcc	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor	R_{RST}	Vcc = 5 V ± 10%	50		150	kΩ
		Vcc = 3 V ± 10%	80		200	
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, P40, P41, P87, P90 to 92, P94, P95	V_{TH}		0.4	1.0		V
Programmable Pull Down Resistor	R_{KL}	Vcc = 5 V ± 10%	10		80	kΩ
		Vcc = 3 V ± 10%	30		150	
Programmable Pull Up Resistor	R_{KH}	Vcc = 5 V ± 10%	50		150	
		Vcc = 3 V ± 10%	100		300	
NORMAL	Icc	Vcc = 5 V ± 10% fc = 25 MHz		45	55	mA
RUN				25	40	
IDLE2				15	30	
IDLE1				3	10	
NORMAL		Vcc = 3 V ± 10% fc = 12.5 MHz (Typ: Vcc = 3.0 V)		13	20	mA
RUN				7	11	
IDLE2				4	7.5	
IDLE1				0.8	1.8	
SLOW		Vcc = 3 V ± 10% fs = 32.768 kHz (Typ: Vcc = 3.0 V)		110	200	μA
RUN				22	52	
IDLE2				14	52	
IDLE1				6	40	
STOP		Ta ≤ 50°C, Vcc = 2.7 to 5.5 V		0.2	10	μA
		Ta ≤ 70°C, Vcc = 2.7 to 5.5 V			20	
		Ta ≤ 85°C, Vcc = 2.7 to 5.5 V			50	

Note 1: Typical values are for Ta = 25°C and Vcc = 5 V unlesss otherwise noted.

Note 2: I-DAR is guranteed for total of up to 8 ports.

4.3 AC Characteristics

(1) Vcc = 5 V ± 10% (fc = 4 to 20 MHz)
(fs = 30 to 34 kHz)

External-bus access isn't supported in over 20 MHz.

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	33.3 μs	62.5		50		ns
2	CLK width	t_{CLK}	2x – 40		85		60		ns
3	A0 to 23 Valid→CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→A0 to 23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to 15 Valid→ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→A0 to 15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall→$\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to 15 Valid→$\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to 23 Valid→$\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ rise→A0 to 23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to 15 Valid→D0 to 15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to 23 Valid→D0 to 15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ fall→D0 to 15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ rise→D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise→A0 to 15 output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise→D0 to 15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ fall→ $\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid→PORT input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to 23 Valid→PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise→PORT Valid	t_{CP}		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V /Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

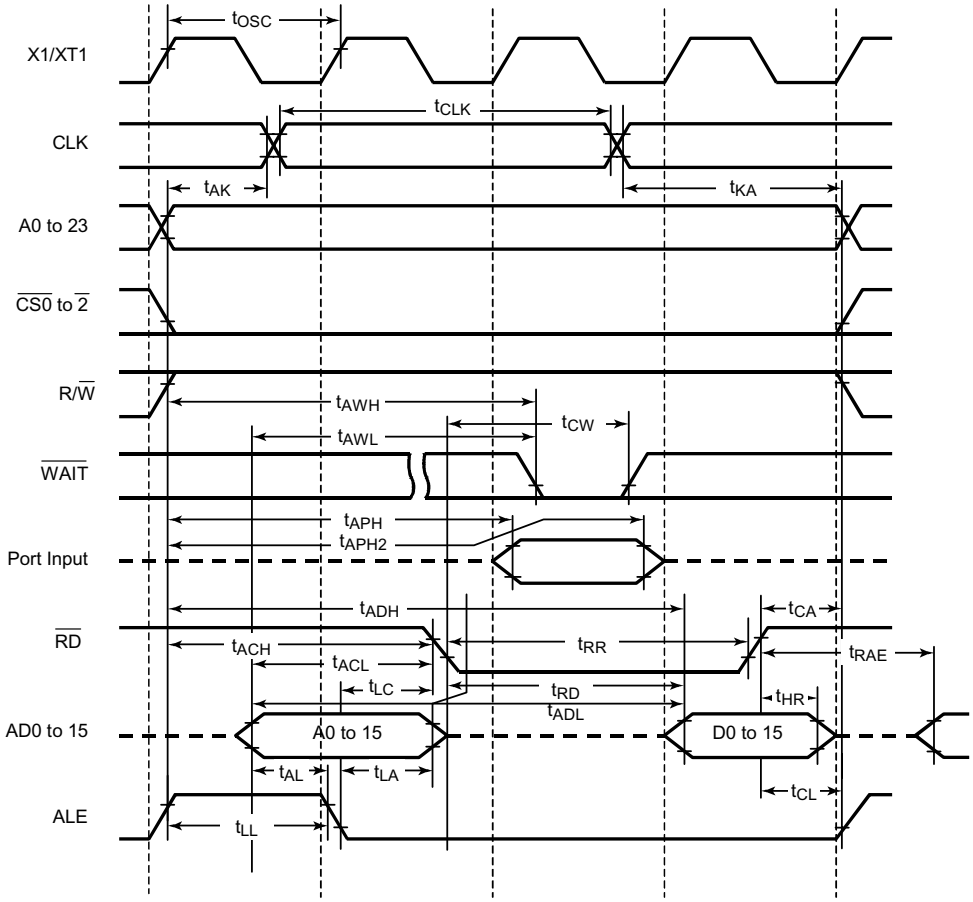
(2) Vcc = 3 V ± 10% (fc = 4 to 12.5 MHz)
(fs = 30 to 34 kHz)

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	80	33.3 μs	80		ns
2	CLK width	t_{CLK}	2x – 40		120		ns
3	A0 to 23 Valid→CLK Hold	t_{AK}	0.5x – 30		10		ns
4	CLK Valid→A0 to 23 Hold	t_{KA}	1.5x – 80		40		ns
5	A0 to 15 Valid→ALE fall	t_{AL}	0.5x – 35		5		ns
6	ALE fall→A0 to 15 Hold	t_{LA}	0.5x – 35		5		ns
7	ALE High width	t_{LL}	x – 60		20		ns
8	ALE fall→ $\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5x – 35		5		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ALE rise	t_{CL}	0.5x – 40		0		ns
10	A0 to 15 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	x – 50		30		ns
11	A0 to 23 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5x – 50		70		ns
12	$\overline{RD}$/$\overline{WR}$ rise→A0 to 23 Hold	t_{CA}	0.5x – 40		0		ns
13	A0 to 15 Valid→D0 to 15 input	t_{ADL}		3.0x – 110		130	ns
14	A0 to 23 Valid→D0 to 15 input	t_{ADH}		3.5x – 125		155	ns
15	$\overline{RD}$ fall→D0 to 15 input	t_{RD}		2.0x – 115		45	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		120		ns
17	$\overline{RD}$ rise→D0 to 15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$ rise→A0 to 15 output	t_{RAE}	x – 25		55		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		120		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 120		40		ns
21	$\overline{WR}$ rise→D0 to 15 Hold	t_{WD}	0.5x – 40		0		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWH}		3.5x – 130		150	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWL}		3.0x – 100		140	ns
24	$\overline{RD}$/$\overline{WR}$ fall→ $\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		160		ns
25	A0 to 23 Valid→PORT input	t_{APH}		2.5x – 120		80	ns
26	A0 to 23 Valid→PORT Hold	t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ rise→PORT Valid	t_{CP}		200		200	ns

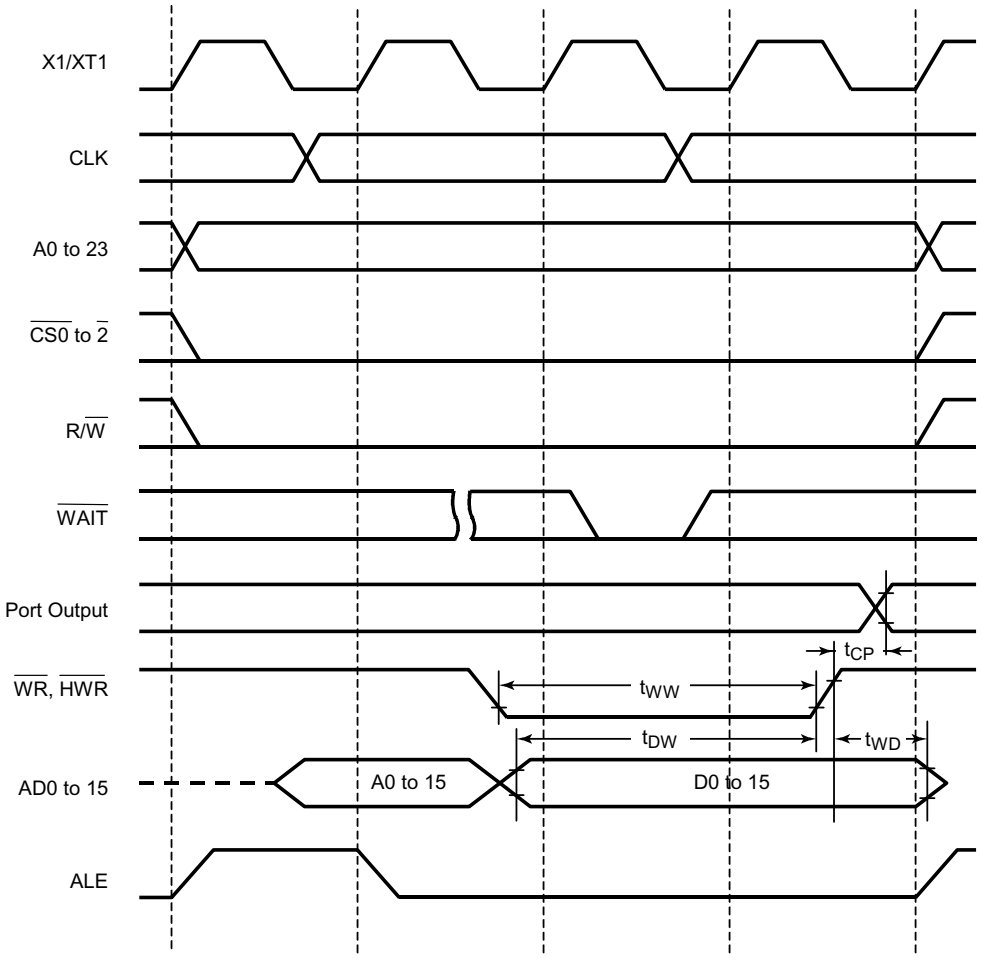
AC Measuring Conditions

- Output Level: High 0.7 Vcc / Low 0.3 Vcc, CL = 50 pF
- Input Level: High 0.9 Vcc / Low 0.1 Vcc

(1) Read Cycle


tOSC
X1/XT1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to 2
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tADH
tCA
RD
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
AD0 to 15
A0 to 15
D0 to 15
tAL
tLA
tCL
ALE
tLL

(2) Write Cycle



4.4 AD Conversion Characteristics (Vss = 0 V, AVcc = Vcc, AVss = Vss, Ta = –40 to 85°C)

Vcc = +5V ± 10%, (fc = 4 to 25 MHz)
Vcc = +3V ± 10%, (fc = 4 to 12.5 MHz)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
AD analog reference supply voltage (+)		V_{REFH}		Vcc – 0.2		Vcc	V
AD analog reference supply voltage (–)		V_{REFL}		Vss		Vss + 0.2	
Analog reference voltage		AV_{CC}		Vcc – 0.2		Vcc	
Analog reference voltage		AV_{SS}		Vss		Vss + 0.2	
Analog input voltage		V_{AIN}		V_{REFL}		V_{REFH}	
Analog input impedance		R_{AIN}				5	kΩ
Analog reference voltage supply current	<VREFON> = 1	I_{REF}	Vcc = 5 V ± 10%			3.7	mA
			Vcc = 3 V ± 10%			2.2	
	<VREFON> = 0		Vcc = 2.7 to 5.5 V		0.02	5.0	μA
Total tolerance (excludes quantization error)		E_T	Vcc = 5 V ± 10%			±3	LSB
			Vcc = 3 V ± 10%			±3	

Note 1: 1LSB = (VREFH -VREFL)/2^{10} [V]

Note 2: Power supply current ICC from the VCC pin includes the power supply current from the AVCC pin.

4.5 Serial Channel Timing (Serial channel 2, 3 and 4)

(1) SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	16X		488 μs		1.28 μs		0.8 μs	
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		91.5 μs		190 ns		100 ns	
SCLK edge* → Output Data hold	t_{OHS}	5X – 100		152 μs		300 ns		150 ns	
SCLK edge* → Input Data hold	t_{HSR}	0		0		0		0	
SCLK edge* → effective data input	t_{SRD}		t_{SCY} – 5X – 100		336 μs		780 ns		450 ns

* It is rising edge in using rising edge mode and falling edge in using falling edge mode.

(2) SCLK Output Mode

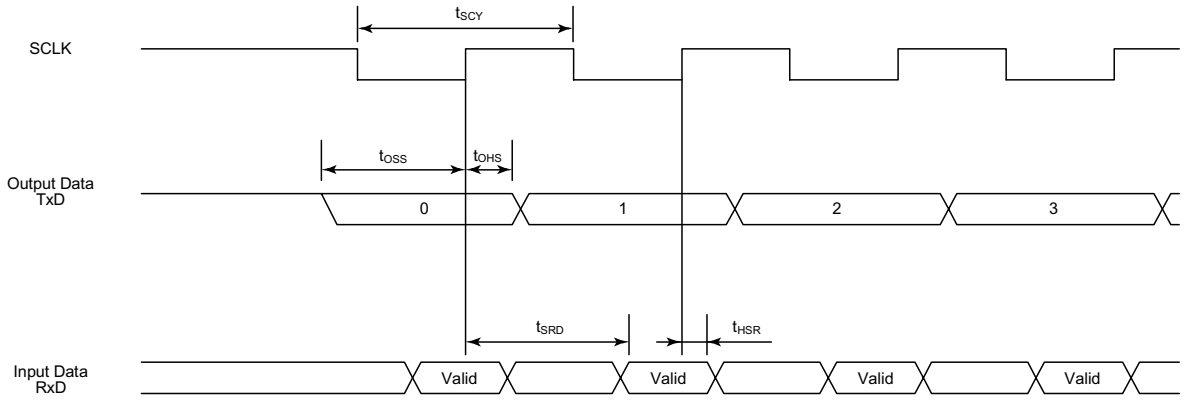
Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28 μs	655.36 μs	0.8 μs	409.6 μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2X – 150		427 μs		970 ns		550 ns	
SCLK rising edge → Output Data hold	t_{OHS}	2X – 80		60 μs		80 ns		20 ns	
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		0	
SCLK rising edge → effective data input	t_{SRD}		t_{SCY} – 2X – 150		428 μs		970 ns		550 ns

(3) SCLK Input Mode (UART mode)

Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t_{SCY}	SCLK cycle	4X + 20		122 μs		340 ns		220 ns	
t_{SCYL}	Low level SCLK Pulse width	2X + 5		6 μs		165 ns		105 ns	
t_{SCYH}	High level SCLK Pulse width	2X + 5		6 μs		165 ns		105 ns	

Note: fs is used as system clock or input clock to prescaler.

Timing Chart for I/O Interface Mode



Note: SCLK is reversed in SCLK input falling mode.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low level pulse width	t_{VCKL}	4X + 40		360		240		ns
High level pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level pulse width	t_{INTAL}	4X		320		200		ns
$\overline{NMI}$, INT0 High level pulse width	t_{INTAH}	4X		320		200		ns

(2) INT4 to 7

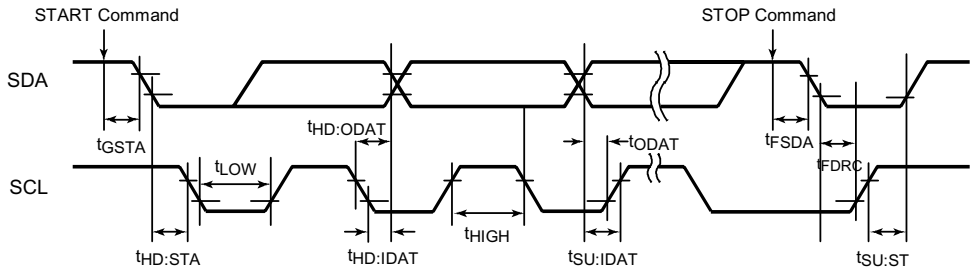
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT4 to INT7 Low level pulse width	t_{INTBL}	4X + 100		420		300		ns
INT4 to INT7 High level pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 Serial Bus Interface Timing

(1) I^2C bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ	Max	
START command → SDA fall	t_{GSTA}	3X			s
Hold time START condition	$t_{HD: STA}$	2^nX			s
SCL Low level pulse width	t_{LOW}	2^nX			s
SCL High level pulse width	t_{HIGH}	2^nX + 8X			s
Data hold time (input)	$t_{HD: IDAT}$	0			ns
Data set-up time (input)	$t_{SU: IDAT}$	250			ns
Data hold time (output)	$t_{HD: ODAT}$	7X		11X	s
Data output → SCL Rising edge	t_{ODAT}		2^nX – $t_{HD: ODAT}$		s
STOP command → SDA falling edge	t_{FSDA}	3X			s
SDA Falling edge → SCL Rising edge	t_{FDRC}	2^nX			s
Set-up time STOP condition	$t_{SU: STO}$	2^nX + 16X			s

Note: n value is set by SBICR1 <SCK2 to 0>



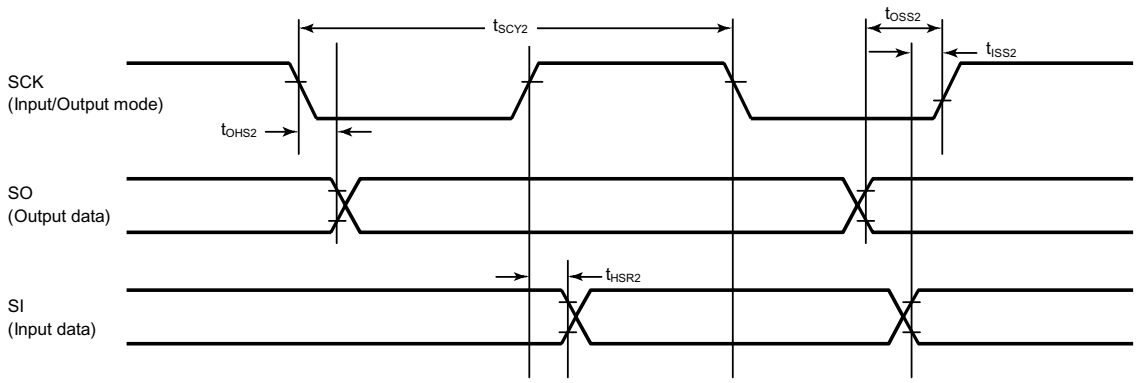
(2) Clocked-synchronous 8-bit SIO Mode

a. SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling edge → Output data hold	t_{OHS2}	6X		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 6X$	s
SCK rising edge → Input data hold	t_{HSR2}	6X		ns
Input data → SCK rising edge	t_{ISS2}	0		ns

b. SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling edge → Output data hold	t_{OHS2}	2X		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 2X$	s
SCK rising edge → Input data hold	t_{HSR2}	2X		s
Input data → SCK rising edge	t_{ISS2}	0		ns



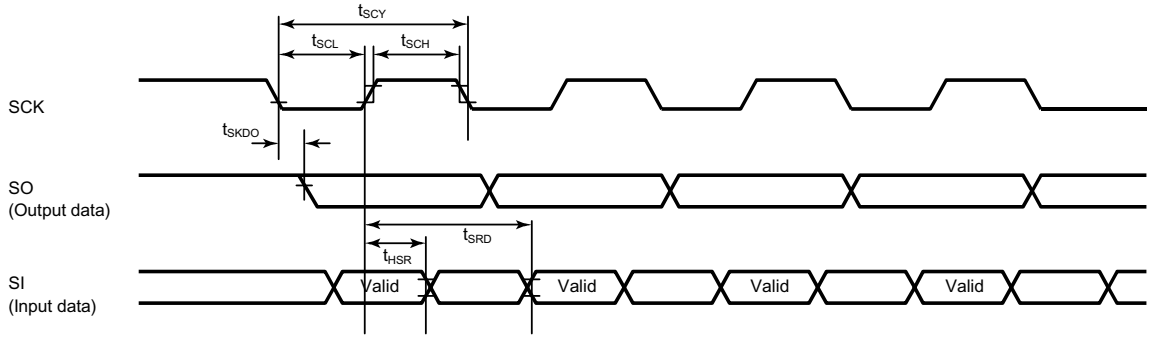
4.9 Timing Chart for Sirial Channel 0,1

a. SCK input mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	6X		ns
SCK rising edge → Effective data input	t_{SRD}		t_{SCY} – 2X	ns
SCK rising edge → Input data hold	t_{HSR}	6X		ns

b. SCK output mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	2X		ns
SCK rising edge → Effective data input	t_{SRD}		t_{SCY} – 2X	ns
SCK rising edge → Input data hold	t_{HSR}	2X		ns

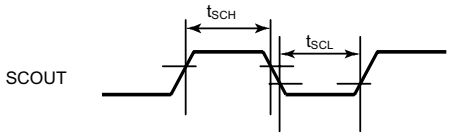


4.10 SCOUT pin AC characteristics

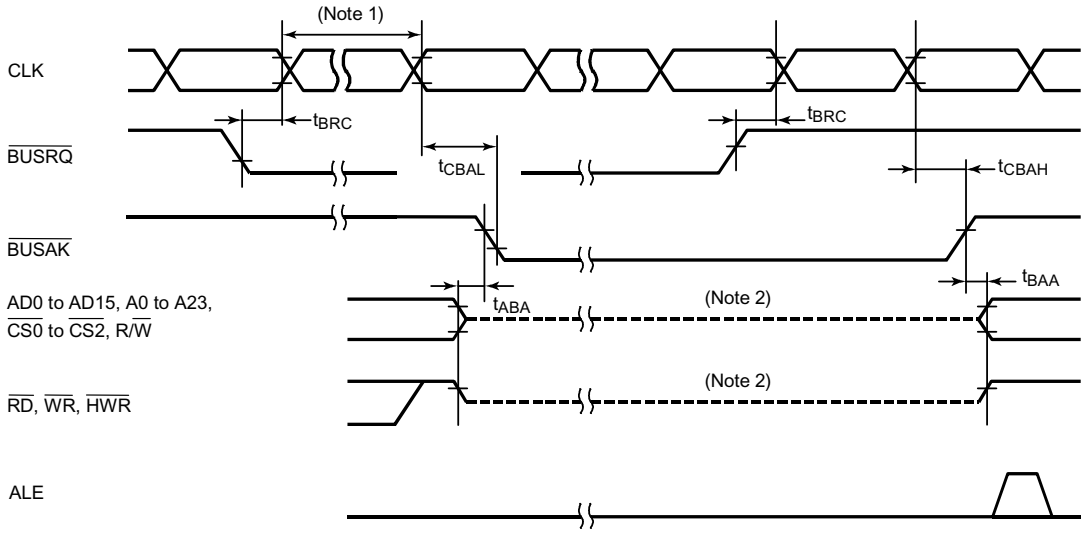
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
High-level pulse width VCC = 5 V ± 10%	t_{SCH}	0.5X – 10		30		15		ns
VCC = 3 V ± 10%		0.5X – 20		20		—		ns
Low-level pulse width VCC = 5 V ± 10%	t_{SCL}	0.5X – 10		30		15		ns
VCC = 3 V ± 10%		0.5X – 20		20		—		ns

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.11 Timing Chart for Bus Request ($\overline{BUSRQ}$)/Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time to CLK	t_{BRC}	120		120		120		ns
CLK → $\overline{BUSAK}$ falling edge	t_{CBAL}		1.5X + 120		240		195	ns
CLK → $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5X + 40		80		65	ns
Output Buffer is off to $\overline{BUSAK}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↑ to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1: The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to 0 during Wait cycle.

Note 2: This line shows the output buffer is off-state. It doen't indicate the signal level is fixed. Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level - fix will be delayed.

The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.