

# Octal D-type transparent latch; 3-state

## KK74LV373

The KK74LV373 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT373.

The KK74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all internal latches.

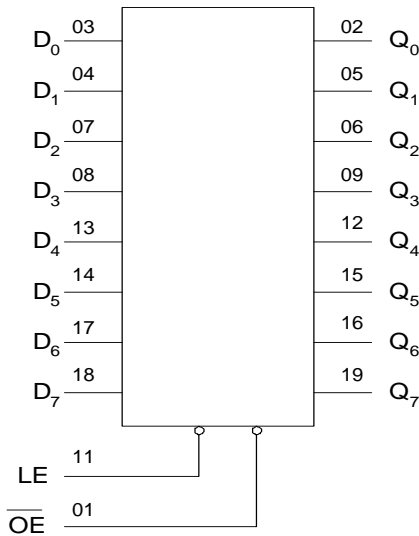
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX PLASTIC

DW SUFFIX SOIC

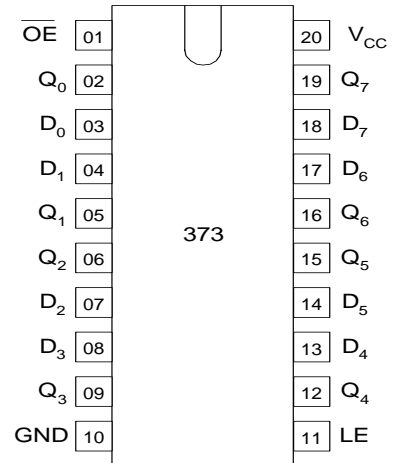
**ORDERING INFORMATION**  
 KK74LV373N Plastic  
 KK74LV373DW SOIC  
 $T_A = -40^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 20= $V_{CC}$   
 PIN 10 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
OE	LE	Dn	Qn
L	H	H	H
L	H	L	L
L	L	X	Qo
H	X	X	Z

X = Don't care  
 Z = High impedance OFF-state  
 L = Low voltage level  
 H= HIGH voltage level

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage	-0.5 to +5.0	V
I <sub>IK</sub> * <sup>1</sup>	DC input diode current	±20	mA
I <sub>OK</sub> * <sup>2</sup>	DC output diode current	±50	mA
I <sub>O</sub> * <sup>3</sup>	DC output source or sink current -bus driver outputs	±35	mA
I <sub>GND</sub>	DC V <sub>CC</sub> or GND current for types with - bus driver outputs	±70	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND current for types with - bus driver outputs	±70	mA
P <sub>D</sub>	Power dissipation per package, plastic DIP+ SOIC package+	750 500	mW
T <sub>stg</sub>	Storage temperature	-65 to +150	°C
T <sub>L</sub>	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP ), 0.3 mm (SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SOIC Package: - 8 mW/°C from 70° to 125°C

\*1: V<sub>I</sub> < -0.5 or V<sub>I</sub> > V<sub>CC</sub>+0.5V

\*2: V<sub>O</sub> < -0.5 or V<sub>O</sub> > V<sub>CC</sub>+0.5V

\*3: -0.5V < V<sub>O</sub> < V<sub>CC</sub>+0.5V

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	1.2	3.6	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> =1.2 V	0	1000	ns
	V <sub>CC</sub> =2.0 V	0	700	
	V <sub>CC</sub> =3.0 V	0	500	
	V <sub>CC</sub> =3.6 V		400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**

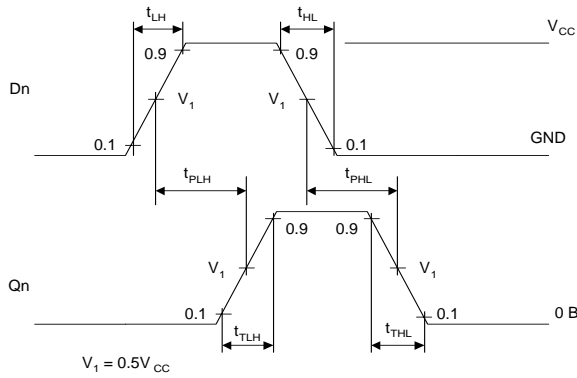
Symbol	Parameter	Test Conditions	V <sub>CC</sub> , B	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		-40°C to 125°C		
				min	max	min	max	min	max	
V <sub>IH</sub>	HIGH level input voltage	V <sub>O</sub> = V <sub>CC</sub> -0.1 B	1.2	0.9	-	0.9	-	0.9	-	B
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V <sub>IL</sub>	LOW level input voltage	V <sub>O</sub> = 0.1 B	1.2	-	0.3	-	0.3	-	0.3	B
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 mA	1.2	1.1	-	1.0	-	1.0	-	B
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
V <sub>OH</sub>	HIGH level output voltage; bus driver outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -8.0 mA	3.0	2.48	-	2.34	-	2.20	-	B
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 mA	1.2	-	0.09	-	0.1	-	0.1	B
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.1	-	0.1	
V <sub>OL</sub>	LOW-level output voltage; bus driver outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 8.0 mA	3.0	-	0.33	-	0.4	-	0.5	B
I <sub>IN</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6	-	±0.1	-	±1.0	-	±1.0	mA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	1.2 3.6	-	±0.5	-	±5	-	±10	mA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>I</sub> = V <sub>CC</sub> or 0 B I <sub>O</sub> = 0 mA	3.6	-	8.0	-	80	-	160	mA

**AC ELECTRICAL CHARACTERISTICS ( $C_L=50$  пФ,  $t_{LH} = t_{HL} = 6.0$  нс,  $V_{IL}=0B$ ,  $V_{IH}=V_{CC}$ )**

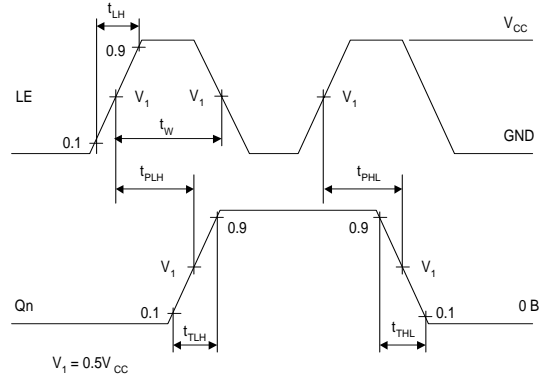
Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit						Unit
			25°C		-40°C to 85°C		-40°C to 125°C		
			min	max	min	max	min	max	
t <sub>PHL</sub> , t <sub>PLH</sub> от Dn к Qn	Propagation delay Dn to Qn	1.2	-	150	-	190	-	220	ns
		2.0	-	38	-	48	-	58	
		3.0	-	23	-	29	-	35	
t <sub>PHL</sub> , t <sub>PLH</sub> от LE к Qn	Propagation delay LE to Qn	1.2	-	180	-	230	-	270	
		2.0	-	45	-	56	-	68	
		3.0	-	27	-	34	-	41	
t <sub>PHZ</sub> , t <sub>PLZ</sub> от OE к Qn	3-state output enable time OE to Qn	1.2	-	160	-	200	-	240	
		2.0	-	35	-	43	-	45	
		3.0	-	23	-	28	-	32	
t <sub>PZH</sub> , t <sub>PZL</sub> от OE к Qn	3-state output disable time OE to Qn	1.2	-	160	-	200	-	240	
		2.0	-	40	-	50	-	60	
		3.0	-	24	-	30	-	36	
t <sub>THL</sub> , t <sub>TLH</sub>	Output transition time	1.2	-	75	-	100	-	120	
		2.0	-	16	-	20	-	24	
		3.0	-	10	-	13	-	15	
t <sub>w</sub>	LE pulse width HING	1.2	250	-	350	-	450	-	
		2.0	30	-	34	-	41	-	
		3.0	18	-	24	-	24	-	
t <sub>SU</sub>	Hold time Dn to LE	1.2	45	-	50	-	100	-	
		2.0	15	-	17	-	15	-	
		3.0	9	-	10	-	12	-	
t <sub>H</sub>	Hold time Dn to LE	1.2	25	-	25	-	25	-	
		2.0	5	-	5	-	5	-	
		3.0	5	-	5	-	5	-	
C <sub>I</sub>	Input capacitance	3.0	-	7.0	-	7.0	-	7.0	pF

C <sub>PD</sub>	Power dissipation capacitance per latch	Typical @25°C, V <sub>CC</sub> =3.0 V						pF
		80						

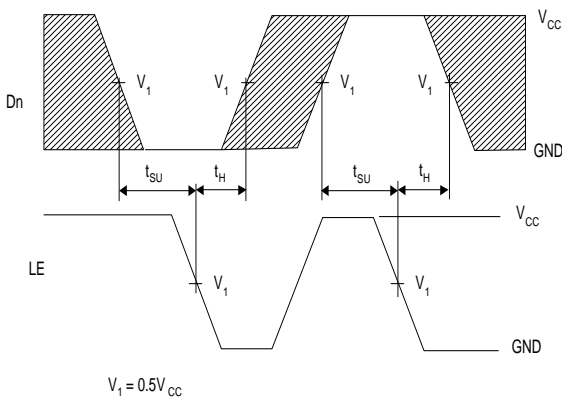
Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_0)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_0$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L V_{CC}^2 f_0)$  = sum of outputs.



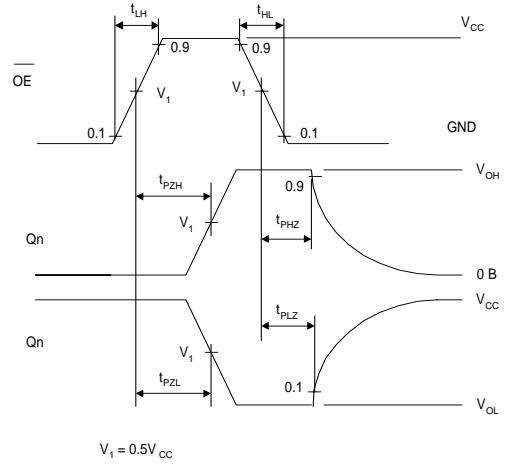
**Figure 1. Switching Waveforms**



**Figure 2. Switching Waveforms**

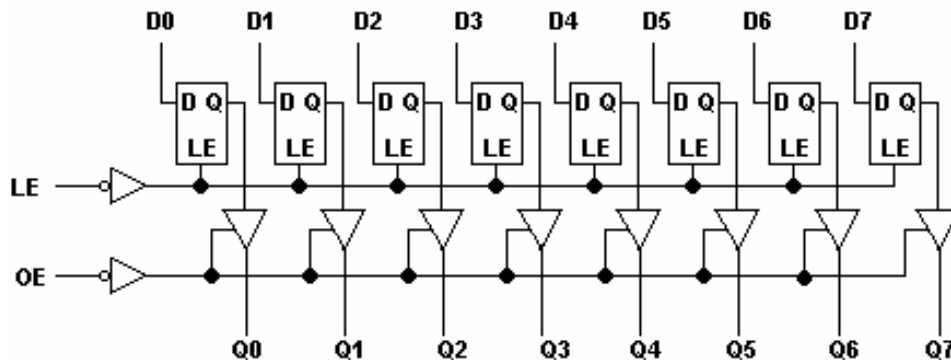


**Figure 3. Switching Waveforms**

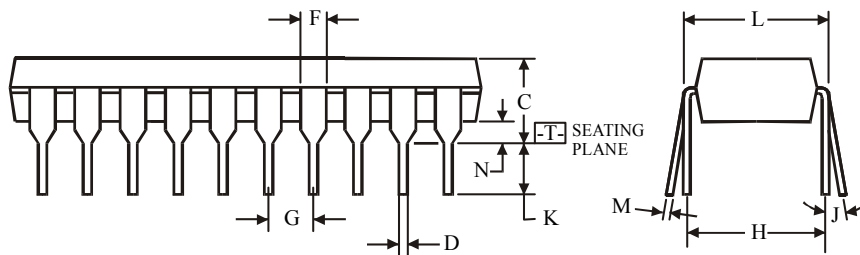
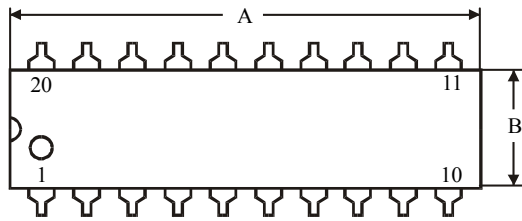
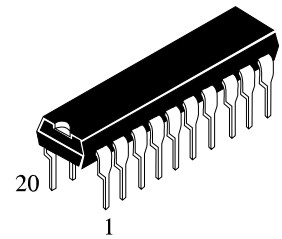


**Figure 4. Switching Waveforms**

**EXPANDED LOGIC DIAGRAM**



### N SUFFIX PLASTIC DIP (MS - 001AD)



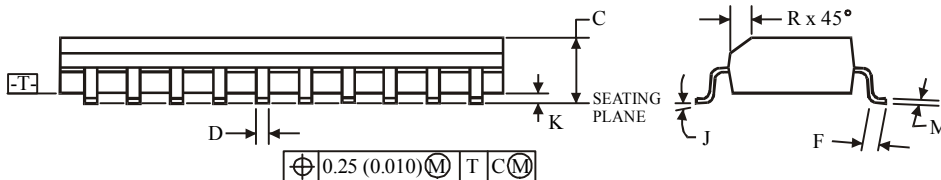
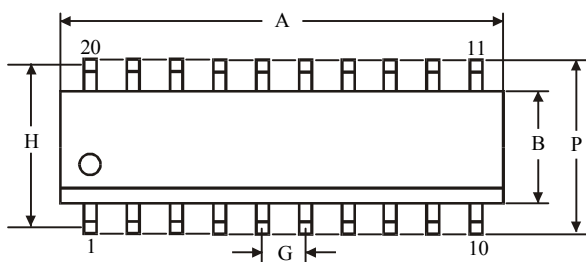
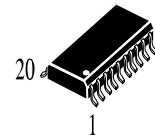
$\oplus 0.25 (0.010) \text{M} \text{T}$

#### NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

### D SUFFIX SOIC (MS - 013AC)



$\oplus 0.25 (0.010) \text{M} \text{T} \text{C} \text{M}$

#### NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75