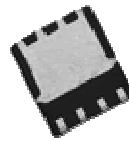


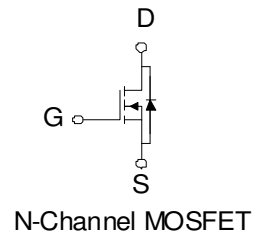
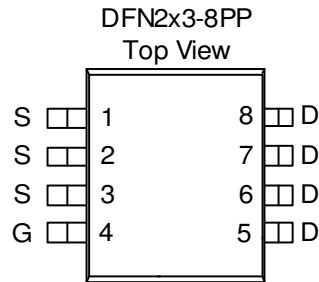
N-Channel 80-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2x3-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
80	82 @ $V_{GS} = 10V$	± 5.4
	115 @ $V_{GS} = 4.5V$	± 4.6



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	± 5.4	A
	$T_A = 70^\circ\text{C}$		± 4.4	
Pulsed Drain Current ^b		I_{DM}	± 25	
Continuous Source Current (Diode Conduction) ^a		I_S	2	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.5	W
	$T_A = 70^\circ\text{C}$		2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	35	$^\circ\text{C/W}$
	Steady State		81	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	uA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55°C			10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.6 A			86	mΩ
		V _{GS} = 4.5 V, I _D = 3.9 A			115	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 4.6 A		11		S
Diode Forward Voltage	V _{SD}	I _S = 2.0 A, V _{GS} = 0 V		1.1		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 4.6 A		3.6		nC
Gate-Source Charge	Q _{gs}			1.8		
Gate-Drain Charge	Q _{gd}			1.3		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω , I _D = 1 A, V _{GEN} = 10 V		9		nS
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(off)}			21		
Fall-Time	t _f			8		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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