ARIZONA MICROTEK, INC.

AZP81

PECL/ECL Filter-Based Multiplier & Limiting Amp with Selectable Enable

FEATURES

- High Bandwidth for 1+GHz
- 3.0V to 5.5V Power Supply
- Selectable Enable Polarity
- Designed for Filters to Select Odd or Even Harmonics
- S-Parameter (.s1p and .s2p) Files Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 16 (3x3) Green / RoHS Compliant / Lead (Pb) Free	AZP81LG	AZMG P81 <Date Code>	1,2

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZP81 is a specialized multiplier chip designed to be used with an external filter. It supplies three different gain paths. A low gain path is used with a resonator, usually a crystal (D/$\overline{D}$ to $\overline{Q}$). An intermediate gain path with fast output edges supplies a filter (D/$\overline{D}$ to FLTRDR/$\overline{FLTRDR}$). A high gain limiting amp (AMPIN to Q_{HG}/$\overline{Q}_{HG}$) with a selectable enable provides industry standard 100k PECL/ECL outputs.

When Q_{HG}/$\overline{Q}_{HG}$ are disabled, the AZP81's oscillator loop continues to operate. See truth table below for enable function. It also provides a V_{BB} and 470Ω internal bias resistors from D/$\overline{D}$ to V_{BB} and AMPIN to V_{BB}. The V_{BB} pin can support 1.5mA sink/source current. Bypassing V_{BB} and $\overline{D}$ to ground with 0.01 to 0.1 µF capacitors is recommended.

Output $\overline{Q}$ has an on-chip 4mA pull-down current source while output FLTRDR has an on-chip 8mA pull-down current source. External resistors to V_{EE} may also be used to increase pull-down current to a maximum of 25mA each.

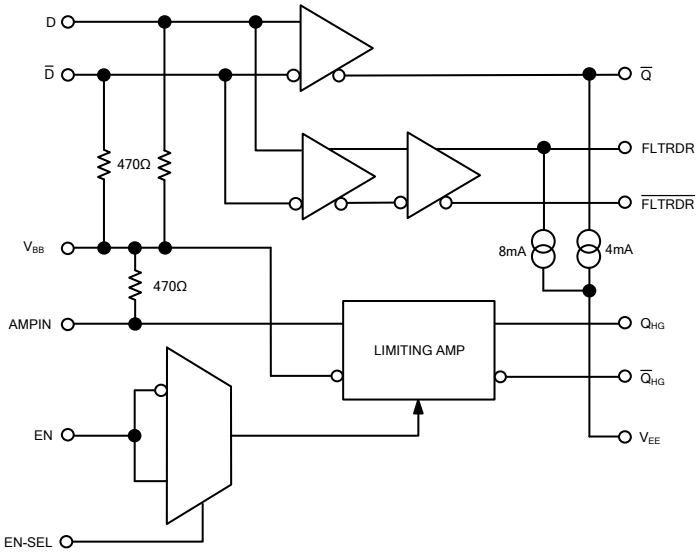
ENABLE TRUTH TABLE

EN-SEL	EN (PECL/CMOS)	Q_{HG}	$\overline{Q}_{HG}$
NC	Low	Low	High
NC	High or NC	Data	Data
V_{EE}*	Low or NC	Data	Data
V_{EE}*	High	Low	High

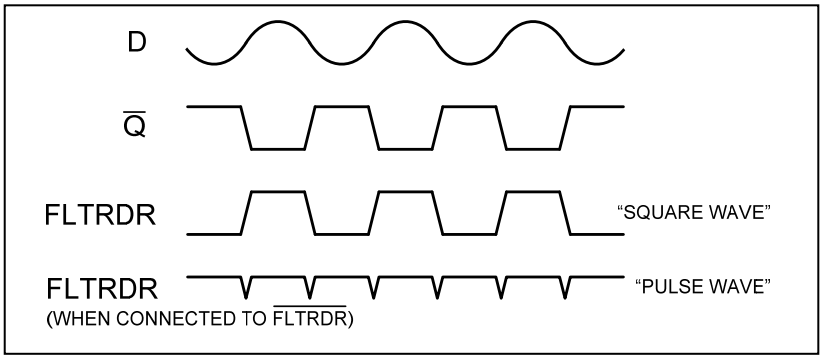
*Connections to V_{EE} must be less than 1Ω.

PIN DESCRIPTION

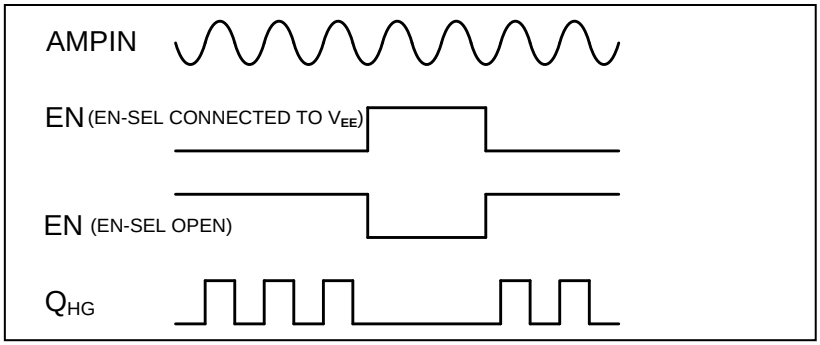
PIN	FUNCTION
D/$\overline{D}$	Inputs from Resonator
$\overline{Q}$	Output to Resonator
AMPIN	Inputs from Filter
FLTRDR/$\overline{FLTRDR}$	Outputs to Filter
Q_{HG}/$\overline{Q}_{HG}$	Outputs w/High Gain
V_{BB}	Ref. Voltage Output
EN	Enable Input
EN-SEL	Selects Enable Logic



TIMING DIAGRAMS

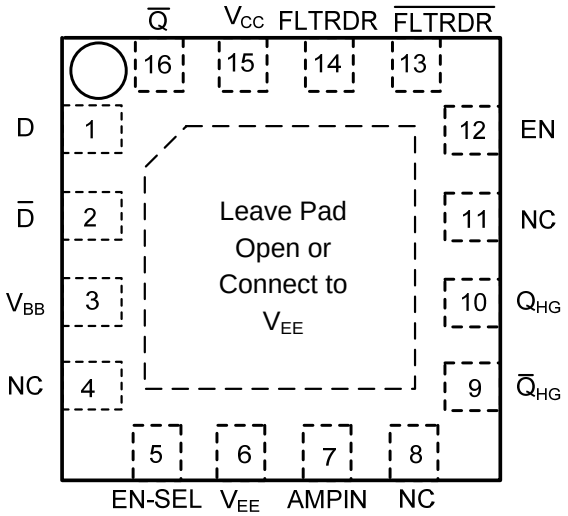


D to $\overline{Q}$/FLTRDR



AMPIN to Q_{HG}

AZP81L PINOUT



TOP VIEW

Absolute Maximum Ratings. Beyond which device life may be impaired.

Characteristic	Symbol	Rating	Unit
PECL Power Supply (V_{EE} = 0V)	V_{EE}	0 to 6.0	V_{DC}
PECL Input Voltage (V_{EE} = 0V)	V_I	±0.75 with respect to V_{BB}	V_{DC}
PECL EN Input Voltage (V_{EE} = 0V)	V_I	0 to 6.0	V_{DC}
ECL Power Supply (V_{CC} = 0V)	V_{EE}	-6.0 to 0	V_{DC}
ECL Input Voltage (V_{CC} = 0V)	V_I	±0.75 with respect to V_{BB}	V_{DC}
ECL EN Input Voltage (V_{EE} = 0V)	V_I	-6.0 to 0	V_{DC}
Output Current --- Continuous $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$ --- Surge	I_{OUT}	25 50	mA
Output Current --- Continuous $Q_{HG}/\overline{Q}_{HG}$ --- Surge	I_{OUT}	50 100	mA
Operating Temperature Range	T_A	-40 to +85	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	-1045	-895	-1005	-855	-980	-830	-910	-760	mV
V_{OL}	Output LOW Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	-2010	-1710	-1985	-1685	-1965	-1665	-1910	-1610	mV
V_{OH}	Output HIGH Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	-1830	-1555	-1810	-1620	-1810	-1620	-1810	-1620	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$ EN	 -1165 -1165	 -390 V_{CC}	 -1165 -1165	 -390 V_{CC}	 -1165 -1165	 -390 V_{CC}	 -1165 -1165	 -390 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$ EN	 -2250 V_{EE}	 -1475 -1475	 -2250 V_{EE}	 -1475 -1475	 -2250 V_{EE}	 -1475 -1475	 -2250 V_{EE}	 -1475 -1475	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IL}	Input LOW Current EN (ECL) EN (CMOS)	 -150 -300		 -150 -300		 -150 -300		 -150 -300		µA
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{EE}	Power Supply Current		63		63		63		68	mA

1. Specified with each output terminated through a 50Ω resistor to V_{CC} – 2V.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	2255	2405	2295	2445	2320	2470	2390	2540	mV
V_{OL}	Output LOW Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	1290	1590	1315	1615	1335	1635	1390	1690	mV
V_{OH}	Output HIGH Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	1470	1745	1490	1680	1490	1680	1490	1680	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$ EN	 2135 2135	 2910 V_{CC}	 2135 2135	 2910 V_{CC}	 2135 2135	 2910 V_{CC}	 2135 2135	 2910 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$ EN	 1050 V_{EE}	 1825 1825	 1050 V_{EE}	 1050 V_{EE}	 1825 1825	 1050 V_{EE}	 1825 1825	 -1475 -1475	mV
V_{BB}	Reference Voltage	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IL}	Input LOW Current EN (ECL) EN (CMOS)	 -150 -300		 -150 -300		 -150 -300		 -150 -300		µA
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{EE}	Power Supply Current[1]		63		63		63		68	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with each output terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	3955	4105	3995	4145	4020	4170	4090	4240	mV
V_{OL}	Output LOW Voltage $\overline{Q}$, FLTRDR/$\overline{FLTRDR}$	2990	3290	3015	3315	3035	3335	3090	3390	mV
V_{OH}	Output HIGH Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1] $Q_{HG}/\overline{Q}_{HG}$	1470	1745	1490	1680	1490	1680	1490	1680	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$ EN	3835 3835	4610 V_{CC}	3835 3835	4610 V_{CC}	3835 3835	4610 V_{CC}	3835 3835	4610 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$ EN	2750 V_{EE}	3525 3525	2750 V_{EE}	3525 3525	2750 V_{EE}	3525 3525	2750 V_{EE}	3525 3525	mV
V_{BB}	Reference Voltage	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IL}	Input LOW Current EN (ECL) EN (CMOS)	-150 -300		-150 -300		-150 -300		-150 -300		µA
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{EE}	Power Supply Current[1]		63		63		63		68	mA

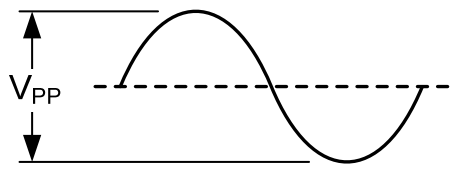
1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with each output terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{CC} = 3.0V to 5.5V, V_{EE} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D/$\overline{D}$ to $\overline{Q}$ D/$\overline{D}$ to FLTRDR/$\overline{FLTRDR}$[2] AMPIN to $Q_{HG}/\overline{Q}_{HG}$[1] (SE)	90 130 200		200 260 380	90 130 200		200 260 380	90 130 200		200 260 380	90 130 200		200 260 380	ps
t_{SKEW}	Duty Cycle Skew[3] (SE)		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing (SE)[4] D/$\overline{D}$ AMPIN	300 150		2000 2000	300 150		2000 2000	300 150		2000 2000	300 150		2000 2000	mV
t_r / t_f	Output Rise/Fall Times (20% - 80%)	80		240	80		240	80		240	80		240	ps
x_{MAX}	Maximum Recommended Multiply Ratio Even Harmonics Odd Harmonics			8 7			8 7			8 7			8 7	

1. Specified with $Q_{HG}/\overline{Q}_{HG}$ terminated through a 50Ω resistor to V_{CC} – 2V.
2. Specified with FLTRDR terminated into an AC coupled 50Ω load, $\overline{FLTRDR}$ into an AC coupled 50Ω load along an external 8mA pull-down current.
3. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
4. Single ended input swing for which AC parameters guaranteed.

SINGLE ENDED AC PP INPUT



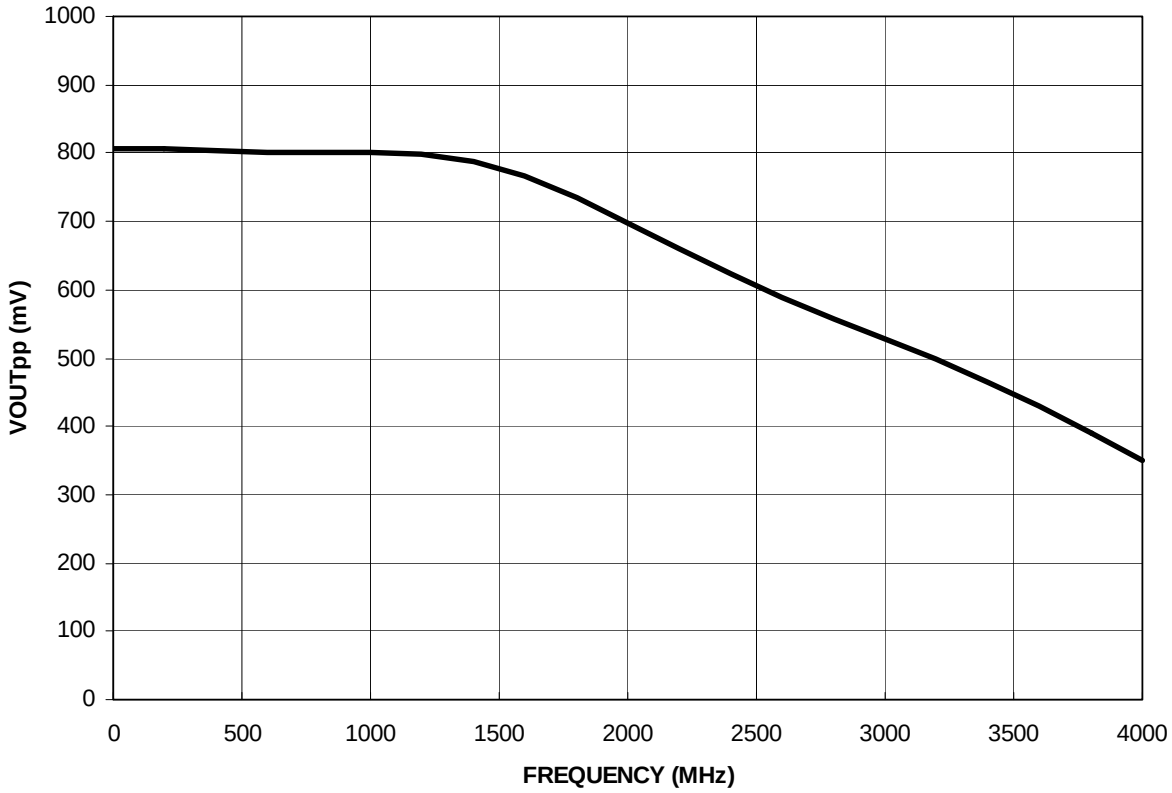


Fig 1: Typical Large Signal Outputs, $Q_{HG}/\overline{Q}_{HG}$

Measured with 750mV$_{PP}$ on AMPIN, $Q_{HG}/\overline{Q}_{HG}$ each terminated to V_{CC}-2V via 50 Ω resistors.

APPLICATION

The AZP81 is a "filter-based" oscillator gain stage and multiplier. Generating a spectrum of harmonics from a sine-wave input, an external bandpass filter selects the desired harmonic.

A crystal or SAW (with associated passive discrete components) is connected between D and $\overline{Q}$ (pins 1 and 16, respectively) to form an high stability oscillator stage. Alternatively, an external Colpitts, Pierce or similar sine-wave oscillator may be fed into D (pin 1) to drive the AZP81. In this case, input amplitude should be less than 1 V_{PP} on D for best results. Also, tie the $\overline{Q}$ pin to V_{CC} to reduce fundamental subharmonic and other noise source coupling into the circuit board.

The D input also drives another higher gain stage. This stage generates fast edges with resultant high harmonic spectral content. In one mode, the signal on FLTRDR (pin 14) is a square wave with greater spectral energy at odd harmonics (3x, 5x, 7x). Figure 4 illustrates the typical spectral output at FLTRDR. Another mode is selected by connecting $\overline{\text{FLTRDR}}$ and FLTRDR. This mode generates a pulse wave which contains greater spectral energy at even harmonics (2x, 4x, 6x, 8x). Figure 5 illustrates the typical spectral output at FLTRDR when the two pins are shorted together.

An external bandpass filter inserted between FLTRDR (or FLTRDR/$\overline{\text{FLTRDR}}$) and AMPIN (pin 7) selects the desired harmonic and attenuates the rest. This filter is typically either an LC or SAW implementation. The bandpass filter is AC coupled since both the FLTDR and AMPIN signals are internally biased. The filter must be designed for the drive impedance found at FLTRDR and the input impedance at AMPIN.

Graphs that follow in this data sheet show the S-parameters for these pins. Also included are graphs of the output impedance magnitude of FLTRDR and the input impedance magnitude of AMPIN. These impedance graphs provide a way to approximate the filter required without the use of S-parameter based design software.

The filter and other elements on the circuit board must be placed carefully to minimize subharmonic feed-through. The resultant signal level at AMPIN should be 150 mV peak-peak or greater for best limiting amplifier performance.

The limiting amplifier provides a high bandwidth PECL/ECL output into the standard load of 50Ω to V_{CC} – 2V. Figure 1 shows the large signal output swing versus frequency.

It may be desirable to hold off the limiting amplifier operation until the sine-wave oscillator has started. A capacitor may be used with the EN pin to create a delay. Connect the capacitor from EN to V_{CC} (if EN-SEL is open) or V_{EE} (if EN-SEL is connected to V_{EE}). This modification will avoid high-frequency parasitic feedback from the circuit board during oscillator startup. A 220ρF capacitor will provide approximately 10μs delay.

Arizona Microtek's website (www.azmicrotek.com) contains S-parameters for all signal paths in industry-standard .s1p and .s2p format supporting an easier RF design process.

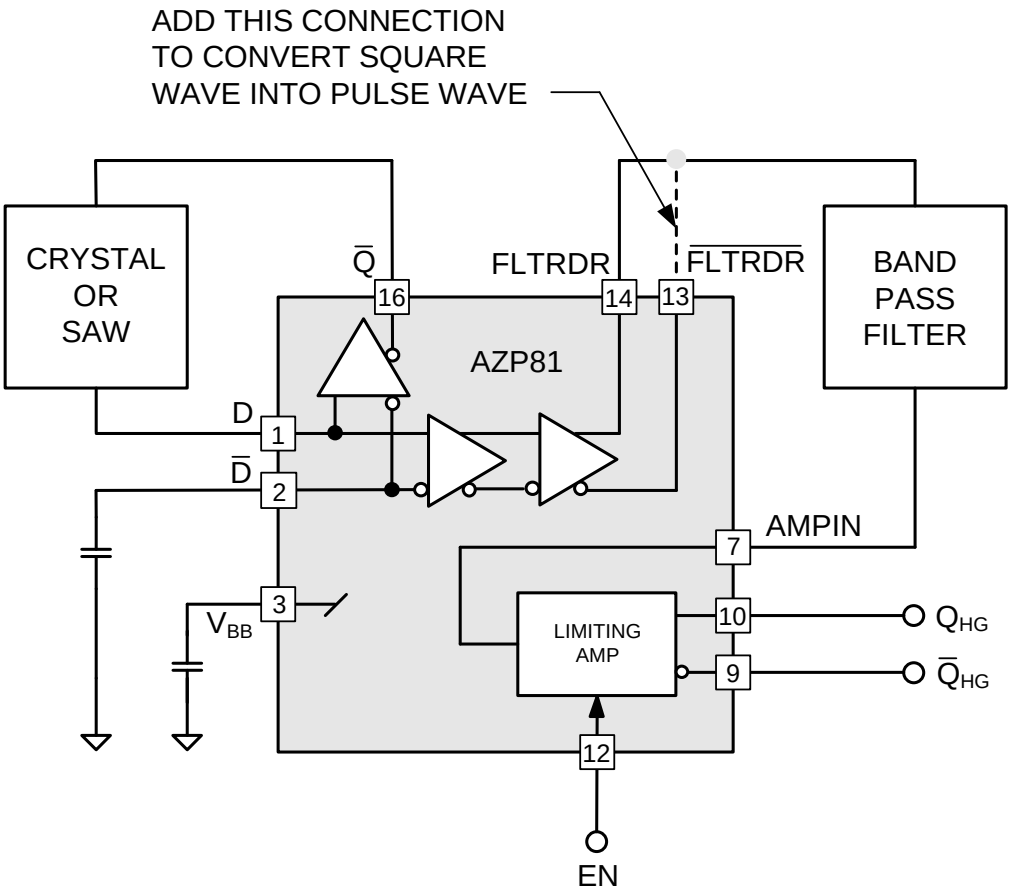


Fig 2: Typical Multiplier Application
(Simplified Logic Shown)

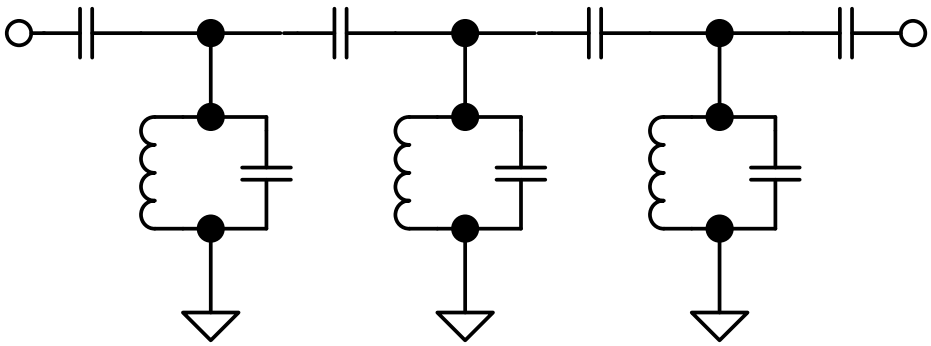


Fig 3: Typical LC Band Pass Filter

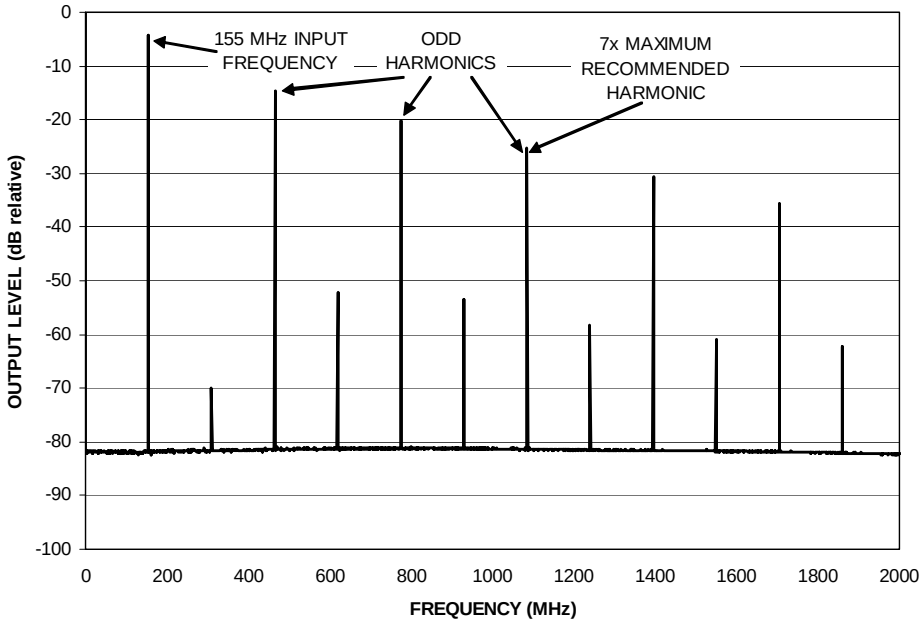


Fig 4: Typical Spectrum Output of FLTRDR (Square wave)
Full Limiting 155 MHz Input Signal

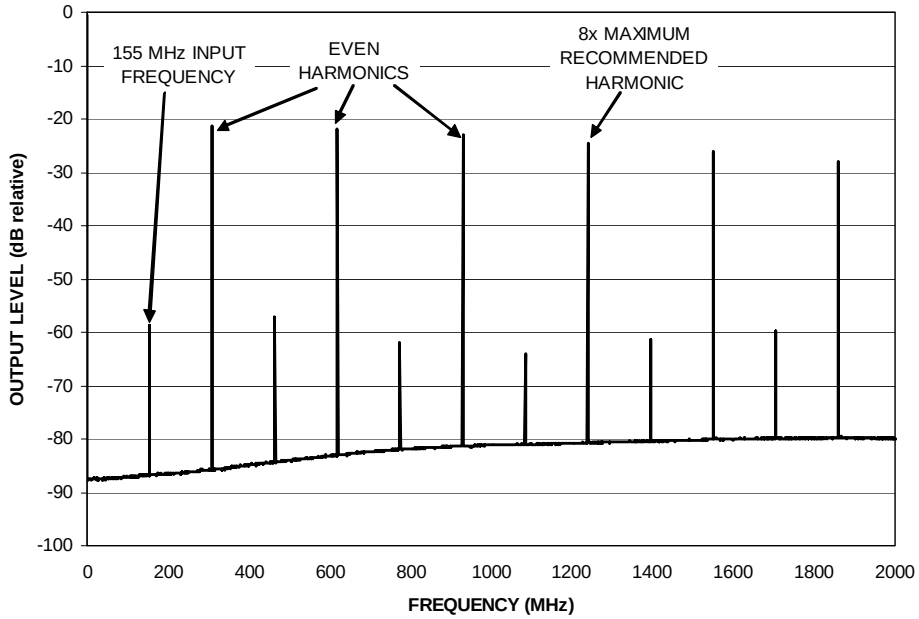


Fig 5: Typical Spectrum Output of FLTRDR (Pulse wave)
Full Limiting 155 MHz Input Signal

S-PARAMETERS

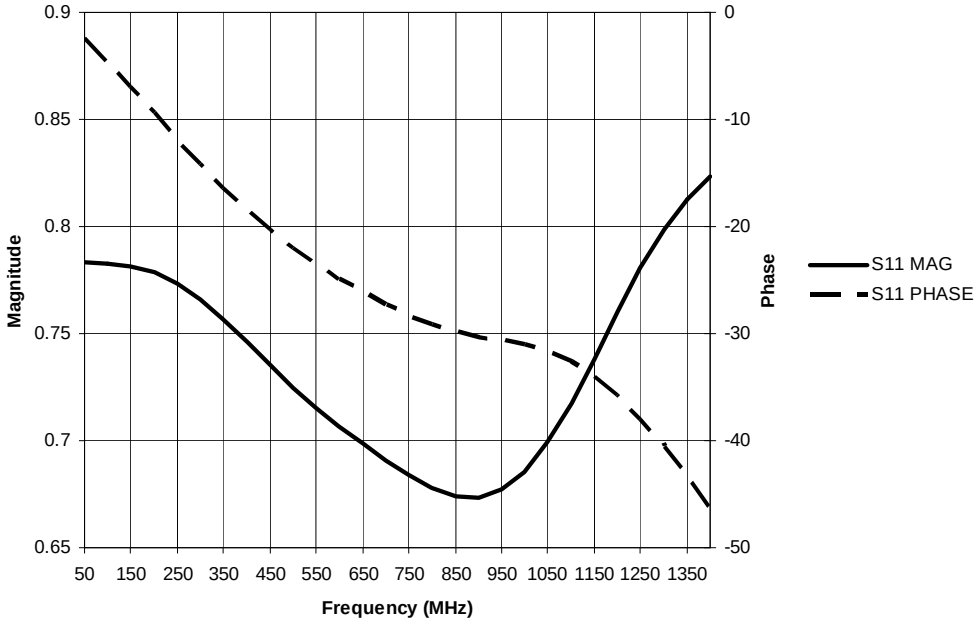


Fig 6: S11, D to $\bar{Q}$

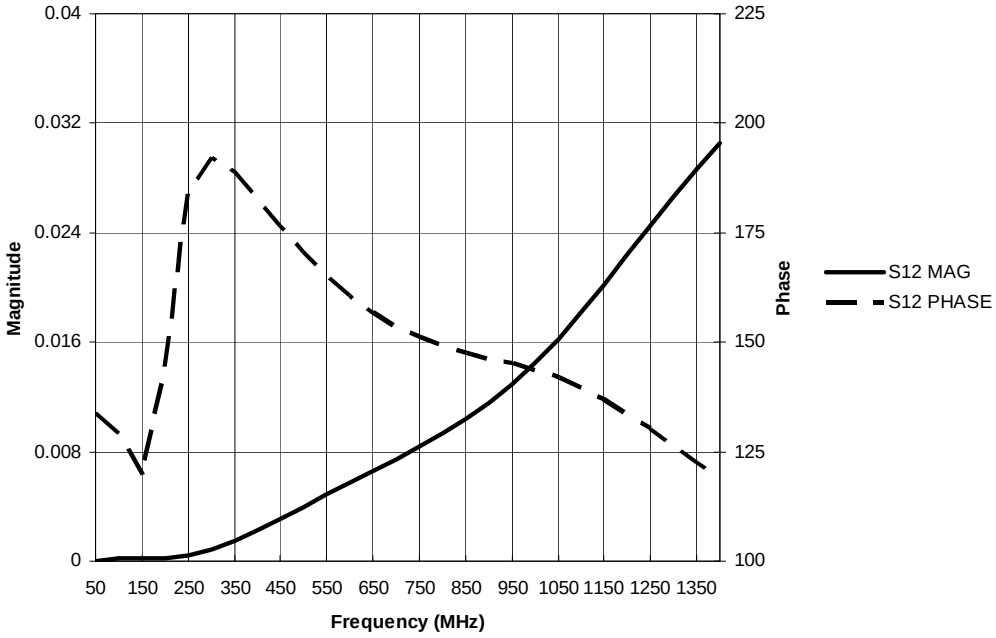


Fig 7: S12, D to $\bar{Q}$

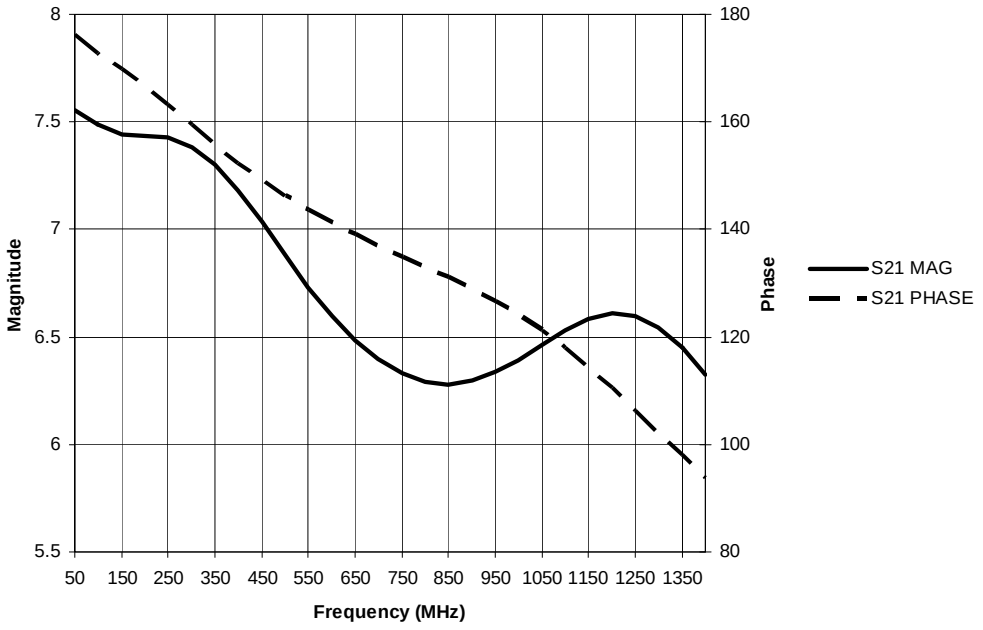


Fig 8: S21, D to $\bar{Q}$

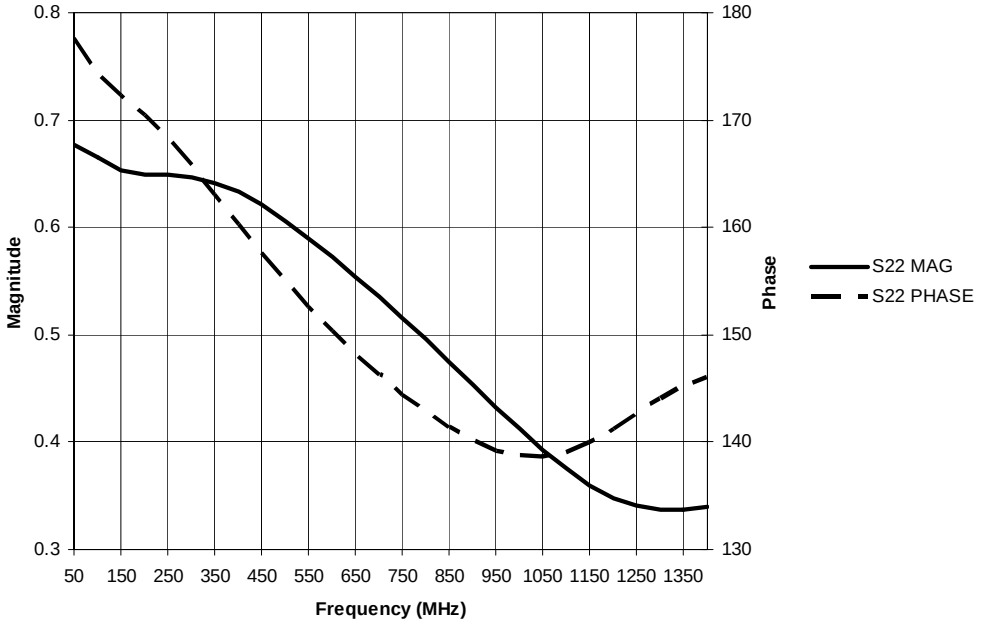


Fig 9: S22, D to $\bar{Q}$

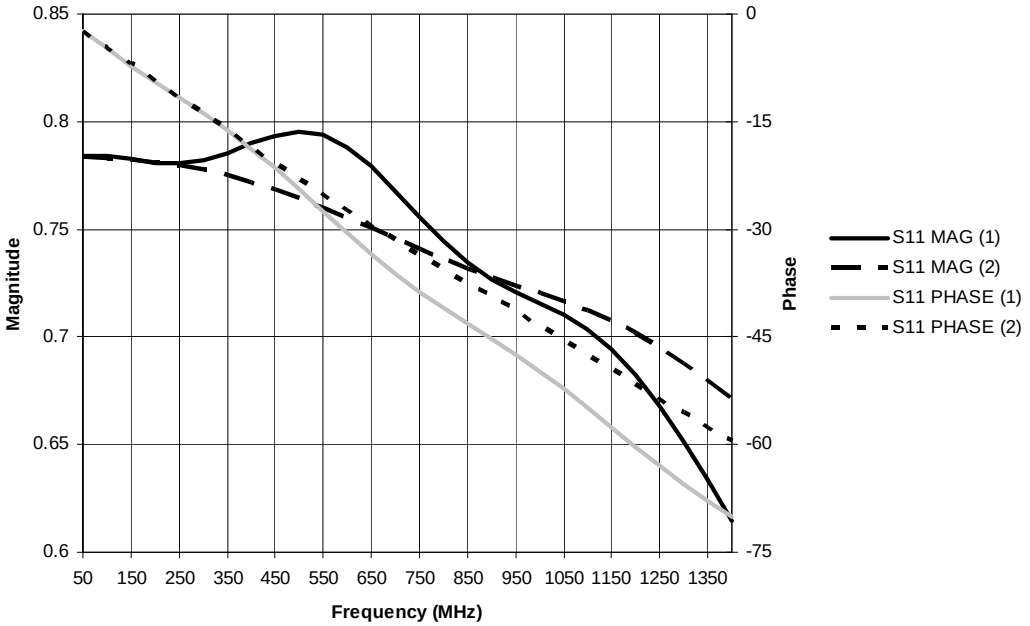


Fig 10: S11, D to FLTRDR

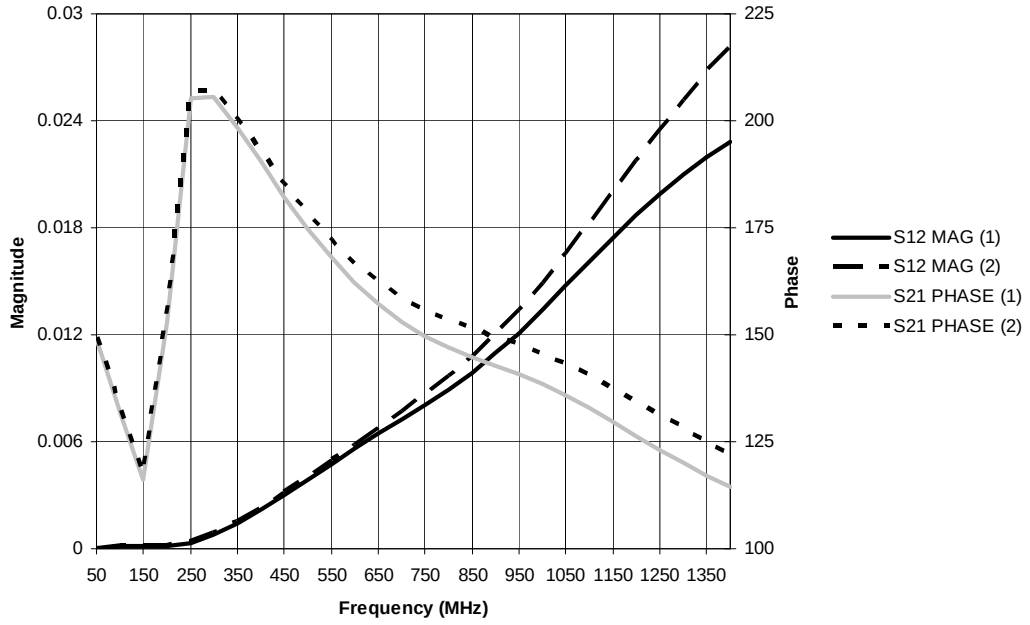


Fig 11: S12, D to FLTRDR

(1): $\overline{\text{FLTRDR}}$ open, not connected to FLTRDR
(2): $\overline{\text{FLTRDR}}$ connected to FLTRDR

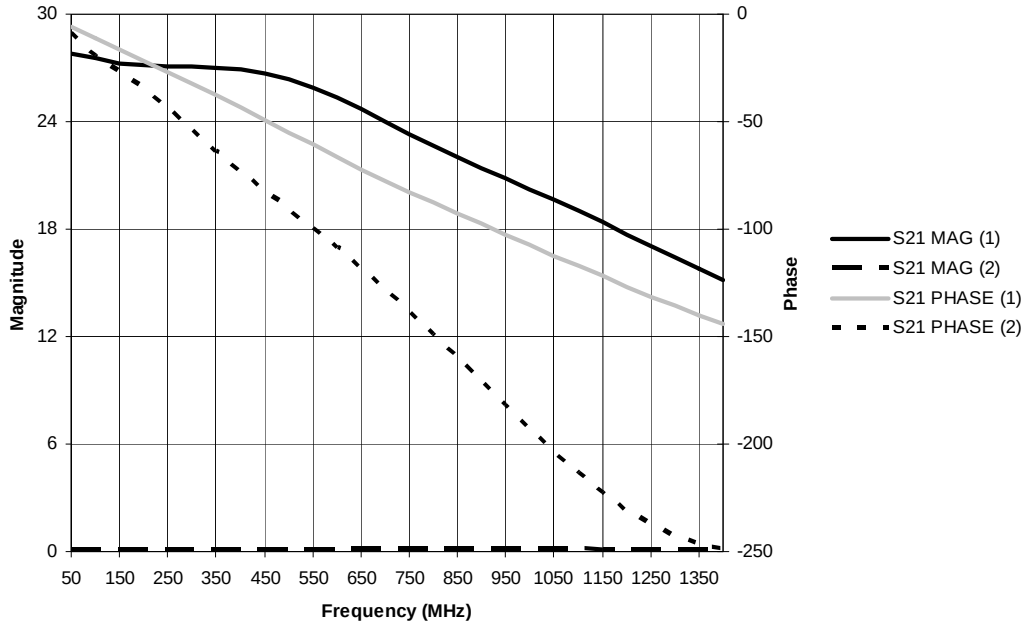


Fig 12: S21, D to FLTRDR

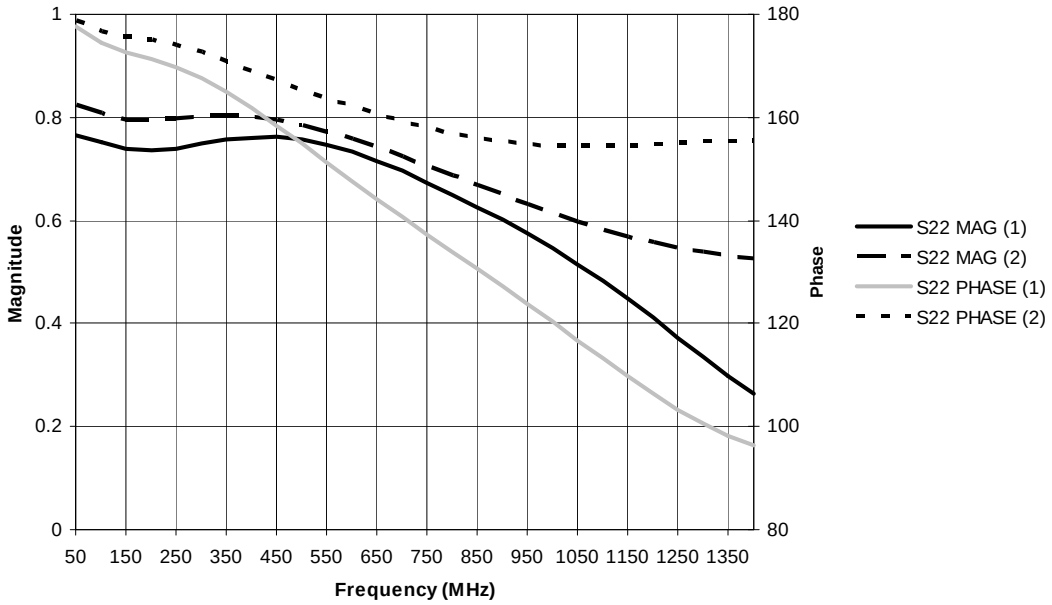


Fig 13: S22, D to FLTRDR

(1): $\overline{\text{FLTRDR}}$ open, not connected to FLTRDR
(2): $\overline{\text{FLTRDR}}$ connected to FLTRDR

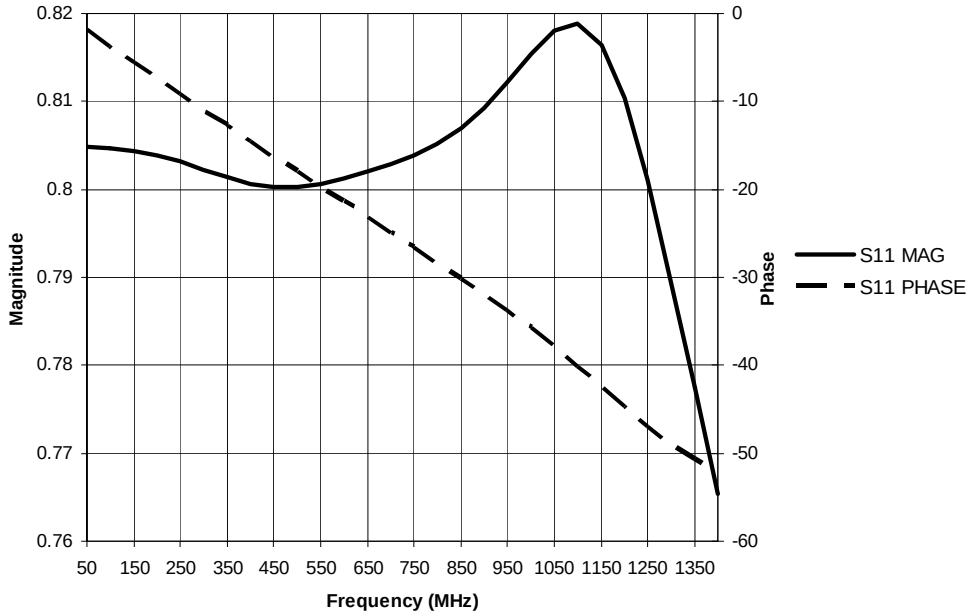


Fig 14: S11, AMPIN to Q_{HG}

IMPEDANCES

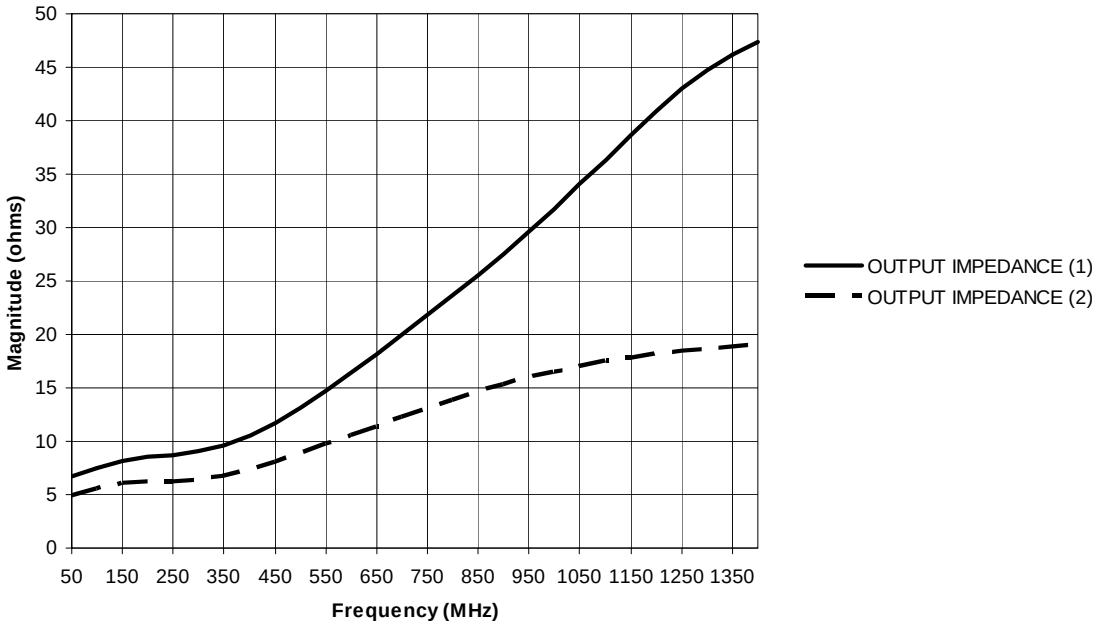


Fig 15: FLTDR Output Impedance

(1): $\overline{\text{FLTRDR}}$ open, not connected to FLTRDR
(2): $\overline{\text{FLTRDR}}$ connected to FLTRDR

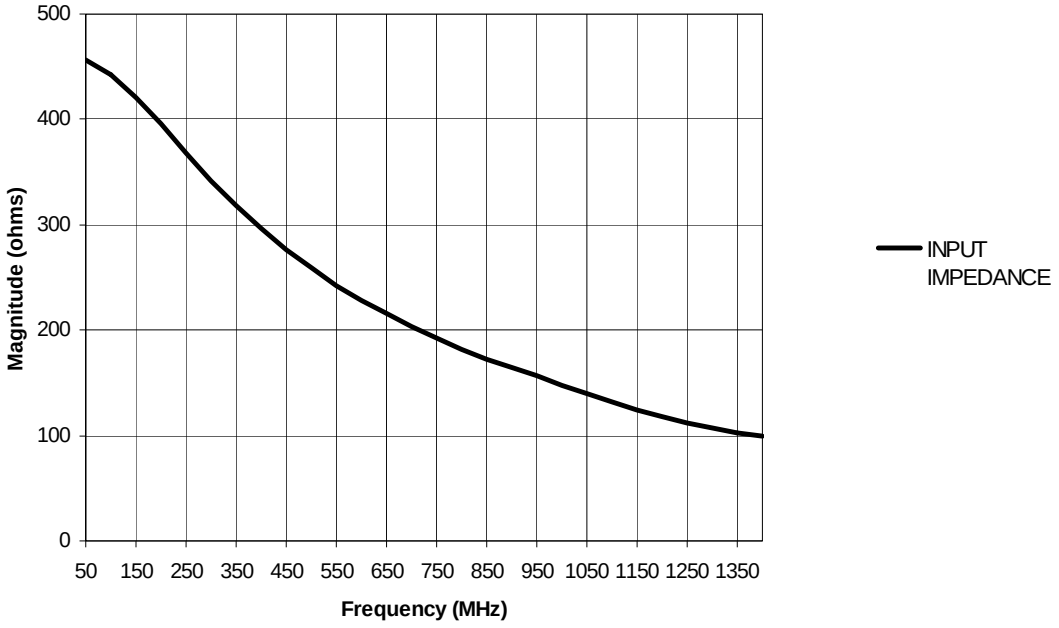
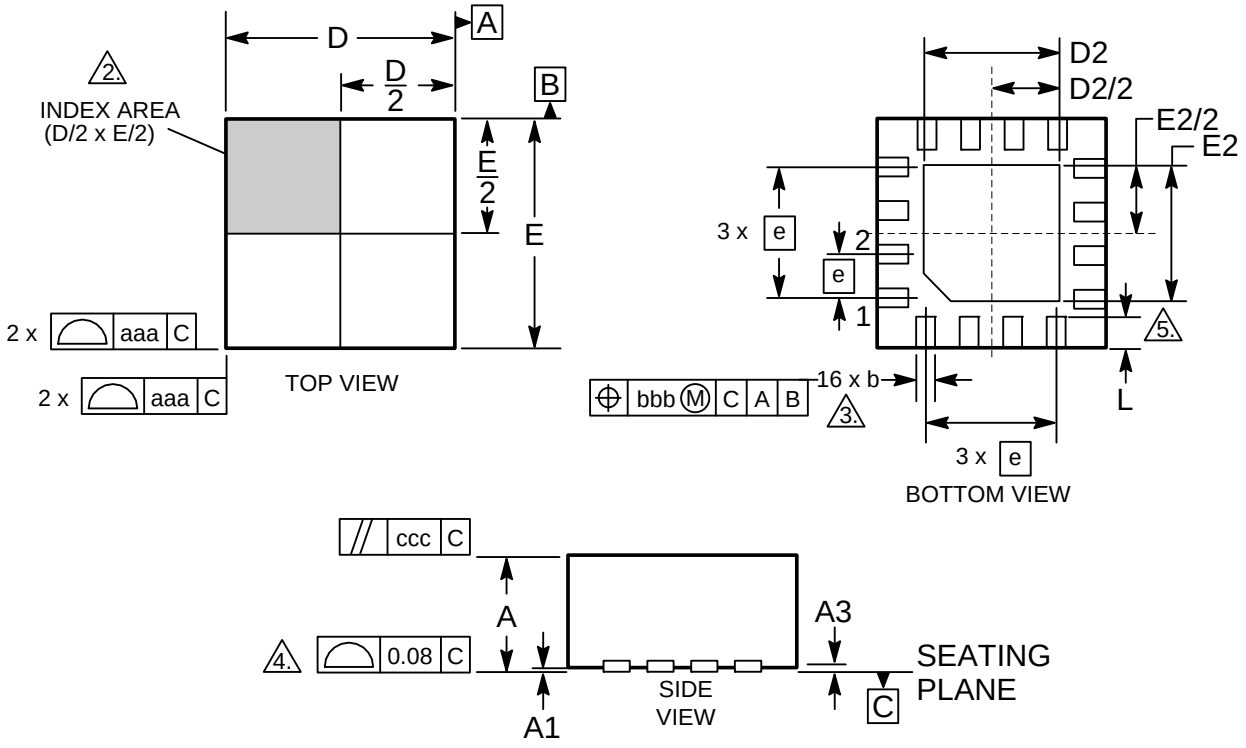


Fig 16: AMPIN Input Impedance

PACKAGE DIAGRAM
MLP 16



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	