



Programmable Spread-Spectrum and DC-Balance 21-Bit Deserializer

General Description

The MAX9232 deserializes three LVDS serial-data inputs into 21 single-ended LVCMOS/LVTTL outputs. A separate parallel-rate LVDS clock provides the timing for deserialization. The MAX9232 features spread-spectrum capability, allowing the output data and clock frequency to spread over a specified range to reduce EMI. The single-ended data and clock outputs are programmable for a frequency spread of $\pm 2\%$, $\pm 4\%$, or no spread. The spread-spectrum function is also available when the MAX9232 operates in non-DC-balanced mode. The modulation rate of the spread is 32kHz for a 33MHz LVDS clock input and scales linearly with frequency. Using VSYNC on RxOUT13 and HSYNC on RxOUT6, a reset of the spread-spectrum FIFO is performed every frame, preventing FIFO overflow and underflow. The single-ended outputs have a separate supply, allowing +1.8V to +5V output logic levels.

The MAX9232 features programmable DC balance, allowing isolation between a serializer and deserializer using AC-coupling. The MAX9232 operates with the MAX9209/MAX9213 serializer and has a falling-edge strobe. The LVDS inputs meet ISO 10605 ESD specifications with $\pm 25\text{kV}$ Air-Gap Discharge and $\pm 8\text{kV}$ Contact Discharge ratings.

The MAX9232 is available in a 48-pin TSSOP package and operates within the -40°C to $+85^{\circ}\text{C}$ temperature range.

Applications

Automotive Navigation Systems
Automotive DVD Entertainment Systems
Digital Copiers
Laser Printers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9232EUM	-40°C to $+85^{\circ}\text{C}$	48 TSSOP	U48-1

Features

- ◆ Programmable $\pm 4\%$, $\pm 2\%$, or OFF Spread-Spectrum Output for Reduced EMI
- ◆ Programmable DC Balance or Non-DC Balance
- ◆ DC Balance Allows AC-Coupling for Wider Input Common-Mode Voltage Range
- ◆ Spread Spectrum Operates in DC-Balanced or Non-DC-Balanced Mode
- ◆ FIFO Reset During Vertical Blanking
- ◆ 16MHz-to-34MHz (DC-Balanced) and 20MHz-to-40MHz (Non-DC-Balanced) Operation
- ◆ High-Impedance Outputs when PWRDWN is Low Allow Output Busing
- ◆ Fail-Safe Inputs in Non-DC-Balanced Mode
- ◆ Separate Output Supply Pins Allow Interface to +1.8V, +2.5V, +3.3V, and +5V Logic
- ◆ LVDS Inputs Meet ISO 10605 ESD Protection at $\pm 25\text{kV}$ Air Discharge and $\pm 8\text{kV}$ Contact Discharge
- ◆ LVDS Inputs Meet IEC 61000-4-2 Level 4 ESD Protection at $\pm 15\text{kV}$ Air and $\pm 8\text{kV}$ Contact Discharge
- ◆ LVDS Inputs Conform to ANSI TIA/EIA-644 Standard
- ◆ +3.3V Main Power Supply

Pin Configuration

