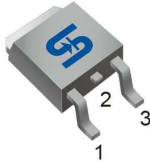


TO-252  
(DPAK)



**Pin Definition:**

1. Gate
2. Drain
3. Source

**PRODUCT SUMMARY**

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
60	7.3 @ $V_{GS}=10V$	66

**Features**

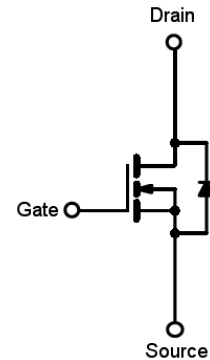
- Advanced Trench Technology
- Low  $R_{DS(ON)}$  7.3m $\Omega$  (Max.)
- Low gate charge typical @ 81nC (Typ.)
- Low  $C_{rss}$  typical @ 339pF (Typ.)

**Ordering Information**

Part No.	Package	Packing
TSM60N06CP ROG	TO-252	2.5Kpcs / 13" Reel

**Note:** "G" denote for Halogen Free Product

**Block Diagram**



N-Channel MOSFET

**Absolute Maximum Rating** ( $T_a = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	66
		$T_C=70^\circ C$	53
		$T_A=25^\circ C$	13
		$T_A=70^\circ C$	10
Drain Current-Pulsed Note 1	$I_{DM}$	150	A
Avalanche Current, L=0.1mH	$I_{AS}, I_{AR}$	53	A
Avalanche Energy, L=0.1mH	$E_{AS}, E_{AR}$	400	mJ
Maximum Power Dissipation	$P_D$	$T_C=25^\circ C$	44.6
		$T_C=70^\circ C$	28.6
		$T_A=25^\circ C$	2
		$T_A=70^\circ C$	1.3
Storage Temperature Range	$T_{STG}$	-55 to +150	$^\circ C$
Operating Junction Temperature Range	$T_J$	-55 to +150	$^\circ C$

\* Limited by maximum junction temperature

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R_{\theta_{JC}}$	2.8	$^\circ C/W$
Thermal Resistance - Junction to Ambient	$R_{\theta_{JA}}$	62	$^\circ C/W$

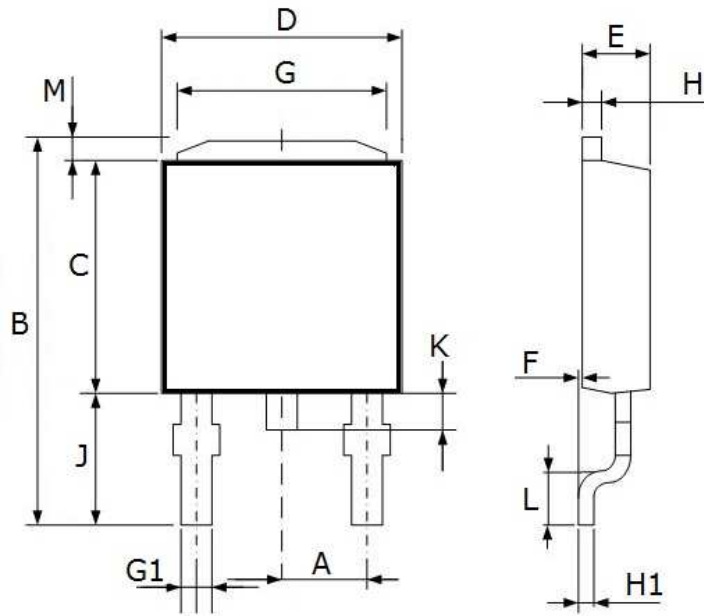
**Electrical Specifications** (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	BV <sub>DSS</sub>	100	--	--	V
Drain-Source On-State Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A	R <sub>DS(ON)</sub>	--	6.3	7.3	mΩ
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	V <sub>GS(TH)</sub>	2	3	4	V
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>	--	--	1	uA
Gate Body Leakage	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	I <sub>GSS</sub>	--	--	±100	nA
<b>Dynamic</b>						
Total Gate Charge	V <sub>DS</sub> = 630V, I <sub>D</sub> = 30A, V <sub>GS</sub> = 10V	Q <sub>g</sub>	--	81	--	nC
Gate-Source Charge		Q <sub>gs</sub>	--	23	--	
Gate-Drain Charge		Q <sub>gd</sub>	--	24	--	
Input Capacitance	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, f = 1.0MHz	C <sub>iss</sub>	--	4382	--	pF
Output Capacitance		C <sub>oss</sub>	--	668	--	
Reverse Transfer Capacitance		C <sub>rss</sub>	--	339	--	
<b>Switching</b>						
Turn-On Delay Time	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 30V, R <sub>G</sub> = 3Ω	t <sub>d(on)</sub>	--	25	--	nS
Turn-On Rise Time		t <sub>r</sub>	--	19	--	
Turn-Off Delay Time		t <sub>d(off)</sub>	--	85	--	
Turn-Off Fall Time		t <sub>f</sub>	--	43	--	
<b>Drain-Source Diode Characteristics and Maximum Rating</b>						
Drain-Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	V <sub>SD</sub>	-	0.8	1.3	V
Reverse Recovery Time	I <sub>S</sub> = 30A, T <sub>J</sub> =25 °C di/dt = 500A/us	t <sub>fr</sub>		36		nS
Reverse Recovery Charge		Q <sub>fr</sub>		53		nC

**Notes:**

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- Rθ<sub>JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Rθ<sub>JC</sub> is guaranteed by design while Rθ<sub>CA</sub> is determined by the user's board design. Rθ<sub>JA</sub> shown below for single device operation on FR-4 in still air

**TO-252 Mechanical Drawing**



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.286 BSC		0.090 BSC	
B	9.40	10.40	0.370	0.409
C	5.40	6.23	0.213	0.245
D	6.40	6.80	0.252	0.268
E	2.20	2.40	0.087	0.094
F	0.00	0.20	0.000	0.008
G	5.20	5.50	0.205	0.217
G1	0.50	0.91	0.020	0.036
H	0.45	0.60	0.018	0.024
H1	0.40	0.60	0.016	0.024
J	2.50	2.90	0.098	0.114
K	0.60	1.00	0.023	0.039
L	1.40	1.78	0.055	0.070
M	0.88	1.28	0.034	0.050

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