NEC

MOS INTEGRATED CIRCUIT

μPD78074Y, 78075Y, 78076Y, 78078Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78074Y, 78075Y, 78076Y, and 78078Y are the same as the corresponding product without the Y suffix except that the I²C bus control function has been added. These products are ideal for AV products.

Besides a high-speed, high-performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

The μPD78P078 devices including a one-time PROM version and an EPROM version, both of which can operate in the same power supply voltage range as a mask ROM version, and various development tools are available.

The details of the functions are described in the following user's manuals. Be sure to read it before starting design.

μPD78078,78078Y Subseries User's Manual : IEU-1396

78K/0 Series User's Manual – Instructions : IEU-1372

FEATURES

- Internal high capacity ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Buffer RAM	Internal Expansion RAM	
μPD78074Y[Note]	32K bytes	1024 bytes	32 bytes	Not provided	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78075Y[Note]	40K bytes				
μPD78076Y	48K bytes			1024 bytes	
μPD78078Y	60K bytes				

Note Under development

- External memory expansion space : 64K bytes
- Instruction execution time can be changed from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 88 (N-ch open-drain : 8)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
  - 3-wire/2-wire/I²C bus mode : 1 channel
  - 3-wire mode : 1 channel
  - 3-wire/UART mode : 1 channel
- Timer : 7 channels
- Supply voltage : V_{DD} = 1.8 to 5.5 V

APPLICATION

Cellular telephones, cordless telephones, AV equipment, etc.

The information in this document is subject to change without notice.

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ORDERING INFORMATION

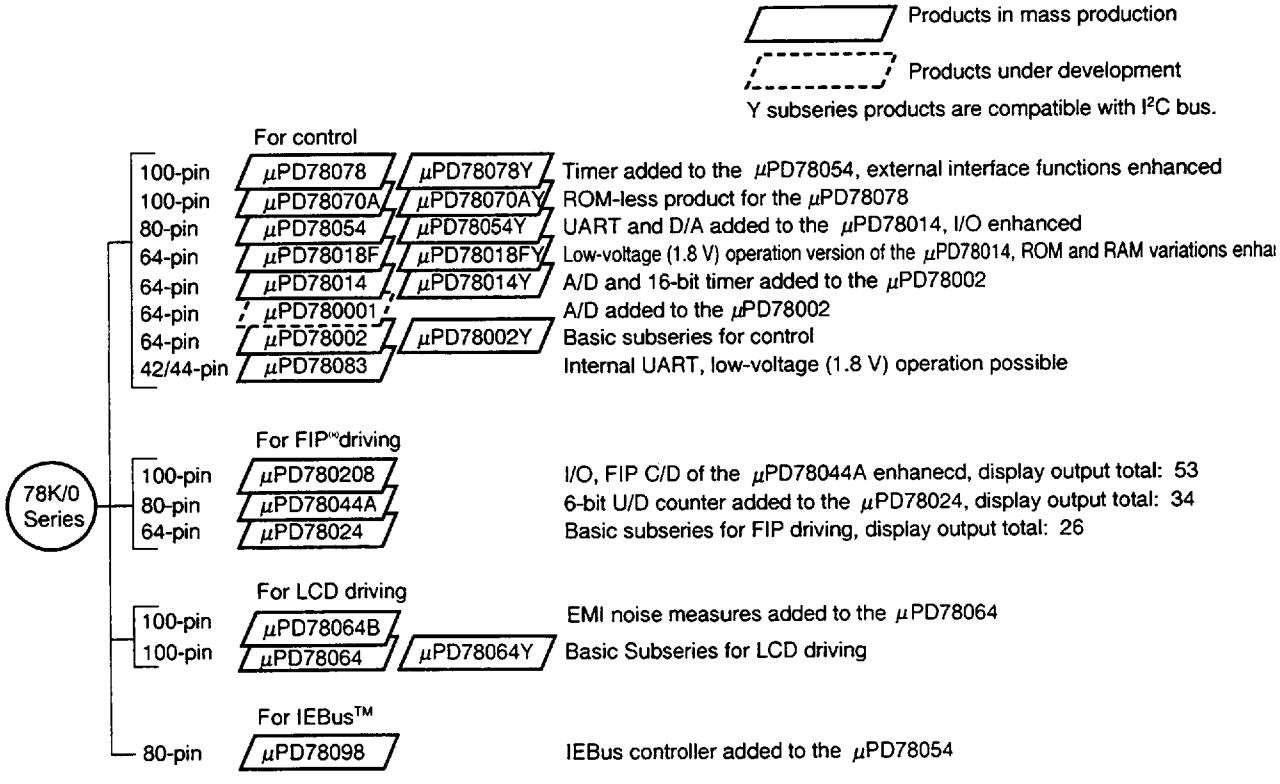
Part Number	Package
μPD78074YGF-xxx-3BA[Note]	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78075YGF-xxx-3BA[Note]	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78076YGF-xxx-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78078YGF-xxx-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)

Note Under development

Remark xxx indicates ROM code suffix.

78K/0 SERIES DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT						
For Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	O
	μPD78070A	—								61	2.7 V	
	μPD78054	16 K-60 K	2ch							69	2.0 V	
	μPD78018F	8 K-48 K						—	2ch	53	1.8 V	
	μPD78014	8 K-32 K									2.7 V	
	μPD780001	8 K		—	—				1ch	39		—
	μPD78002	8 K-16 K			1ch		—			53		O
	μPD78083				—		8ch		1ch (UART: 1ch)	33	1.8 V	—
For FIP driving	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	74	2.7 V	—
	μPD78044A	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
For LCD driving	μPD78064B	32 K	2ch	1ch	1ch	1ch	8ch	—	2ch (UART: 1ch)	57	2.0 V	—
	μPD78064	16 K-32 K										
For IEBus	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	O

OVERVIEW OF FUNCTION

Item \ Part Number		μPD78074Y[Note]	μPD78075Y[Note]	μPD78076Y	μPD78078Y
Internal memory	ROM	32K bytes	40K bytes	48K bytes	60K bytes
	Internal high-speed RAM	1024 bytes			
	Buffer RAM	32 bytes			
	Internal expansion RAM	Not provided		1024 bytes	
Memory space		64K bytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		On-chip instruction execution time selective function			
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz)			
	When subsystem clock selected	122 μs (at 32.768 kHz)			
Instruction set		• 16-bit operation • Multiplcation/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.			
I/O ports		Total : 88 • CMOS input : 2 • CMOS I/O : 78 • N-ch open-drain I/O : 8			
A/D converter		• 8-bit resolution × 8 channels			
D/A converter		• 8-bit resolution × 2 channels			
Serial interface		• 3-wire/2-wire/I²C bus mode selectable: 1 channel • 3-wire mode (on-chip max. 32-byte automatic data transmit/receive function): 1 channel • 3-wire/UART mode selectable: 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 4 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		5 (14-bit PWM output × 1, 8-bit PWM output × 2)			
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock of 5.0 MHz) 32.768 kHz (at subsystem clock of 32.768 kHz)			
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock of 5.0 MHz)			
Vectored interrupts	Maskable interrupts	Internal : 15 external : 7			
	Non-maskable interrupts	Internal : 1			
	Software interrupts	Internal : 1			
Test input		Internal : 1 External : 1			
Supply voltage		V_{DD} = 1.8 to 5.5 V			
Package		• 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)			

Note Under development

CONTENTS

1. PIN CONFIGURATION (TOP VIEW) 6

2. BLOCK DIAGRAM 8

3. PIN FUNCTIONS 9
   3.1 Port Pins 9
   3.2 Non-port Pins 11
   3.3 Pin I/O Circuits and Recommended Connection of Unused Pins 13

4. MEMORY SPACE 17

5. PERIPHERAL HARDWARE FUNCTIONS 18
   5.1 Ports 18
   5.2 Clock Generator 19
   5.3 Timer/Event Counter 19
   5.4 Clock Output Control Circuit 23
   5.5 Buzzer Output Control Circuit 23
   5.6 A/D Converter 24
   5.7 D/A Converter 24
   5.8 Serial Interfaces 25
   5.9 Real-Time Output Port 27

6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS 28
   6.1 Interrupt Functions 28
   6.2 Test Functions 31

7. EXTERNAL DEVICE EXPANSION FUNCTIONS 32

8. STANDBY FUNCTION 32

9. RESET FUNCTION 33

10. INSTRUCTION SET 34

11. ELECTRICAL SPECIFICATIONS 36

12. CHARACTERISTIC CURVES (REFERENCE VALUE) 64

13. PACKAGE DRAWINGS 66

14. RECOMMENDED SOLDERING CONDITIONS 67

APPENDIX A. DEVELOPMENT TOOLS 68

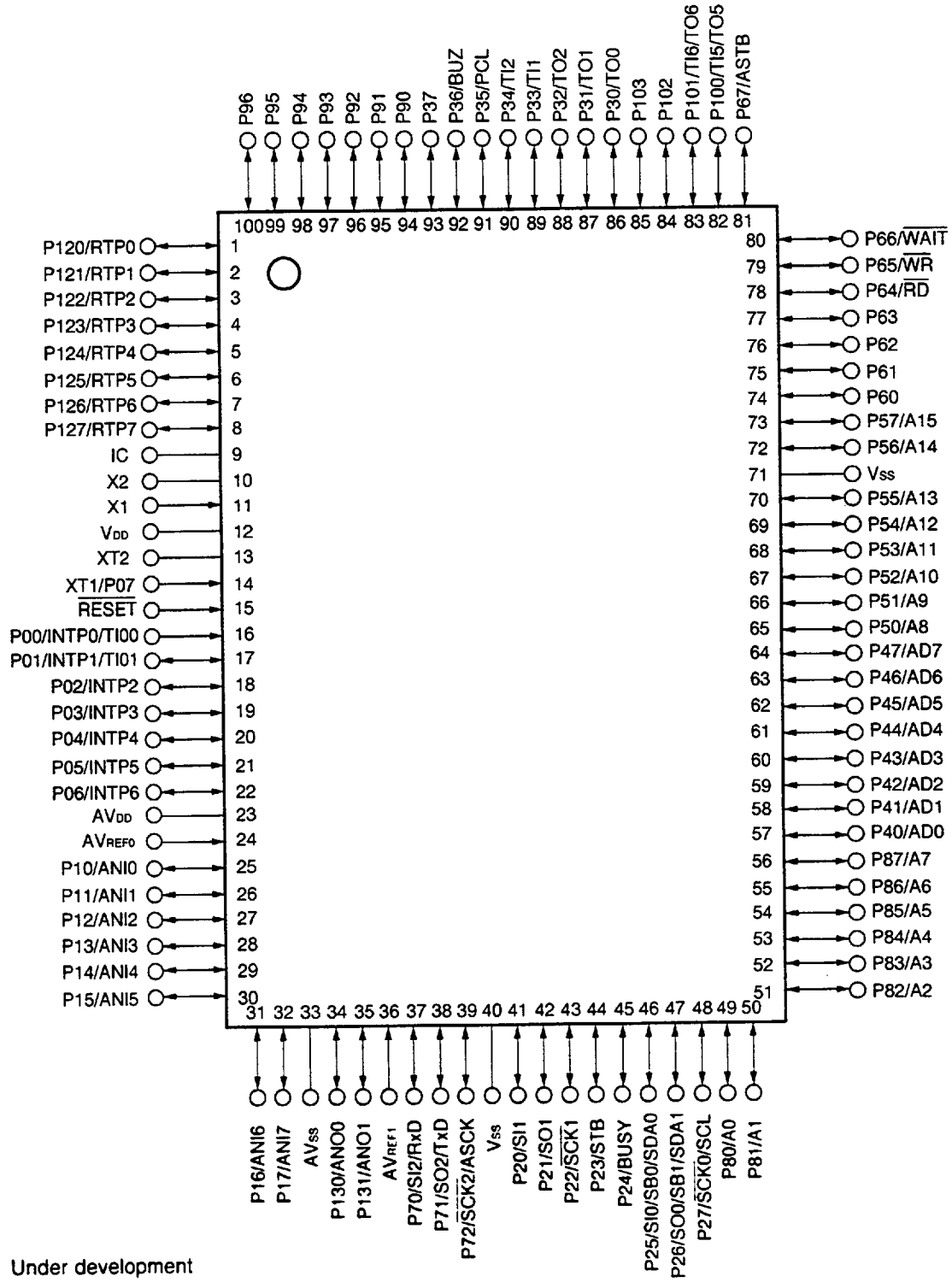
APPENDIX B. RELATED DOCUMENTS 70

1. PIN CONFIGURATION (TOP VIEW)

•100-pin plastic QFP (14 × 20 mm)

μPD78074YGF-xxx-3BA[Note], 78075YGF-xxx-3BA[Note]

μPD78076YGF-xxx-3BA, 78078YGF-xxx-3BA



Note Under development

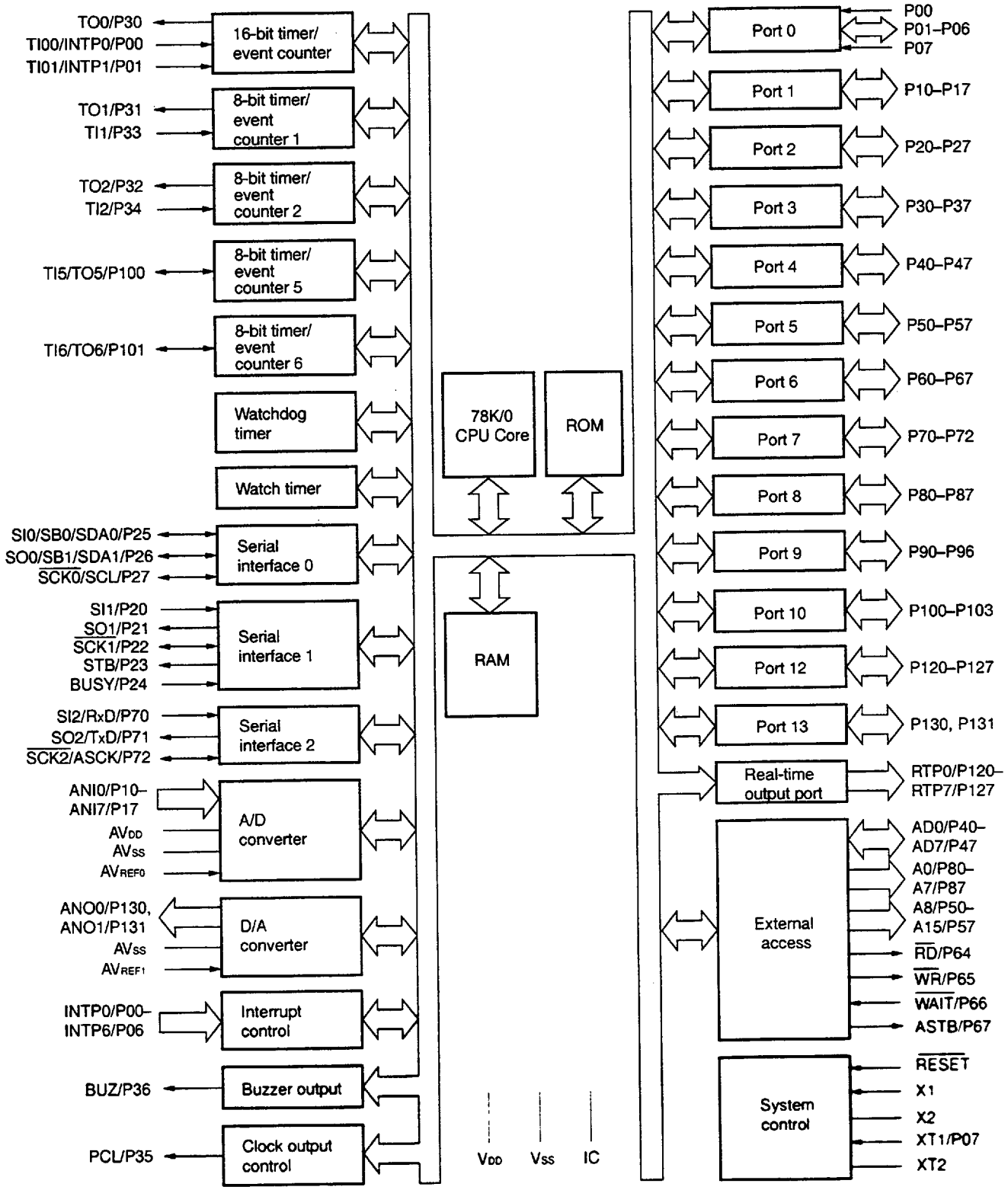
Cautions 1. Connect IC (internally connected) pin directly to VSS.

2. AVDD pin should be connected to VDD.

3. AVSS pin should be connected to VSS.

P00 to P07	:	Port0
P10 to P17	:	Port1
P20 to P27	:	Port2
P30 to P37	:	Port3
P40 to P47	:	Port4
P50 to P57	:	Port5
P60 to P67	:	Port6
P70 to P72	:	Port7
P80 to P87	:	Port8
P90 to P96	:	Port9
P100 to P103	:	Port10
P120 to P127	:	Port12
P130, P131	:	Port13
RTP0 to RTP7	:	Real-Time Output Port
INTP0 to INTP6	:	Interrupt from Peripherals
TI00, TI01	:	Timer Input
TI1, TI2, TI5, TI6	:	Timer Input
TO0 to TO2, TO5, TO6	:	Timer Output
SB0, SB1	:	Serial Bus
SI0 to SI2	:	Serial Input
SO0 to SO2	:	Serial Output
$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
AD0 to AD7	:	Address/Data Bus
A0 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
$AV_{REF0,1}$	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Shared by:
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{SCK0}$/SCL
P30	Input/ output	Port 3 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pins as an input port, set 1 to bit 6 (FRC) of the processor clock control register. Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, pull-up resistor is automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Shared by:
P50 to P57	Input/ output	Port 5 8-bit input/output port LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/ output port Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	——
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/ output	Port 7 3-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P80 to P87	Input/ output	Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	A0 to A7
P90	Input/ output	Port 9 7-bit input/output port Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P91					
P92					
P93					
P94			When used as an input port, pull-up resistor can be connected by software.		
P95					
P96					
P100	Input/ output	Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	TI5/TO5
P101					TI6/TO6
P102, P103					—
P120 to P127	Input/ output	Port 12 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	RTP0 to RTP7
P130, P131	Input/ output	Port 13 2-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	ANO0, ANO1

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Shared by:
INTP0	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output.	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TI5		External count clock input to 8-bit timer (TM5).		P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P100/TO6
TO0	Output	16-bit timer output (also used for 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
TO5		8-bit timer output (also used for 8-bit PWM output).		P100/TI5
TO6				P101/TI6
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Shared by:
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A0 to A7	Output	Low-order address bus at external memory expansion.	Input	P80 to P87
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which externally latches the address information output to ports 4, 5 and 8 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connect to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect directly to V_{SS}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to Vss.
P01/INTP1/TI01	8-A	Input/output	Connect to Vss via a resistor individually.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connected to VDD.
P10/ANI0 to P17/ANI7	11	Input/output	Connect to VDD or Vss via a resistor individually.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Connect to VDD via a resistor individually.
P50/A8 to P57/A15	5-A	Input/output	Connect to VDD or Vss via a resistor individually.
P60 to P63	13-B	Input/output	Connect to VDD via a resistor individually.
P64/$\overline{RD}$	5-A	Input/output	Connect to VDD or Vss via a resistor individually.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/output	Connect to V_{DD} or Vss via a resistor individually.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P80/A0 to P87/A7	5-A		
P90 to P93	13-B	Input/output	Connect to V_{DD} via a resistor individually.
P94 to P96	5-A	Input/output	Connect to V_{DD} or Vss via a resistor individually.
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102, P103	5-A		
P120/RTP0 to P127/RTP7			
P130/ANO0 , P131/ANO1	12-A	Input/output	Connect to Vss via a resistor indivisually.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to Vss.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AVss			Connect to Vss.
IC			Connect directly to Vss.

Figure 3-1. Pin Input/Output Circuits (1/2)

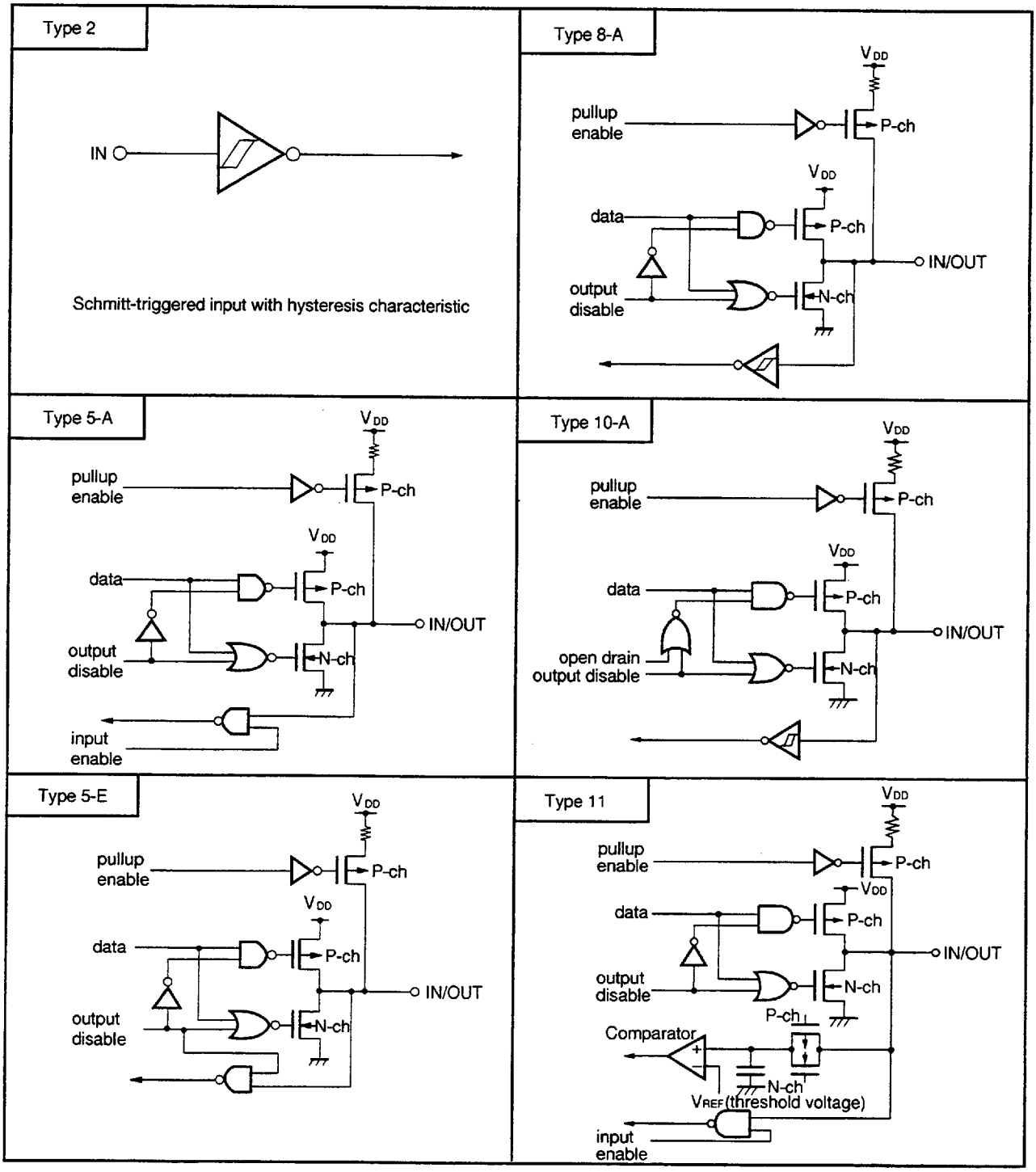
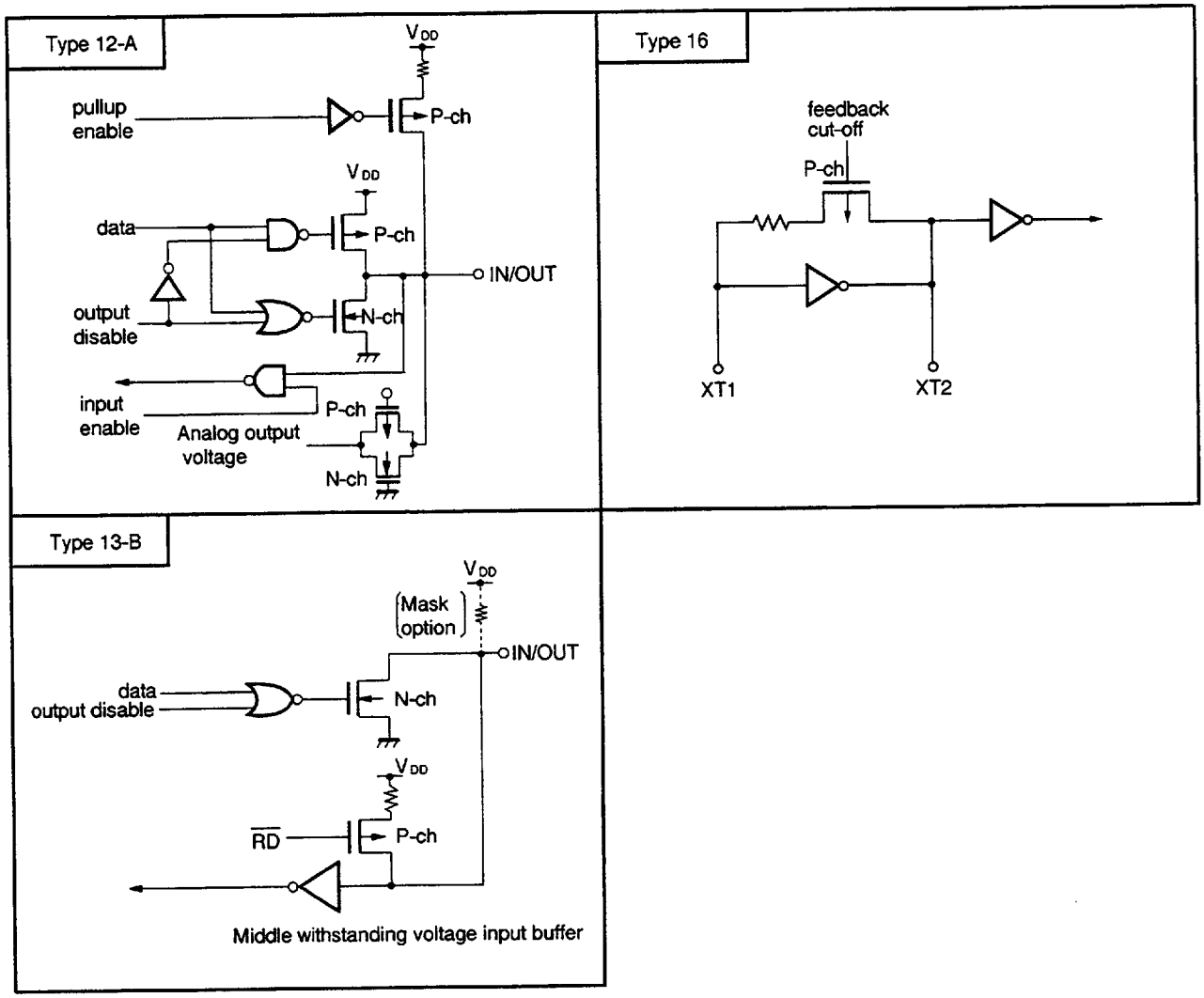


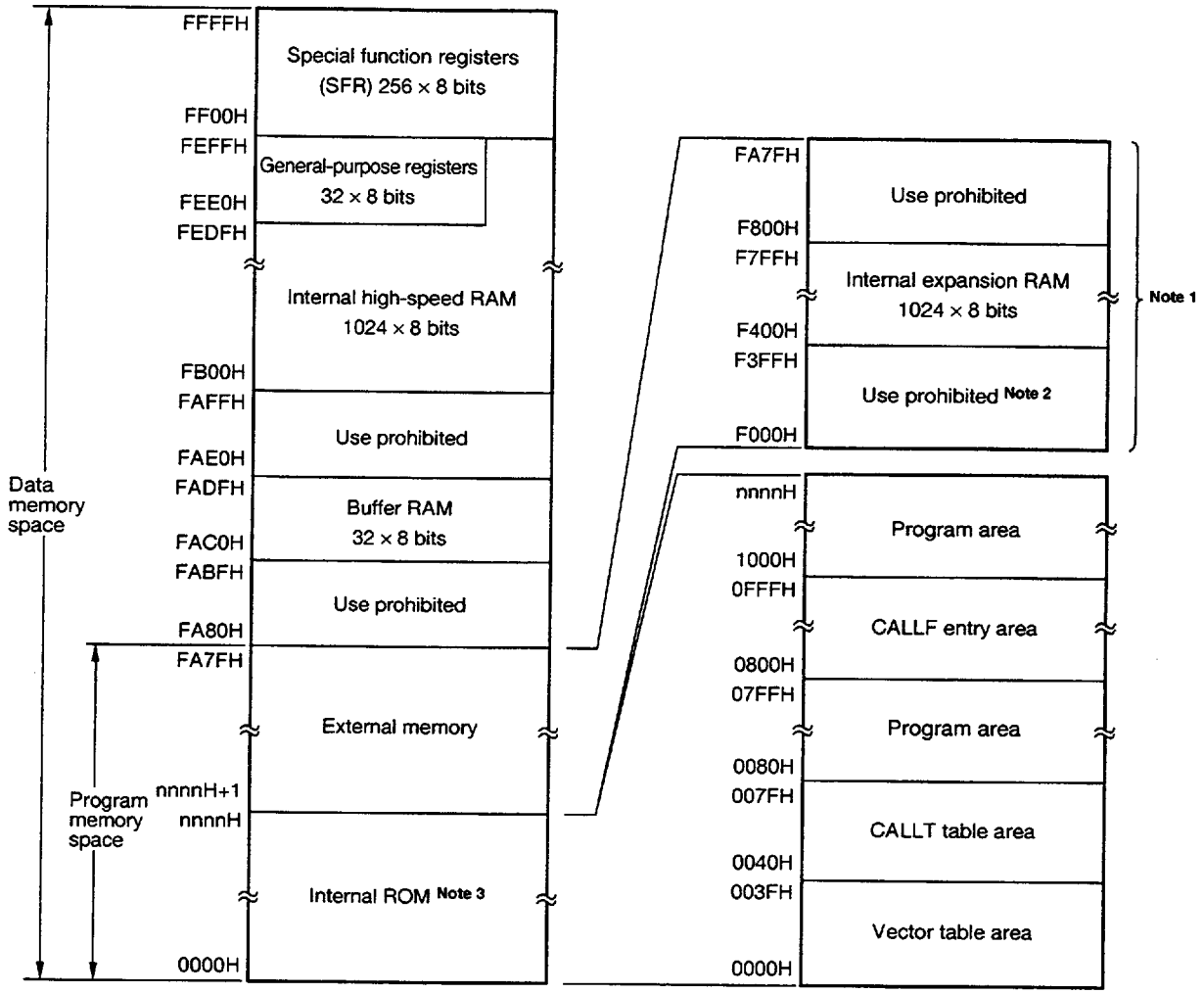
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of the μPD78074Y, 78075Y, 78076Y and 78078Y is shown in Figure 4-1.

Figure 4-1. Memory Map



Notes 1. The μPD78076Y and 78078Y only.

2. If external device expansion functions are to be employed for the μPD78078Y, set the size of the internal ROM to below 56K bytes using the memory size switching register.

3. The internal ROM capacity depends on the product. (See the following table.)

Part Number	Internal ROM Last Address nnnnH
μPD78074Y	7FFFH
μPD78075Y	9FFFH
μPD78076Y	BFFFH
μPD78078Y	EFFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into three types.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P06, Port 1 to 5, P64 to P67, Port 7, Port 8, P94 to P96, Port 10, Port 12, Port 13) : 78
- N-ch open-drain input/output (P60 to P63, P90 to P93) : 8

Total : 88

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P07	Input only.
	P01 to P06	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output port. Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be used by software. The test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be used by mask option. LED can be driven directly.
	P64 to P67	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 8	P80 to P87	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 9	P90 to P93	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be used by mask option. LED can be driven directly.
	P94 to P96	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software
Port 10	P100 to P103	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 12	P120 to P127	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 13	P130, P131	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.

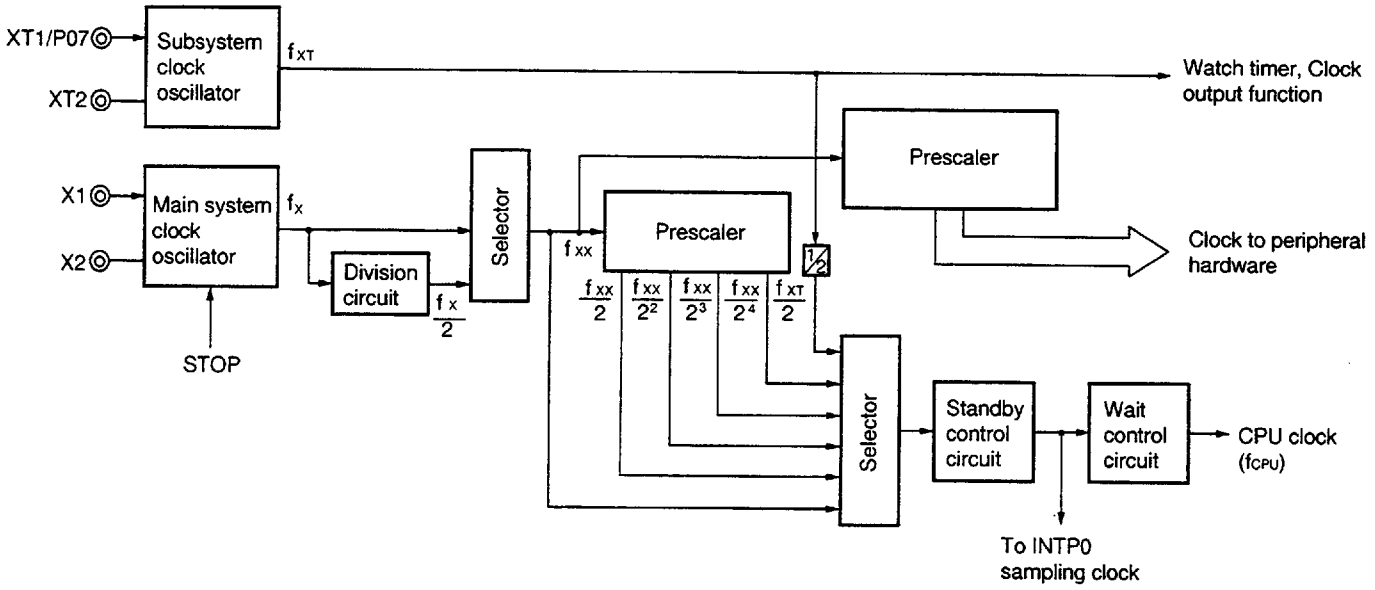
5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators.

It is possible to change the instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 4 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		16-bit Timer/Event Counter	8-bit Timer/Event Counter 1, 2	8-bit Timer/Event Counter 5, 6	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	2 channels	—	—
Function	Timer output	1 output	2 outputs	2 outputs	—	—
	PWM output	1 output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—	—
	Square wave output	1 output	2 outputs	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—	—
	Interrupt request	2	2	2	1	1
	Test input	—	—	—	1	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

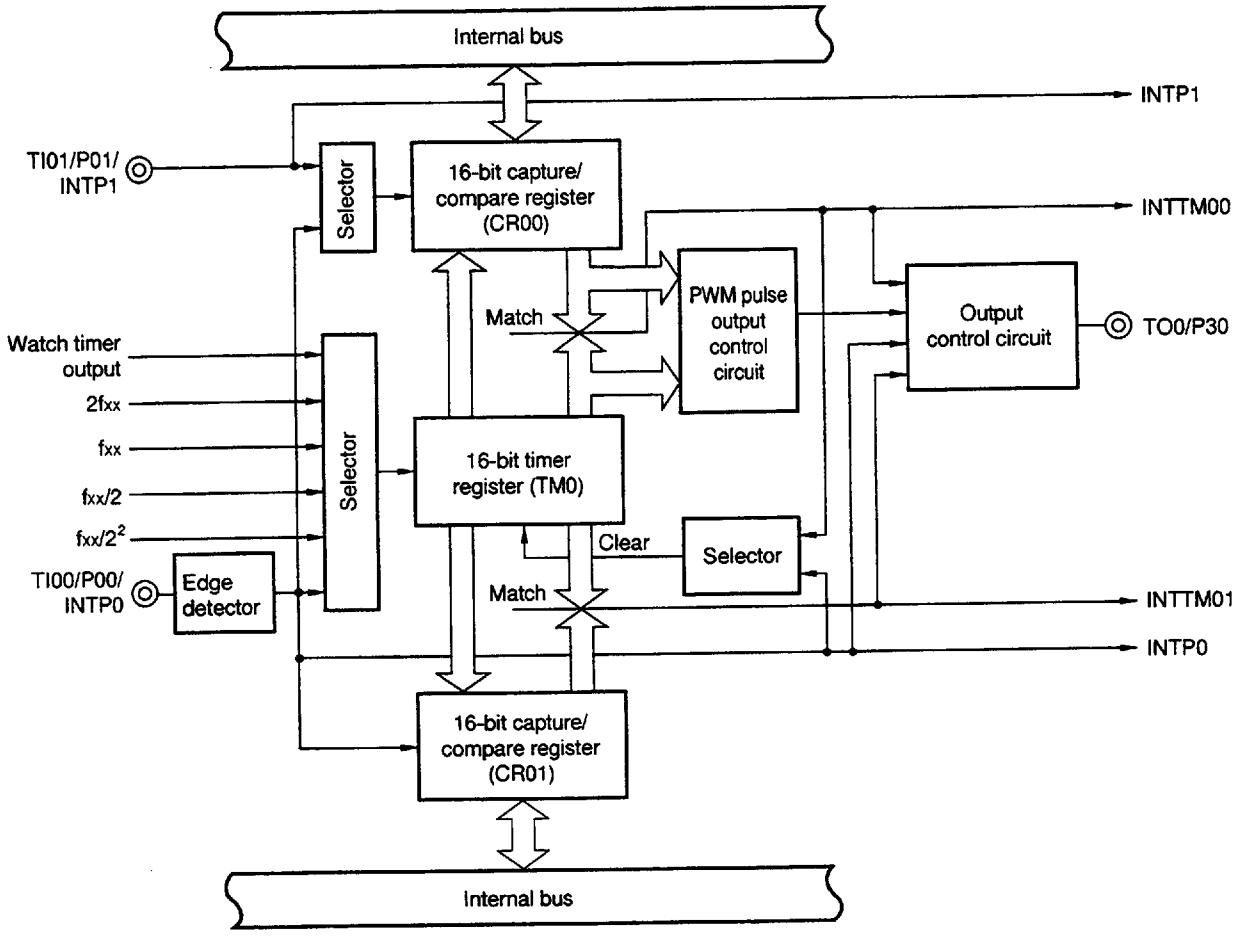


Figure 5-3. 8-Bit Timer/Event Counter 1, 2 Block Diagram

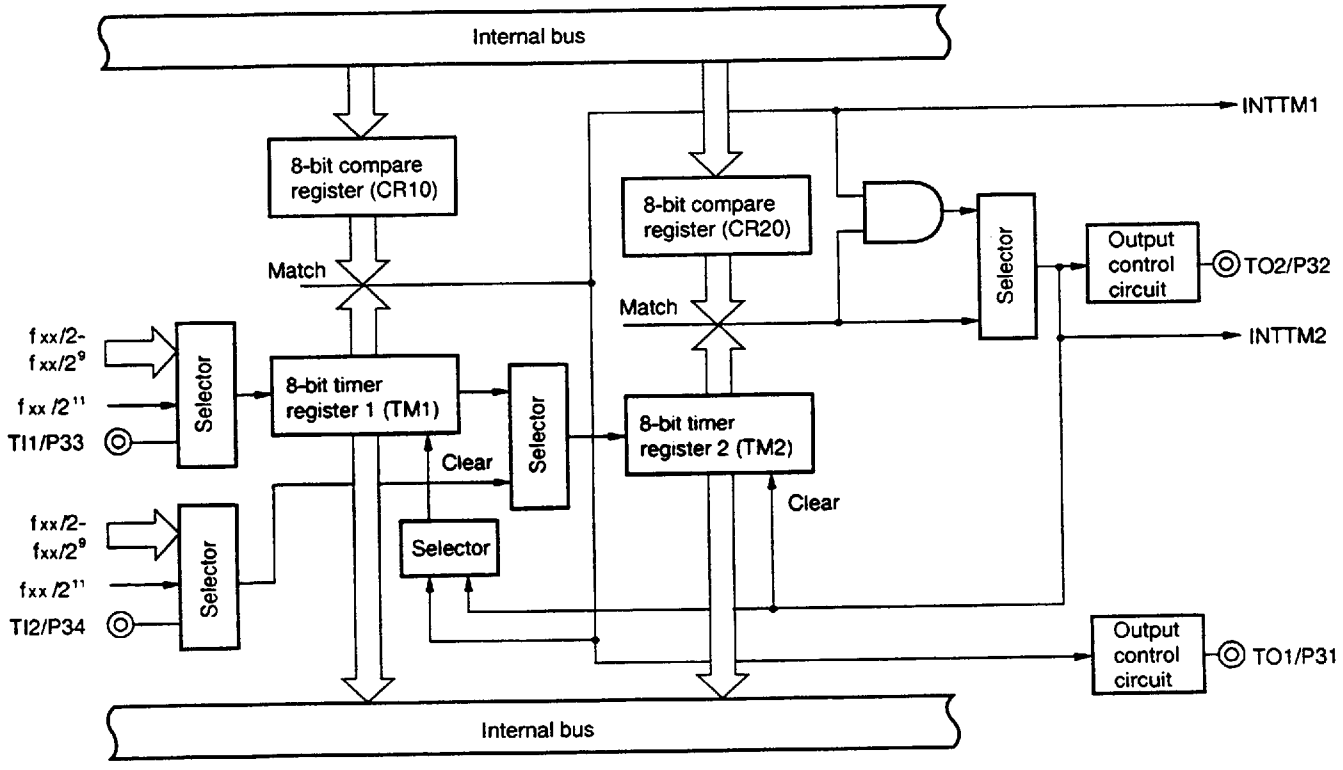
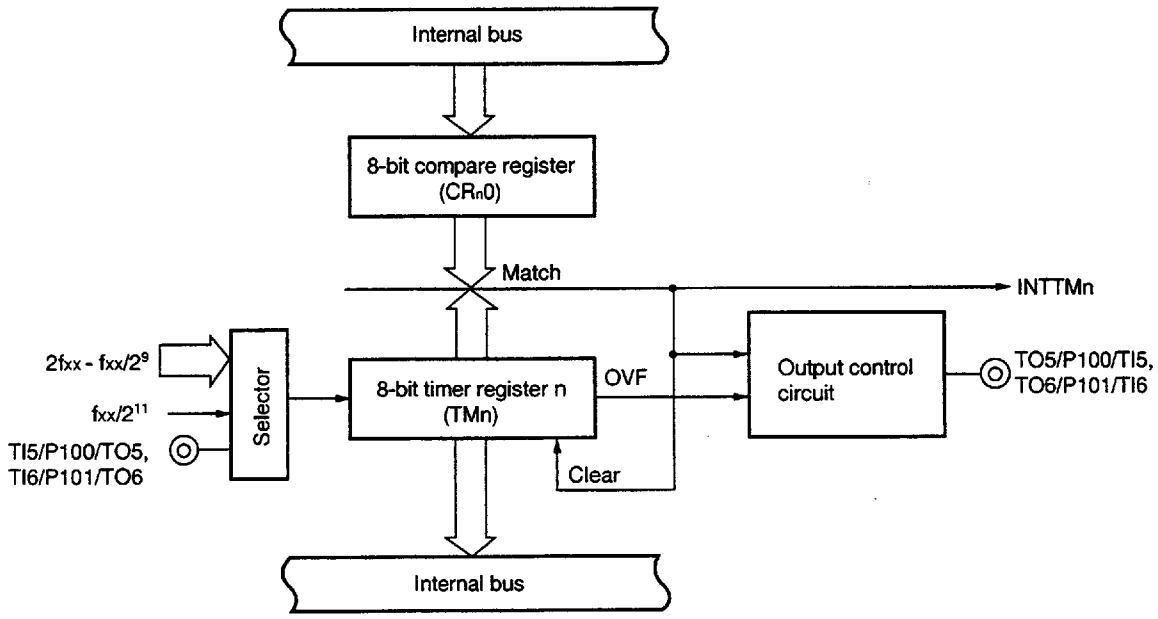


Figure 5-4. 8-Bit Timer/Event Counter 5, 6 Block Diagram



n = 5, 6

Figure 5-5. Watch Timer Block Diagram

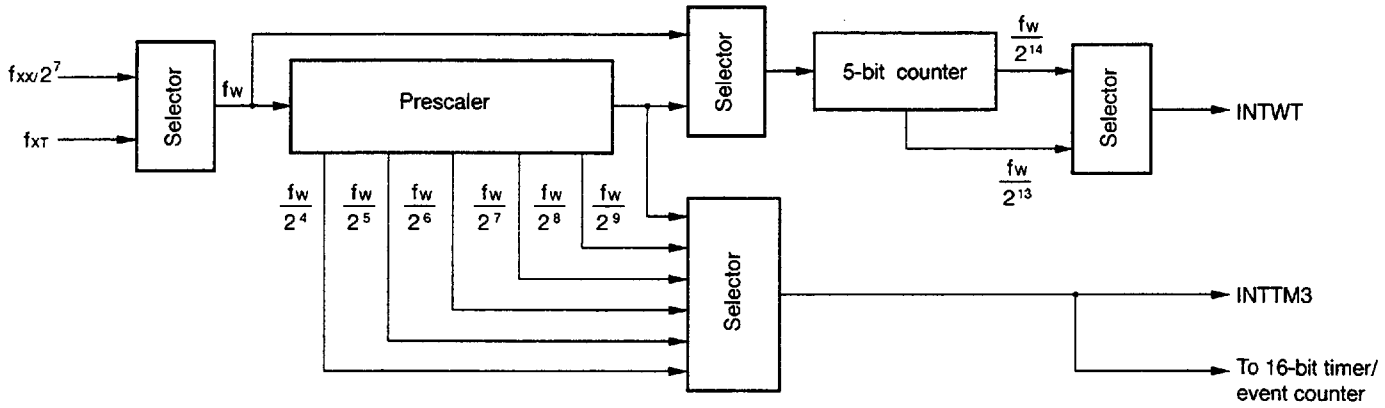
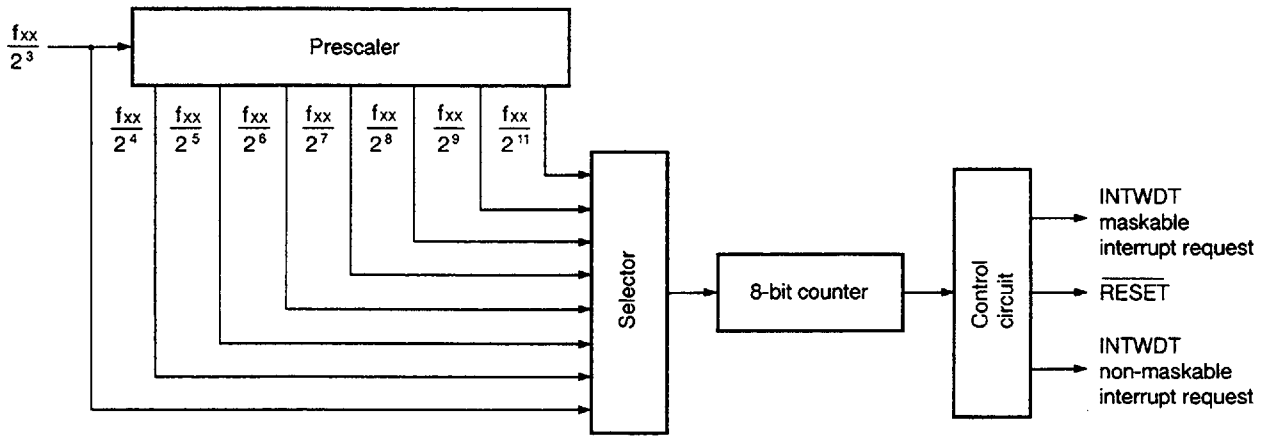


Figure 5-6. Watchdog Timer Block Diagram

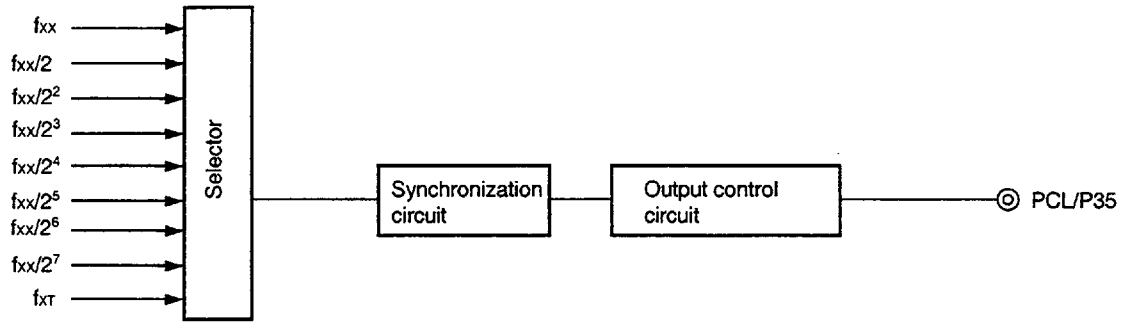


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)
- 32.768 kHz (at subsystem clock frequency of 32.768 kHz)

Figure 5-7. Clock Output Control Circuit Block Diagram

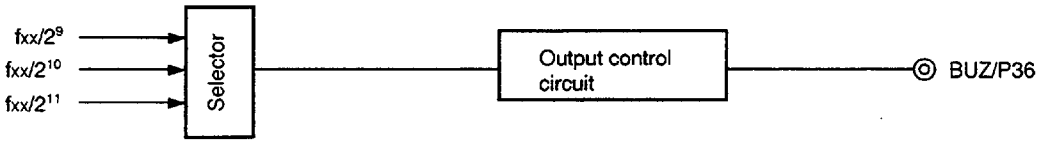


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-8. Buzzer Output Control Circuit Block Diagram



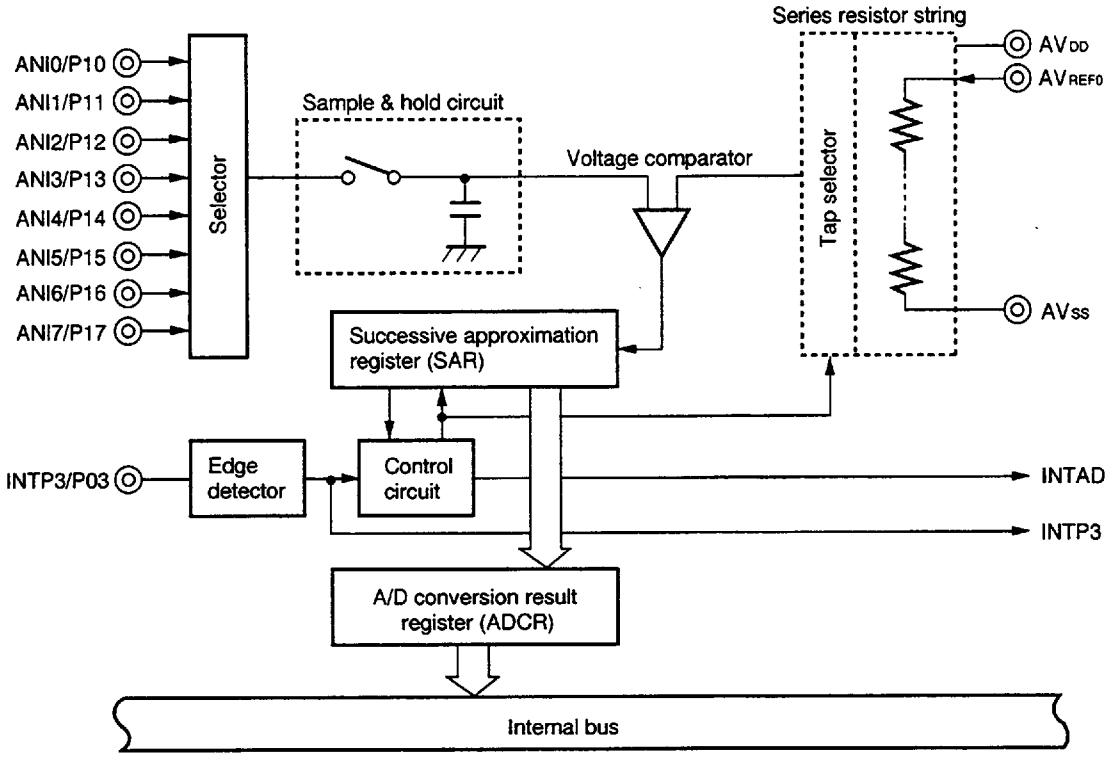
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-9. A/D Converter Block Diagram

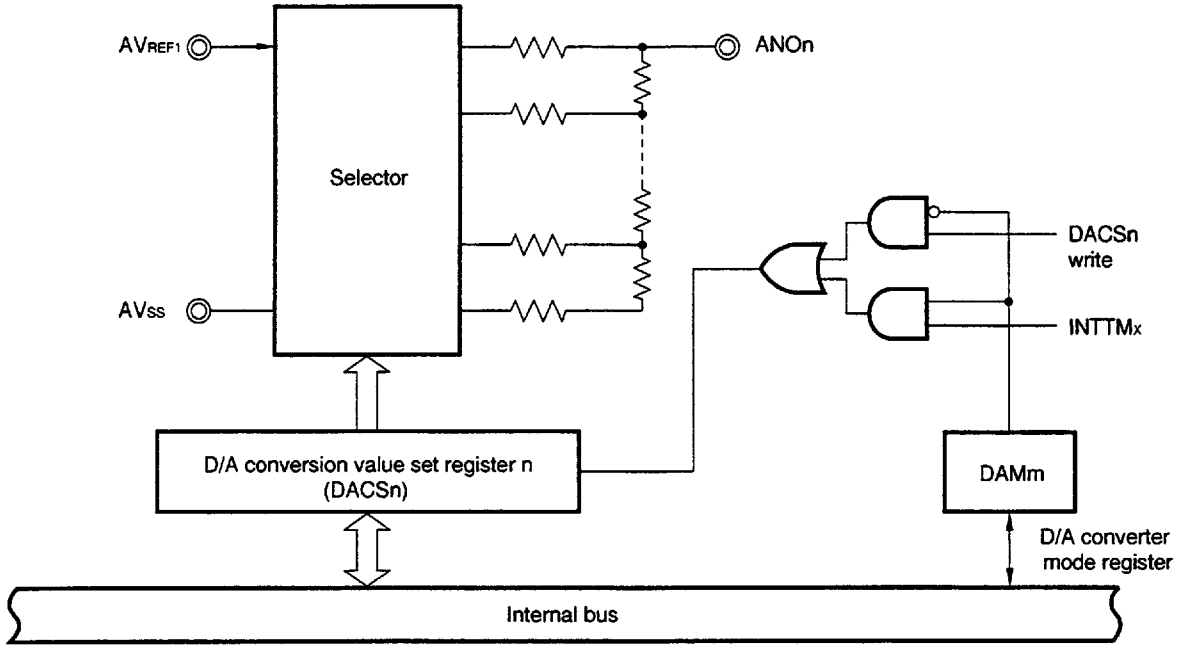


5.7 D/A Converter

The D/A converter consists of two 8-bit resolution channels.

The conversion method is the R-2R resistor ladder method.

Figure 5-10. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○(Starting bit MSB/LSB switching possible)	○(Starting bit MSB/LSB switching possible)	○(Starting bit MSB/LSB switching possible)
3-wire serial I/O mode with automatic data transmit/receive function	—	○(Starting bit MSB/LSB switching possible)	—
2-wire serial I/O mode	○(MSB first)	—	—
I^2C bus mode	○(MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	○(On-chip dedicated baud rate generator)

Figure 5-11. Serial Interface Channel 0 Block Diagram

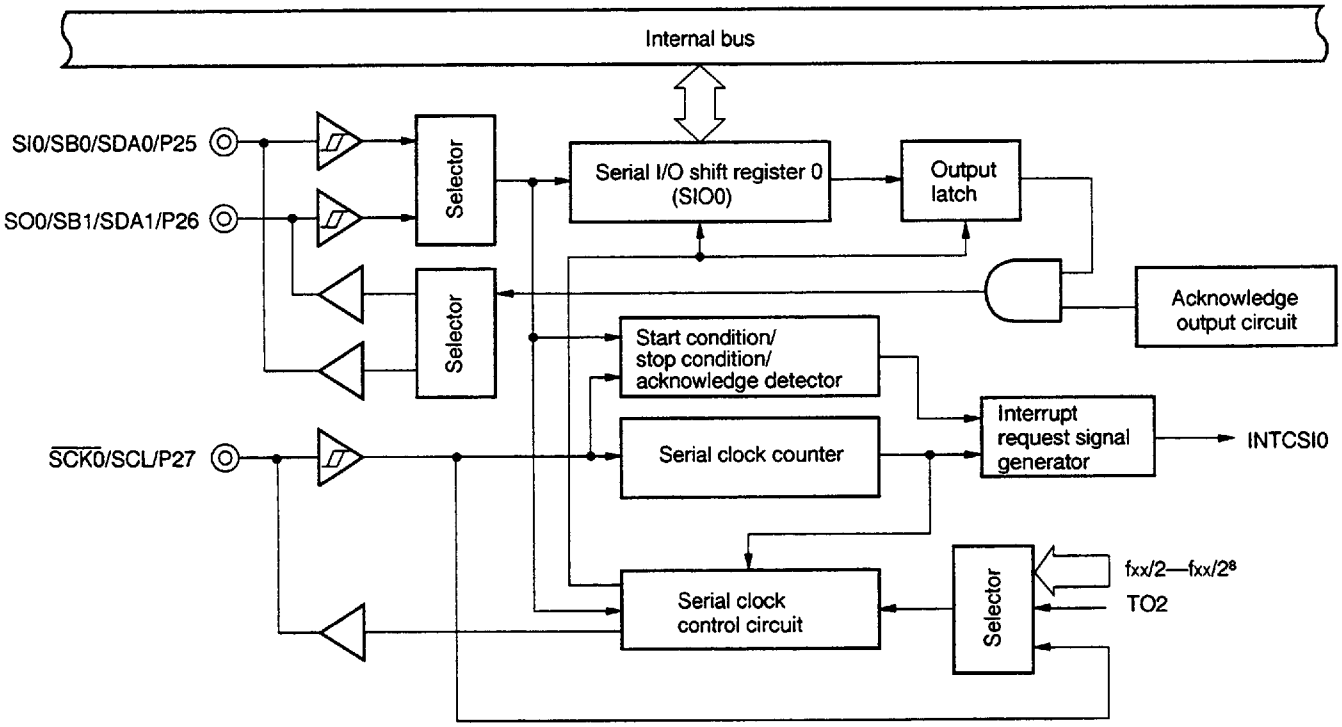


Figure 5-12. Serial Interface Channel 1 Block Diagram

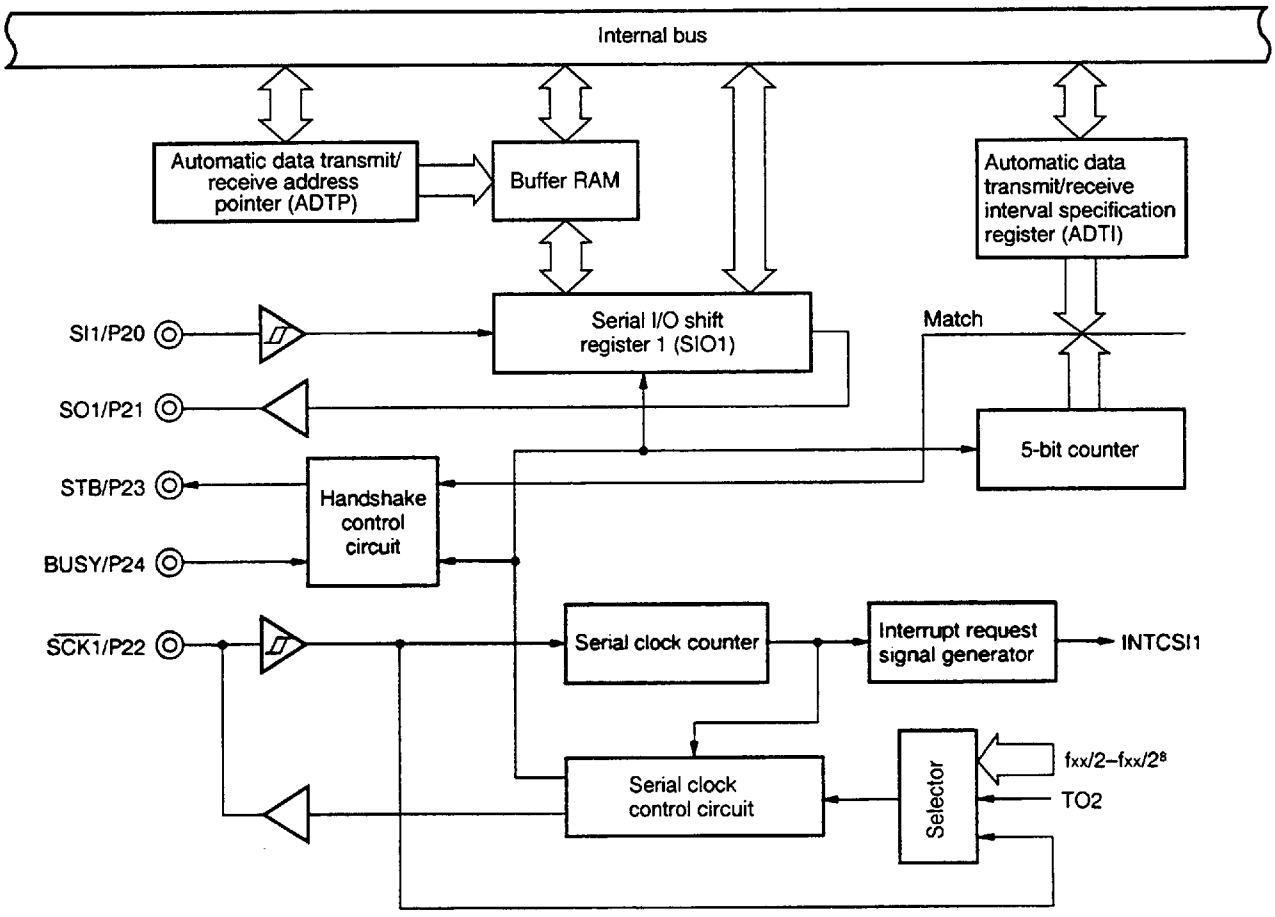
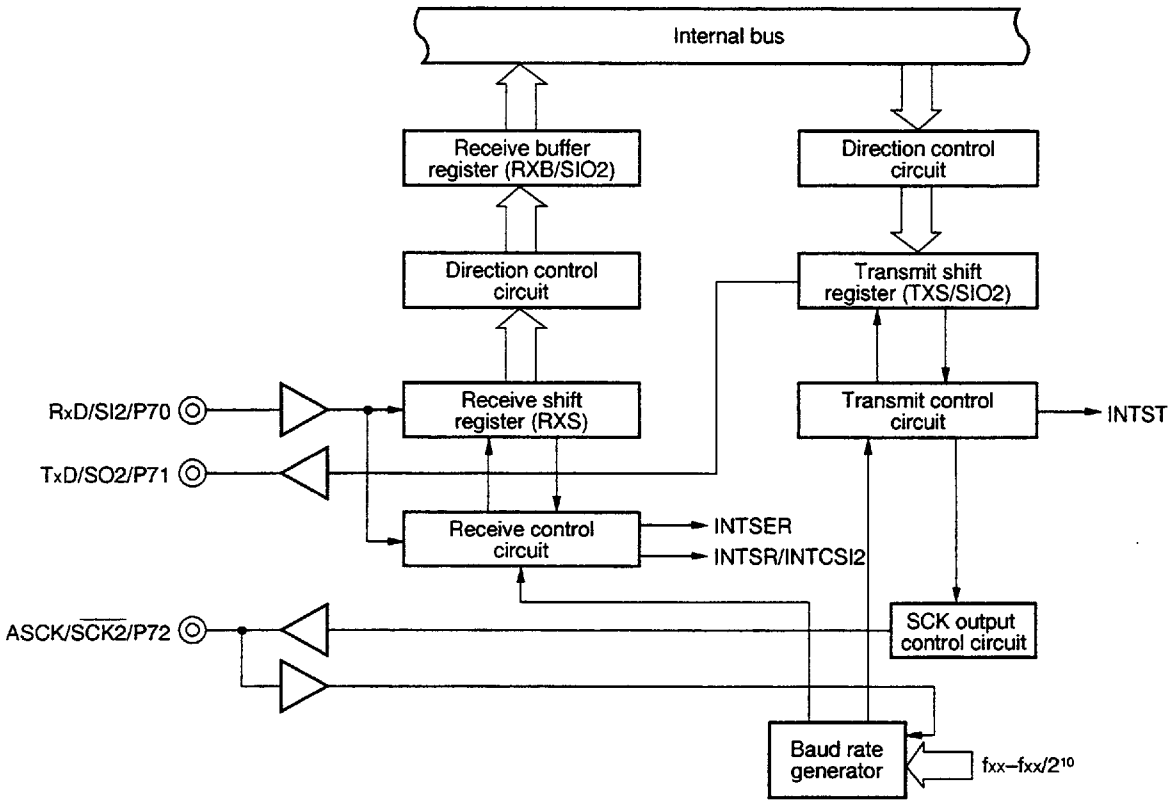


Figure 5-13. Serial Interface Channel 2 Block Diagram

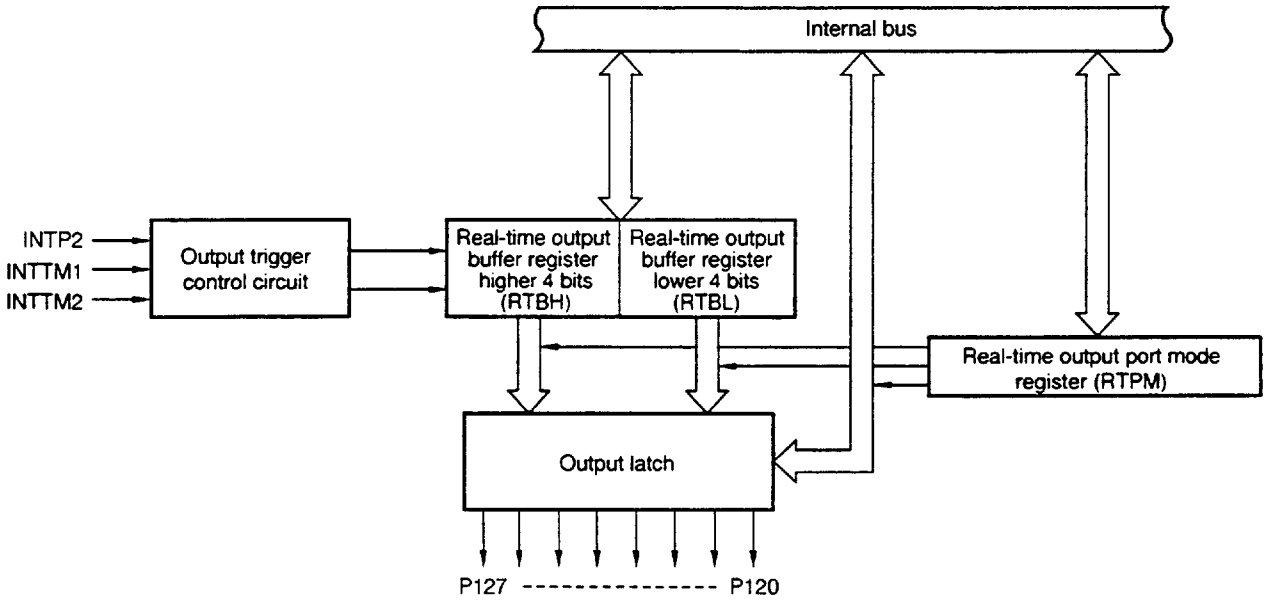


5.9 Real-time Output Port

Data set previously in the real-time output buffer is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is a real-time output function. Pins used to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

Figure 5-14. Real-time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 24 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupt : 22
- Software interrupt : 1

Table 6-1. List of Interrupt Factors

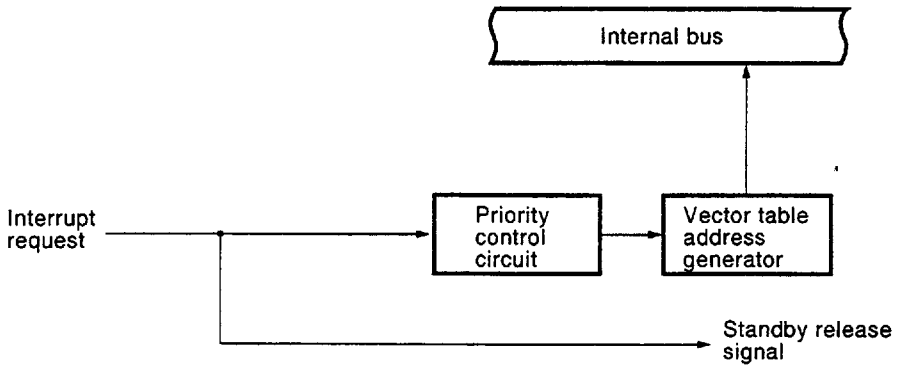
Interrupt Type	Default Priority (Note 1)	Interrupt Factor		Internal/ External	Vector Table Address	Basic Structure Type (Note 2)
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	Completion of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	Completion of serial interface channel 1 transfer		0016H	
	10	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	11	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	12	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	13	INTTM3	Reference interval signal from watch timer		001EH	
	14	INTTM00	Generation of matching signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of matching signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of matching signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of matching signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	Completion of A/D conversion		0028H	
	19	INTTM5	Generation of matching signal of 8-bit timer/event counter 5		002AH	
	20	INTTM6	Generation of matching signal of 8-bit timer/event counter 6		002CH	
Software	—	BRK	Execution of BRK instruction	Internal	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interruptions are generated at the same time. 0 is the highest order and 20 is the lowest order.

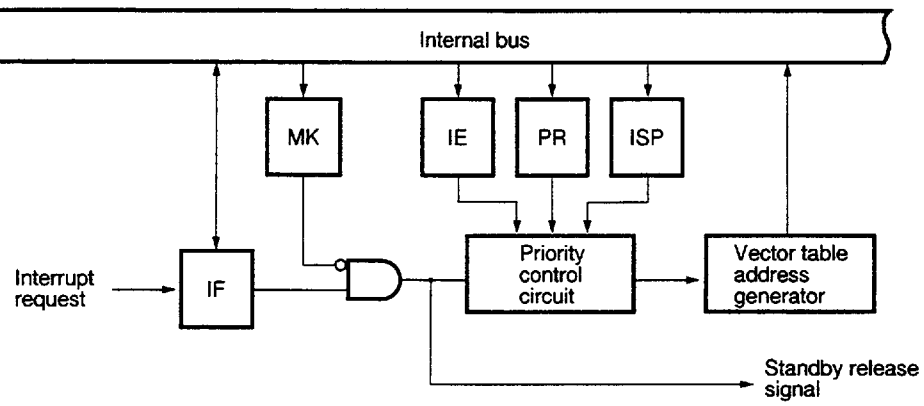
2. Basic structure types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

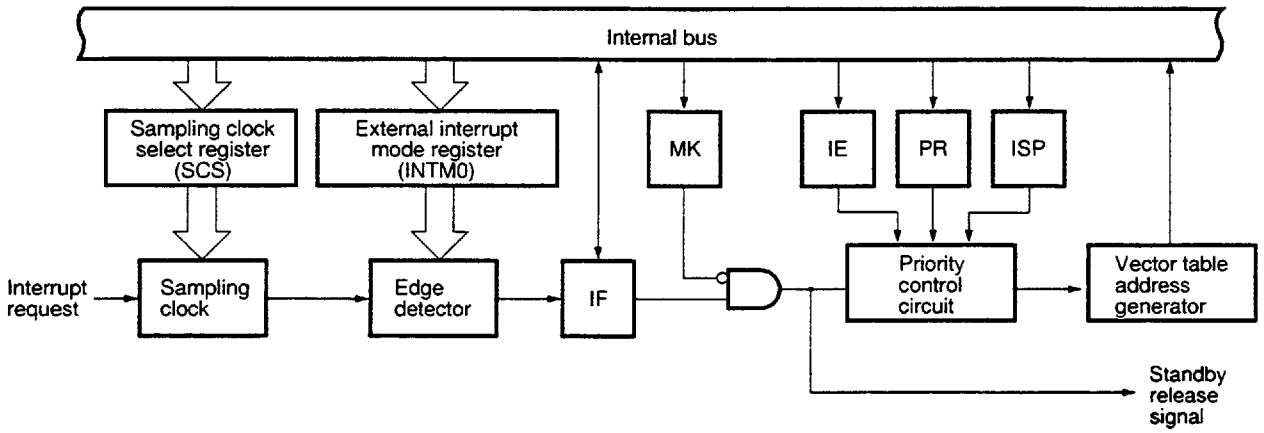
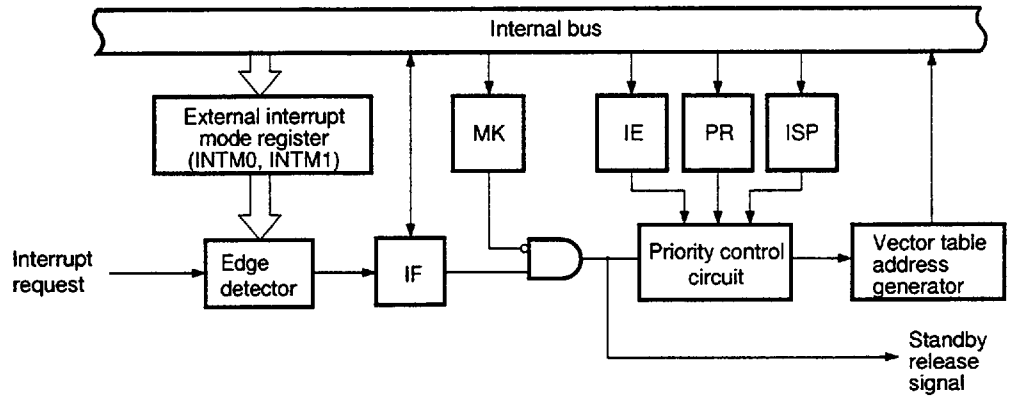
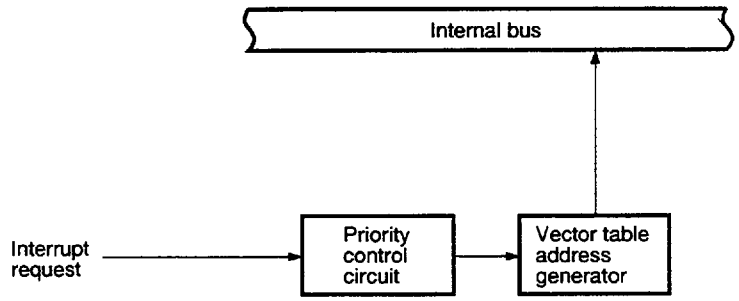


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
E : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

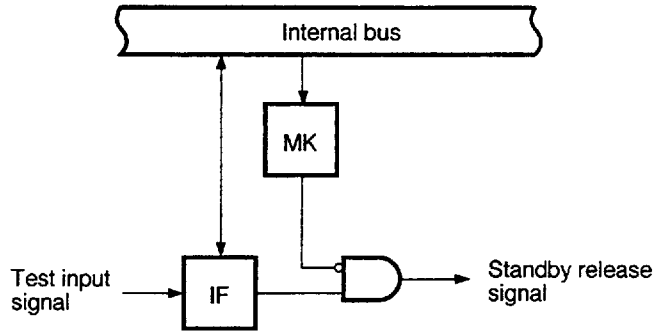
6.2 Test Functions

Table 6-2 shows the two test functions available.

Table 6-2. Test Input Factors

Test Input Factor		Internal/ External
Name	Trigger	
INTWT	Overflow of watch timer	Internal
INTPT4	Detection of falling edge of port 4	External

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR.

External devices connection uses ports 4 to 6 and port 8.

The external device expansion function has the following two modes:

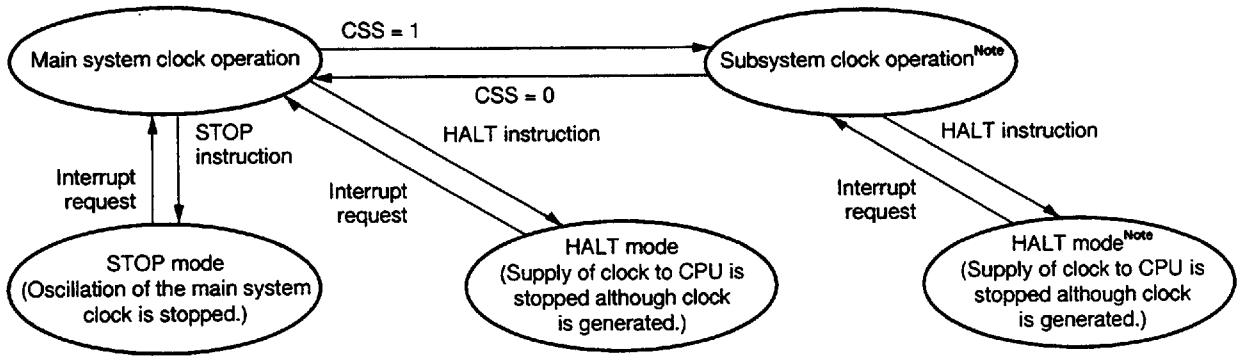
- Separate bus mode : External devices are connected by using an independent address bus and data bus. Because an external latch circuit is not necessary, this mode is effective for reducing the number of components and the mounting area on a printed wiring board.
- Multiplexed bus mode : External devices are connected by using a time-division multiplexed address/data bus. This mode is useful for reducing the number of ports used when external devices are connected.

8. STANDBY FUNCTION

The standby function intends to reduce current consumption. It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 8-1. Standby Function



Note Current consumption is reduced by shutting off the main system clock.
If the CPU is operating on subsystemclock, shut off the main system clock by setting MCC. You cannot use a STOP instruction.

Caution When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for the generation to be stable with the program first.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddrMOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP										DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	Saddr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS[Note1]

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			−0.3 to +7.0	V
	AV_{DD}			−0.3 to V_{DD}+0.3	V
	AV_{REF0}			−0.3 to V_{DD}+0.3	V
	AV_{REF1}			−0.3 to V_{DD}+0.3	V
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		−0.3 to V_{DD}+0.3	V
	V_{I2}	P60 to P63, P90 to P93	N-ch open-drain	−0.3 to +16	V
Output voltage	V_O			−0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS}−0.3 to AV_{REF0}+0.3	V
High-level output current	I_{OH}	1 pin		−10	mA
		P30-P37, P56, P57, P60 to P67, P90 to P96, P100 to P103, P120 to P127 total		−15	mA
		P01 to P06, P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P80 to P87, P130, P131 total		−15	mA
Low-level output current	I_{OL}[Note 2]	1 pin	Peak value	30	mA
			RMS	15	mA
		P50 to P55 total	Peak value	100	mA
			RMS	70	mA
		P56, P57, P60 to P63 total	Peak value	100	mA
			RMS	70	mA
		P30 to P37, P64 to P67, P90 to P96, P100 to P103, P120 to P127 total	Peak value	100	mA
			RMS	70	mA
		P20 to P27, P40 to P47, P80 to P87 total	Peak value	50	mA
			RMS	20	mA
		P01 to P06, P10 to P17, P70 to P72, P130, P131 total	Peak value	50	mA
			RMS	20	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Notes 1. For μPD78076Y and 78078Y (target specifications for μPD78074Y and 78075Y)

2. RMS should be calculated as follows: [RMS] = [Peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

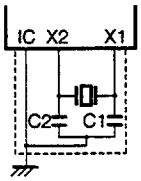
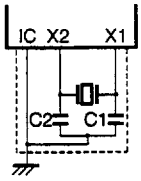
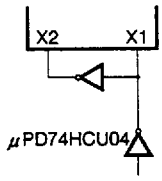
Remark The characteristics of the shared pins are the same as those of the port pins unless otherwise specified.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Other than measured pins : 0 V				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Other than measured pins : 0 V	P01 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131			15	pF
			P60 to P63, P90 to P93			20	pF

Remark The characteristics of the shared pins are the same as those of the port pins unless otherwise specified.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X) Note 1	V_{DD} = Oscillator voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC CHARACTERISTICS** for instruction execution time.

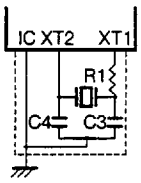
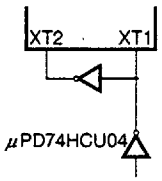
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation stabilization time **Note 2**	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) **Note 1**		32		100	kHz
		XT1 input high/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC CHARACTERISTICS** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage range MIN.

Cautions 1. When using the subsystem clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of Vss.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. The subsystem clock oscillation circuit is designed to be a circuit with a low amplification level, for low power consumption more prone to misoperation due to noise than that of the main system clock. Therefore, when using the subsystem clock, take special cautions for wiring methods.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, P90 to P93 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}−0.5		V_{DD}	V
				V_{DD}−0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			Note	0.9V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60 to P63, P90 to P93 (N-ch open-drain)	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			Note	0		0.1 V_{DD}	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1mA		V_{DD}−1.0			V
		I_{OH} = −100 μA		V_{DD}−0.5			V
Low-level output voltage	V_{OL1}	P50 to P57, P60 to P63, P90 to P93	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, at pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note For use as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remark The characteristics of the shared pins are the same as those of the port pins unless otherwise specified.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63, P90 to P93			80	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			−3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			−20	μA
	I_{LIL3}		P60 to P63, P90 to P93			−3 Note 1	μA
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				−3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63, P90 to P93		20	40	90	kΩ
Software pull-up resistor Note 2	R_2	V_{IN} = 0 V, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} ≤ 4.5 V	20		500	kΩ

Notes 1. When the pull-up resistors are not connected to P60 to P63 and P90 to P93 (specified by mask option), a low-level input current of −200 μA (MAX.) flows only for 1.5 clocks (without wait) after a read instruction has been executed to port 6 (P6), port mode register 6 (PM6), port 9 (P9), or port mode register 9 (PM9).
The current is −3 μA (MAX.) 1.5 clocks after the read instruction has been executed.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 5.5 V.

Remark The characteristics of the shared pins are the same as those of the port pins unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10 % Note 5		4.5	13.5	mA
			V_{DD} = 3.0 V ± 10 % Note 6		0.7	2.1	mA
			V_{DD} = 2.0 V ± 10 % Note 6		0.4	1.2	mA
		5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10 % Note 5		8.0	24.0	mA
			V_{DD} = 3.0 V ± 10 % Note 6		0.9	2.7	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 %		0.5	1.5	mA
			V_{DD} = 2.0 V ± 10 %		280	840	μA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10 %		0.65	1.95	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		32	64	μA
			V_{DD} = 2.0 V ± 10 %		24	48	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	55	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.0 V ± 10 %		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.0 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is unused	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.0 V ± 10 %		0.05	10	μA

Notes 1. The AV_{REF0}, AV_{REF1}, AV_{DD} currents and port current (including a current flowing in the on-chip pull-up resistor) are not included.
2. Operation with f_{XX} = f_X/2 (when oscillation mode select register is set to 00H)
3. Operation with f_{XX} = f_X (when oscillation mode select register is set to 01H)
4. When the main system clock is halted
5. Operating in high-speed mode (when the processor clock control register is set to 00H).
6. Operating in low-speed mode (when the processor clock control register is set to 04H).

Remarks 1. The characteristics of the shared pins are the same as those of the port pins unless otherwise specified.
2. f_{XX}: Main system clock frequency (f_X or f_X/2)
3. f_X: Main system clock oscillator frequency

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
					2.0		64	μs
			$f_{XX} = f_X$ Note 2	3.5 V≤ V_{DD} ≤ 5.5 V	0.4		32	μs
				2.7 V≤ V_{DD} < 3.5 V	0.8		32	μs
		Operating on subsystem clock			40	122	125	μs
TI00 input high/ low-level width	t_{TIH00}, t_{TIL00}	3.5 V≤ V_{DD} ≤ 5.5 V			$2/f_{sam}$ + 0.1 Note 3			μs
		2.7 V≤ V_{DD} < 3.5 V			$2/f_{sam}$ + 0.2 Note 3			μs
					$2/f_{sam}$ + 0.5 Note 3			μs
TI01 input high/ low-level width	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs
TI1, TI2, TI5, TI6 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V			0		4	MHz
					0		275	kHz
TI1, TI2, TI5, TI6 input high/ low-level width	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 5.5 V			100			ns
					1.8			μs
Interrupt input high/low-level width	t_{INTH}, t_{INTL}	INTP0		3.5 V≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1 Note 3			μs
				2.7 V≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2 Note 3			μs
					$2/f_{sam}$ + 0.5 Note 3			μs
		INTP1 to INTP6, KR0 to KR7		V_{DD} = 2.7 to 5.5 V	10			μs
					20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs

Notes 1. When oscillation mode select register is set to 00H

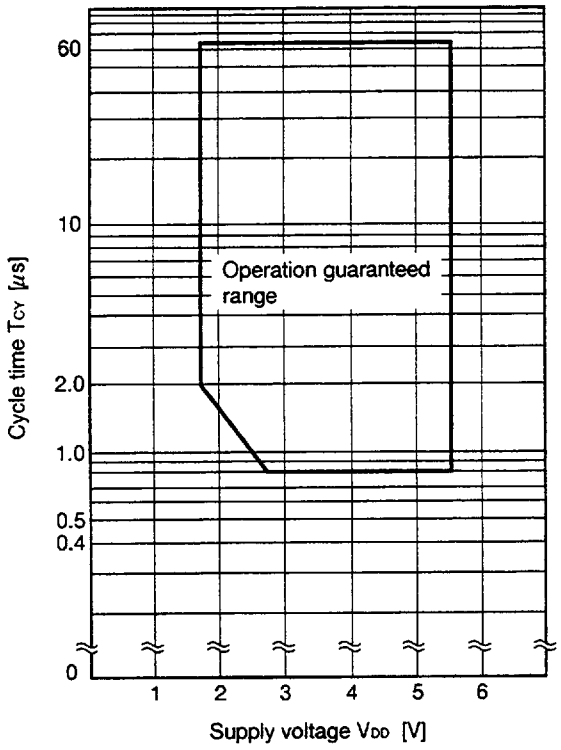
2. When oscillation mode select register is set to 01H

3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of f_{sam} is possible between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ and $f_{XX}/128$ (when N= 0 to 4).

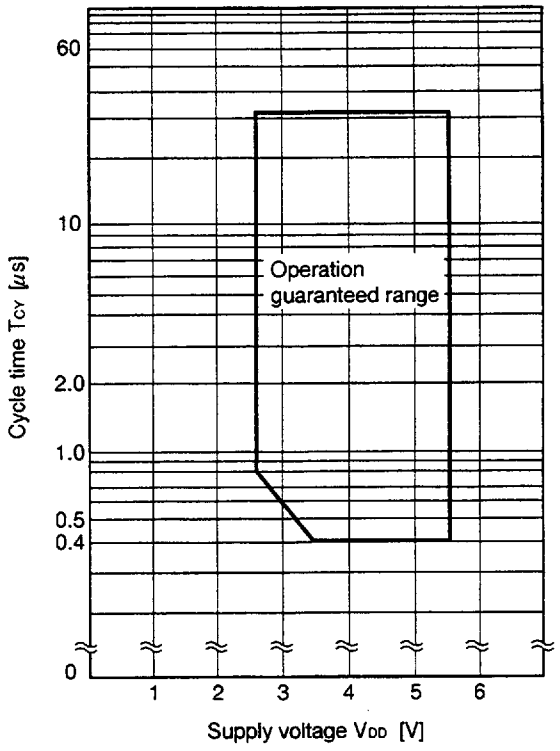
Remarks 1. f_{XX} : Main system clock frequency (f_X or $f_X/2$)

2. f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) READ/WRITE OPERATION

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to + 85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85+2n)t_{CY}$–80	ns
	t_{ADD2}			$(4+2n)t_{CY}$–100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}$–100	ns
	t_{RDD2}			$(2.85+2n)t_{CY}$–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2+2n)t_{CY}$–60		ns
	t_{RDL2}		$(2.85+2n)t_{CY}$–60		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY}$–50	ns
	t_{RDWT2}			$2t_{CY}$–60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY}$–60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15+2n)t_{CY}$	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85+2n)t_{CY}$–100		ns
Write data hold time	t_{WDH}	Load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85+2n)t_{CY}$–60		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ at external fetch	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$ – 20	$1.15t_{CY}$ + 40	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$+ 30	ns

Remarks 1. MCS : Oscillation mode select register bit 0
2. PCC2 to PCC0 : Processor clock control register bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates the number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to + 85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} − 80		ns
Address setup time	t_{ADS}		t_{CY} − 80		ns
Address hold time	t_{ADH}		0.4t_{CY} − 10		ns
Data input time from address	t_{ADD1}			(3+2n)t_{CY}−160	ns
	t_{ADD2}			(4+2n)t_{CY}−200	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(1.4+2n)t_{CY}−70	ns
	t_{RDD2}			(2.4+2n)t_{CY}−70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4+2n)t_{CY}−20		ns
	t_{RDL2}		(2.4+2n)t_{CY}−20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			t_{CY}−100	ns
	t_{RDWT2}			2t_{CY}−100	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			2t_{CY}−100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1+2n)t_{CY}	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.4+2n)t_{CY}−60		ns
Write data hold time	t_{WDH}	Load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4+2n)t_{CY}−20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		0.4t_{CY} −30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		1.4t_{CY} −30		ns
ASTB↑ delay time from $\overline{RD}$↑ at external fetch	t_{RDAST}		t_{CY} −10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		t_{CY} − 80	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		0.4t_{CY} − 30		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		t_{CY} − 60	t_{CY} + 60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY}+ 120	ns

Remarks 1. MCS : Oscillation mode select register bit 0
2. PCC2 to PCC0 : Processor clock control register bit 2 to bit 0
3. t_{CY} = T_{CY}/4
4. n indicates the number of waits.

(3) SERIAL INTERFACE (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF [Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	t_{KCY3}/2–160			ns
				t_{KCY3}/2–190			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2–50			ns
				t_{KCY3}/2–100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
						800	ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(v) I²C bus mode (SCL... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V_{DD} < 2.7 V	20			μs
				30			μs
SCL high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5}–160			ns
				t_{KCY5}–190			ns
SCL low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}–50			ns
				t_{KCY5}–100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK5}		2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} < 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI5}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO5}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL ↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}		V_{DD} = 2.0 to 5.5 V	400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0 and SDA1 output line.

(vi) I²C bus mode (SCL... External clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY6}			1000			ns
SCL high/low-level width	t_{KH6}, t_{KL6}	V_{DD} = 2.0 to 5.5 V		400			ns
				600			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI6}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL ↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}	V_{DD} = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}	V_{DD} = 2.0 to 5.5 V		500			ns
				800			
SCL rise/fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output line.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF [Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise/fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2–50			ns
			t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY9}–30		t_{KCY9}+30	ns
		2.0 V ≤ V_{DD} < 2.7 V	t_{KCY9}–60		t_{KCY9}+60	ns
			t_{KCY9}–90		t_{KCY9}+90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF [Note] V_{DD} = 2.0 to 5.5 V			300	ns
					500	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of SO1 output line.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}			400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF [Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise/fall time	t_{R12}, t_{F12}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function				1000	ns
						160	ns

Note C is the load capacitance of SO2 output line.

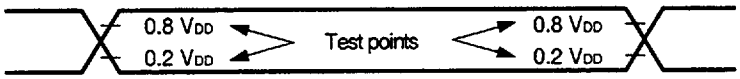
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
		2.0 V ≤ V_{DD} < 2.7 V			19531	bps
					9766	bps

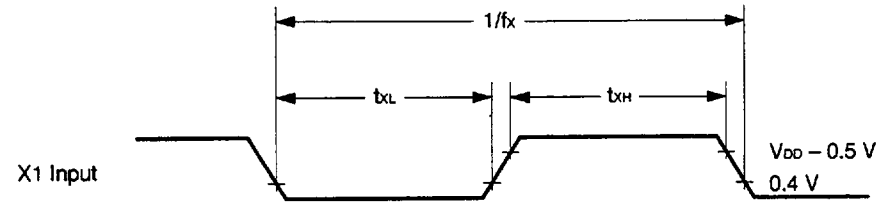
(iv) UART mode (External clock input)

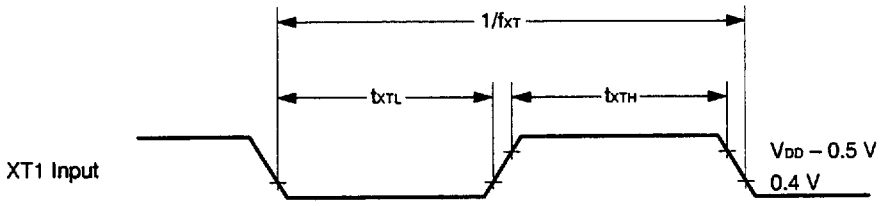
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
		2.0 V ≤ V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise/fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function			1000	ns
					160	ns

AC Timing Test Points (excluding X1, XT1 Inputs)

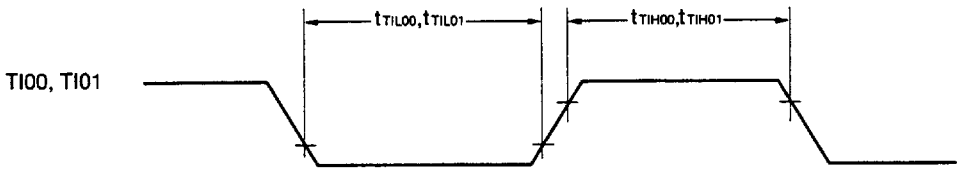


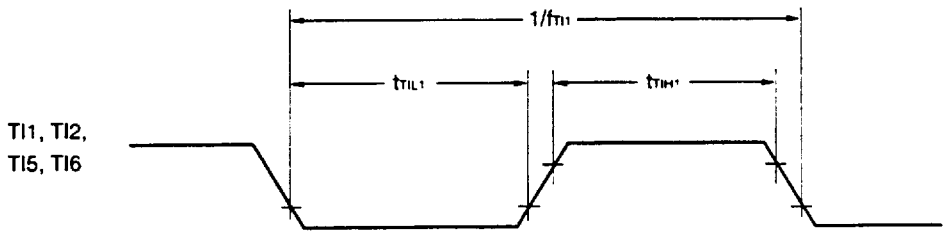
Clock Timing





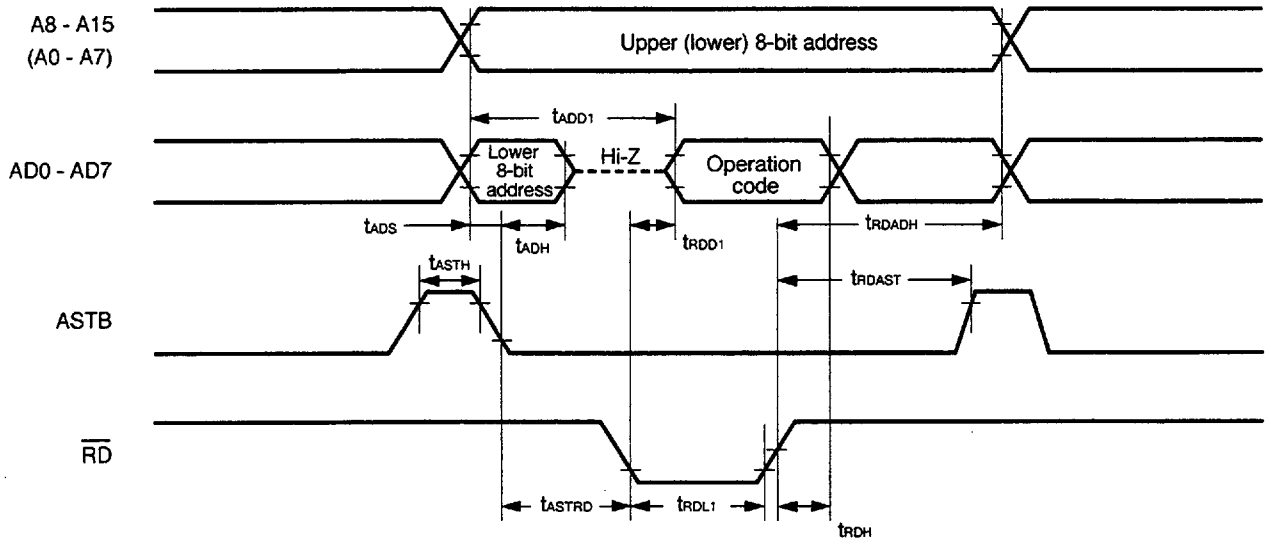
TI Timing





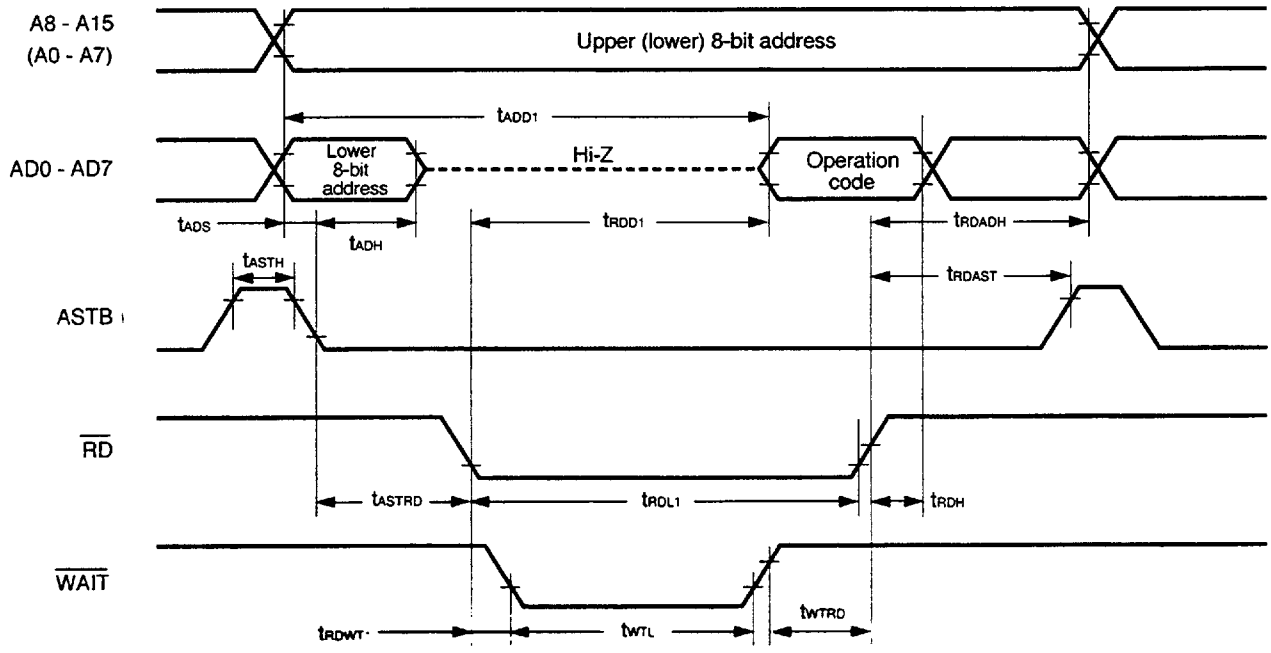
Read/Write Operation

External fetch (no wait) :



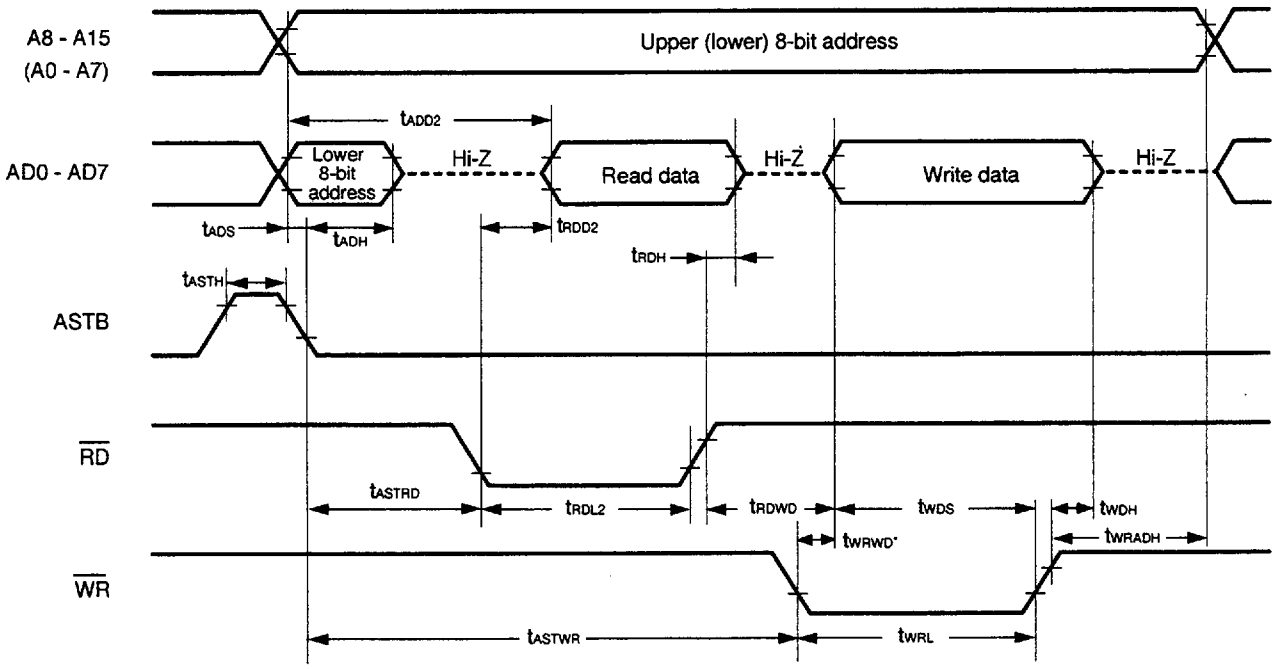
Remark ( ) is valid only in the separate bus mode.

External fetch (wait insertion) :



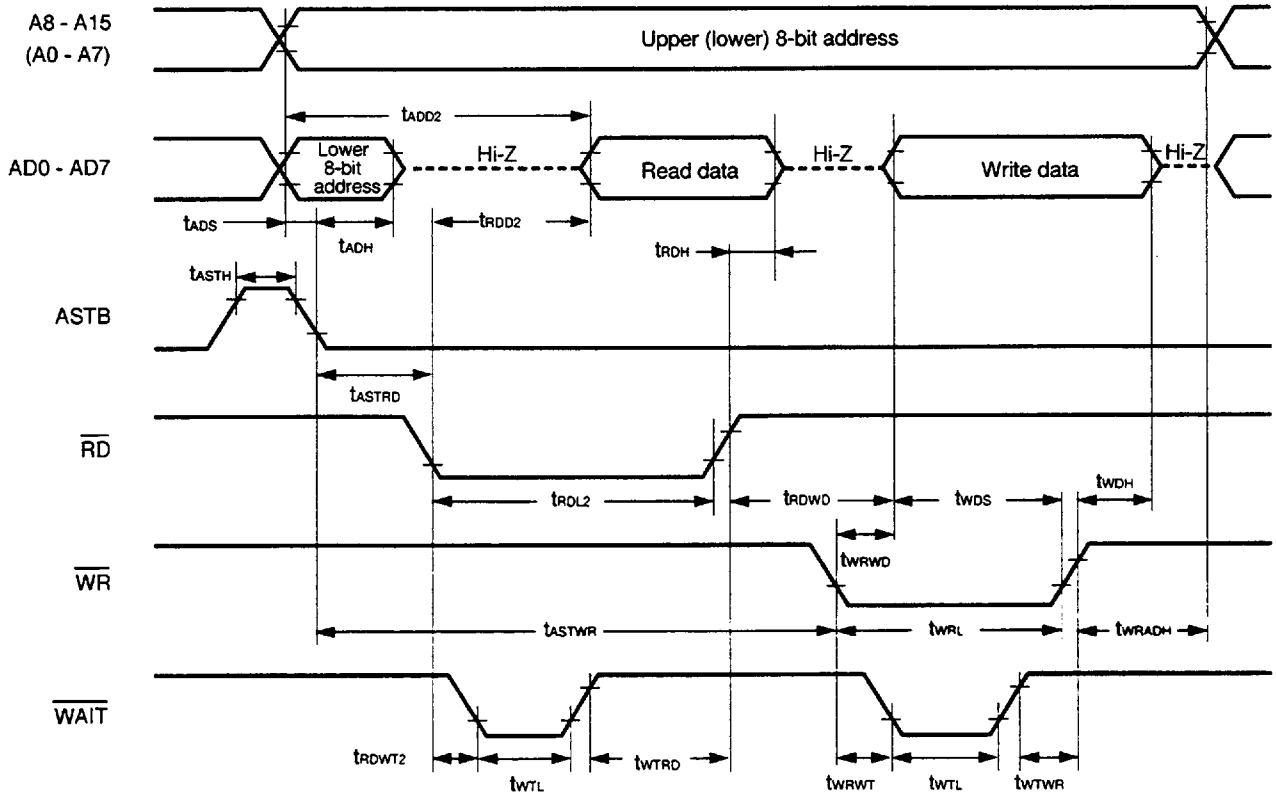
Remark ( ) is valid only in the separate bus mode.

External data access (no wait) :



Remark ( ) is valid only in the separate bus mode.

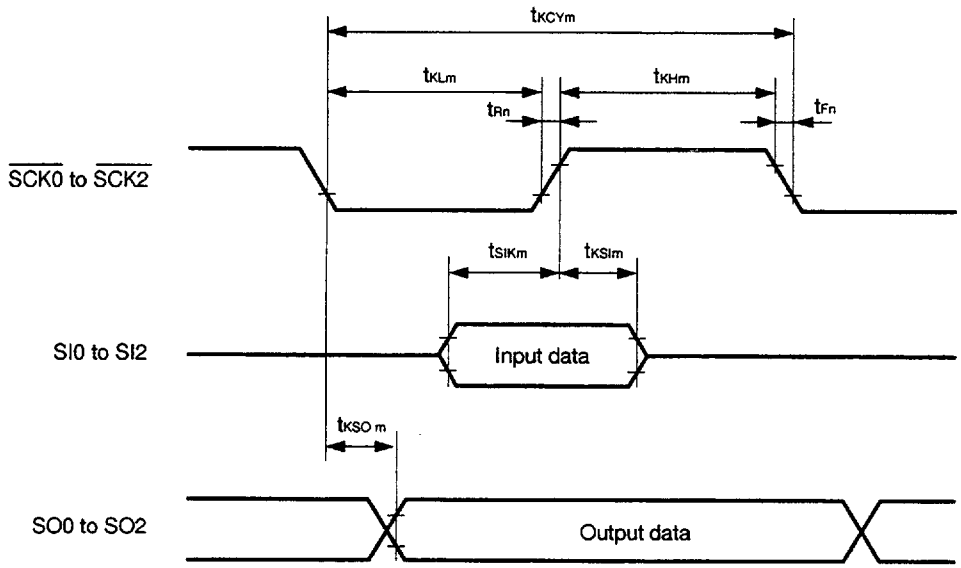
External data access (wait insertion) :



Remark ( ) is valid only in the separate bus mode.

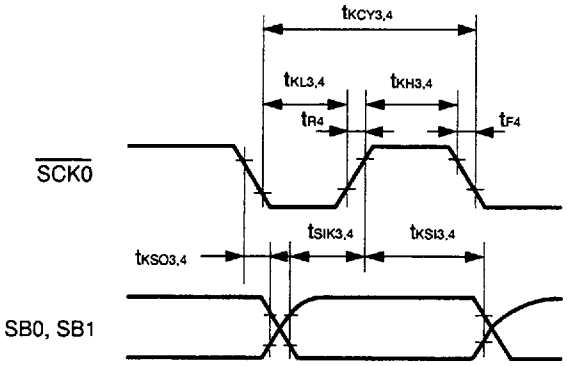
Serial Transfer Timing

3-wire serial I/O mode :

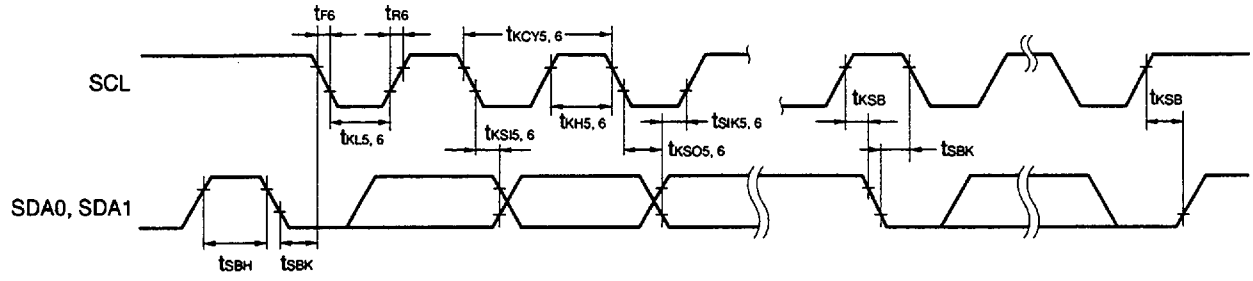


m = 1, 2, 7, 8, 11, 12
n =2, 8, 12

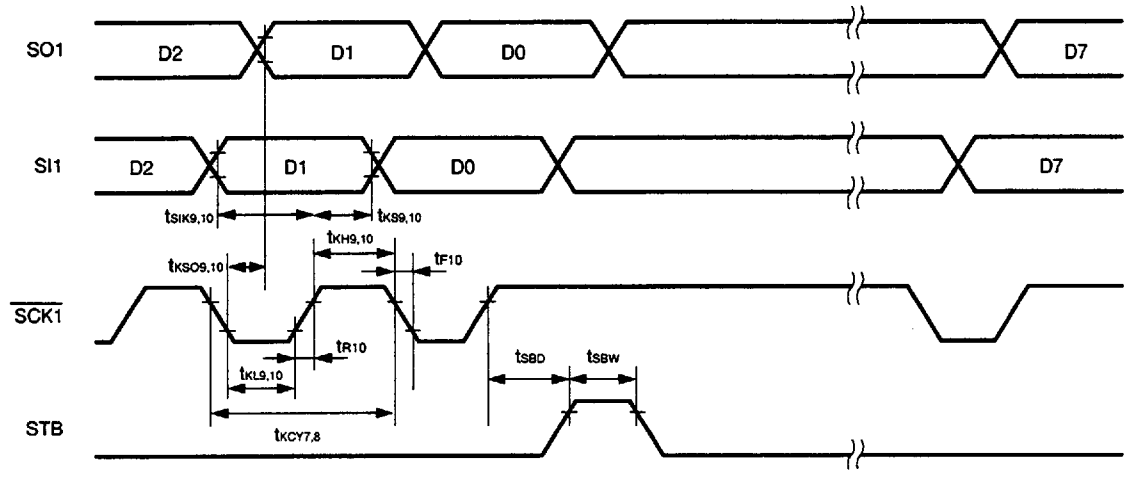
2-wire serial I/O mode :



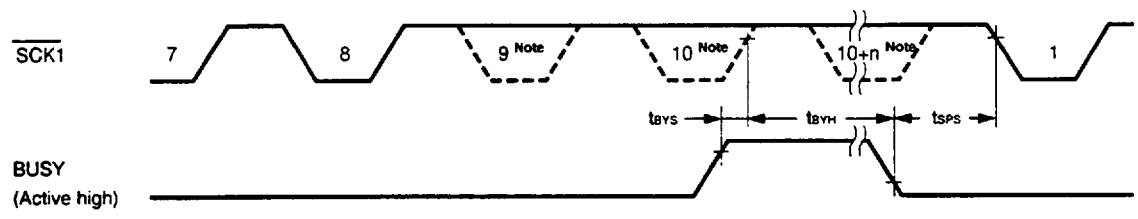
I²C bus mode :



3-wire serial I/O mode with automatic transmit/receive function :

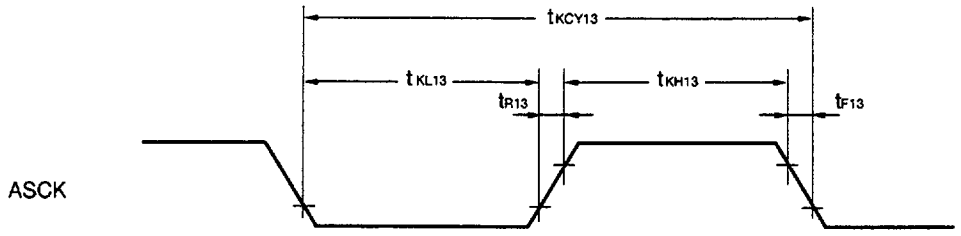


3-wire serial I/O mode with automatic transmit/receive function (busy processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input) :



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF0} < 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} ≤ 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		1.8		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AIREF0}		4	14		kΩ

Note Quantization error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Remarks 1. fxx: Main system clock frequency (fx or fx/2)
2. fx: Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2MΩ Note 1				1.2	%
		R = 4MΩ Note 1				0.8	%
		R = 10MΩ Note 1				0.6	%
Settling time		Note C=30pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			1.8 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	Note 2			10		kΩ
Analog reference voltage	AV_{REF1}			1.8		V_{DD}	V
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H Note 2		4	8		kΩ

Notes 1. R and C are D/A converter output pin load resistance and load capacitance, respectively.
2. Value for 1 D/A converter channel

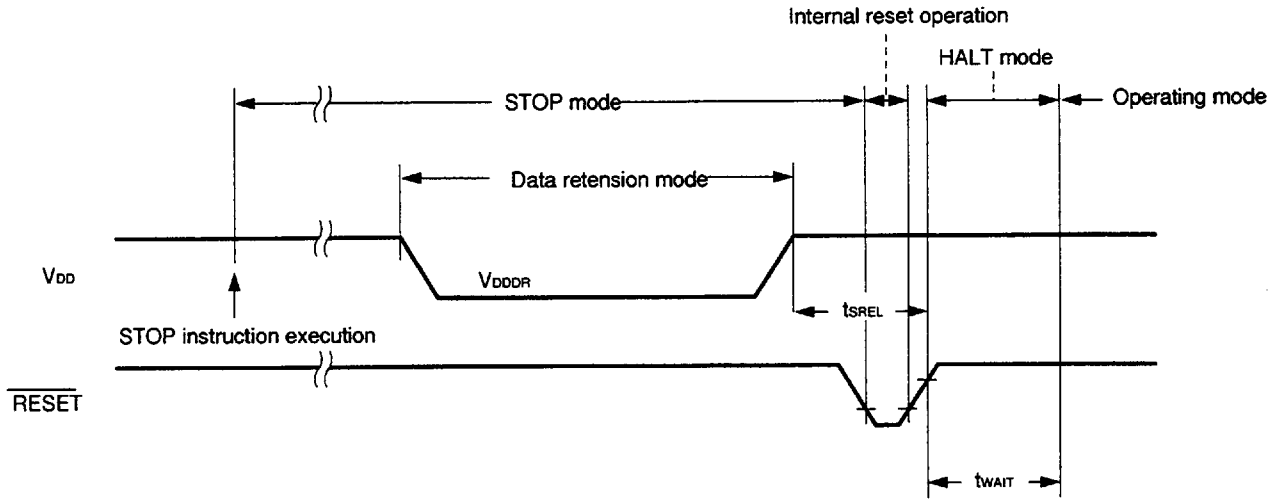
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to + 85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt		**Note**		ms

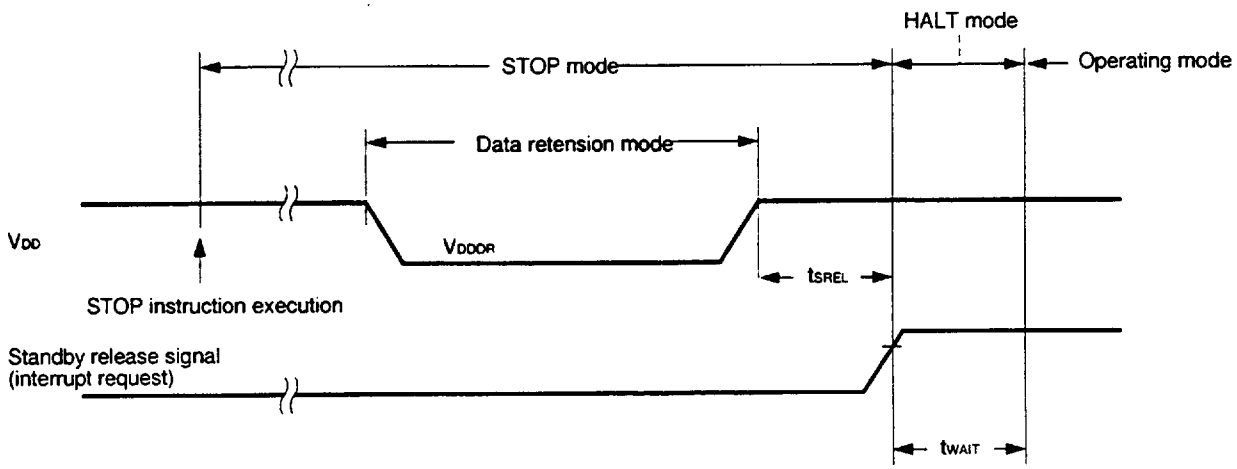
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of $2^{12}/fxx$ and $2^{14}/fxx$ to $2^{17}/fxx$ is possible.

Remark fxx: Main system clock frequency (fx or fx/2)
fx: Main system clock oscillation frequency

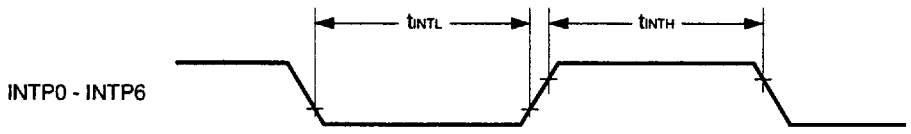
Data Retention Timing (STOP mode release by $\overline{RESET}$)



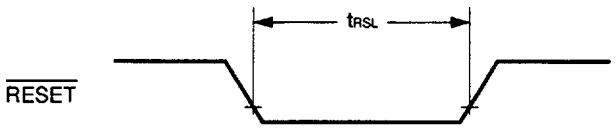
Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



Interrupt Input Timing

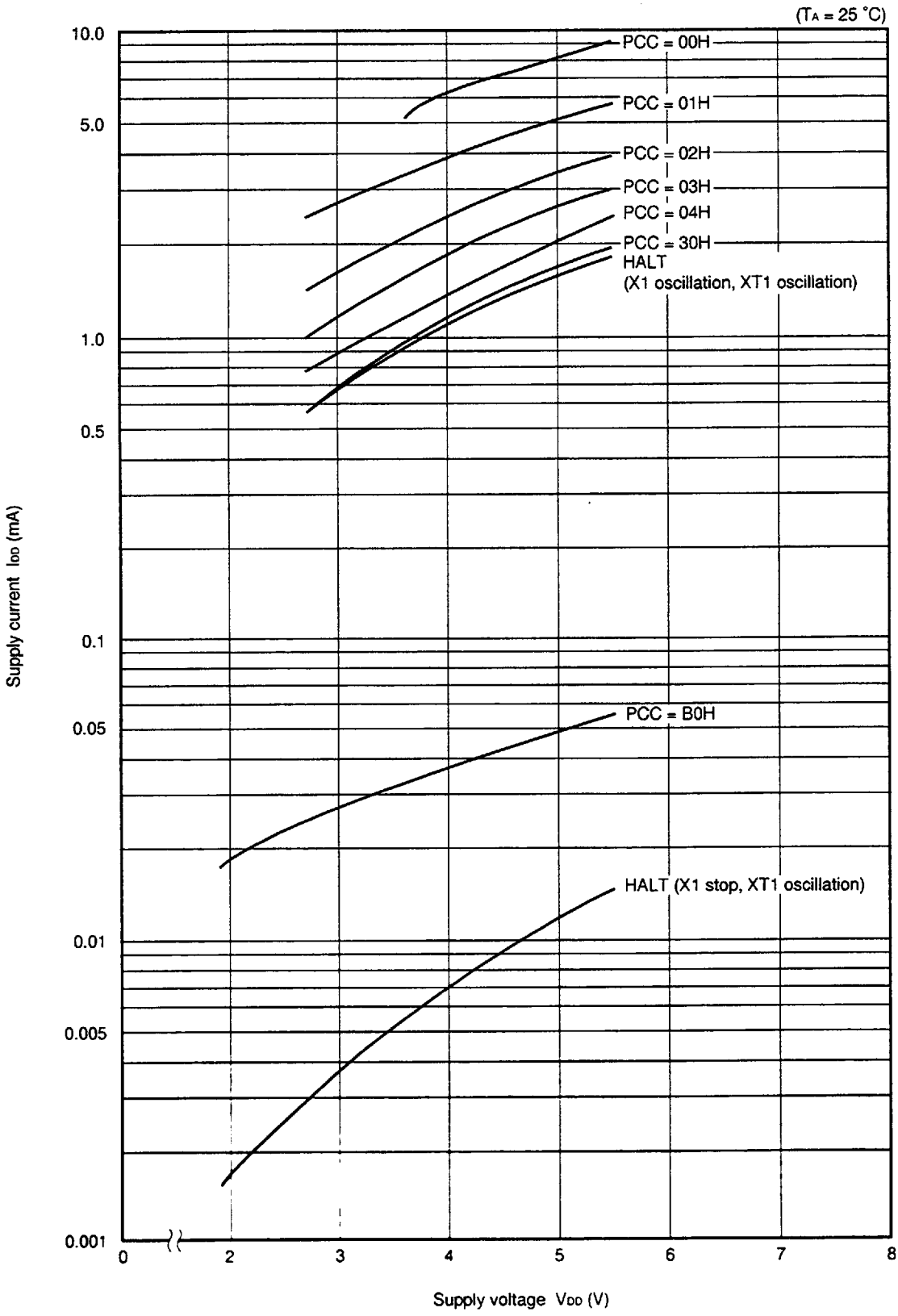


$\overline{\text{RESET}}$ Input Timing

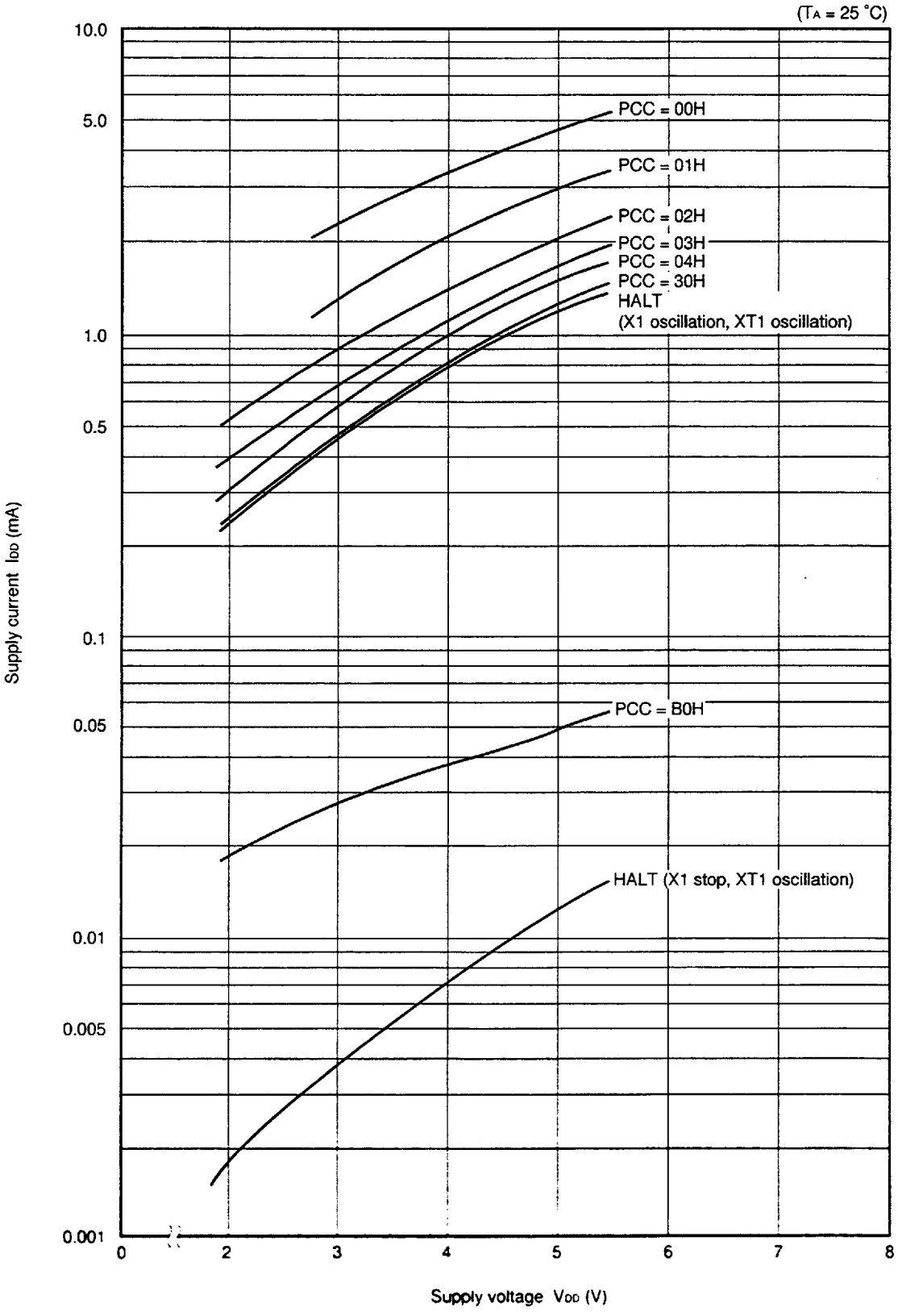


12. CHARACTERISTIC CURVES (REFERENCE VALUE)

I_{DD} vs V_{DD} ($f_X = f_{XX} = 5.0$ MHz)

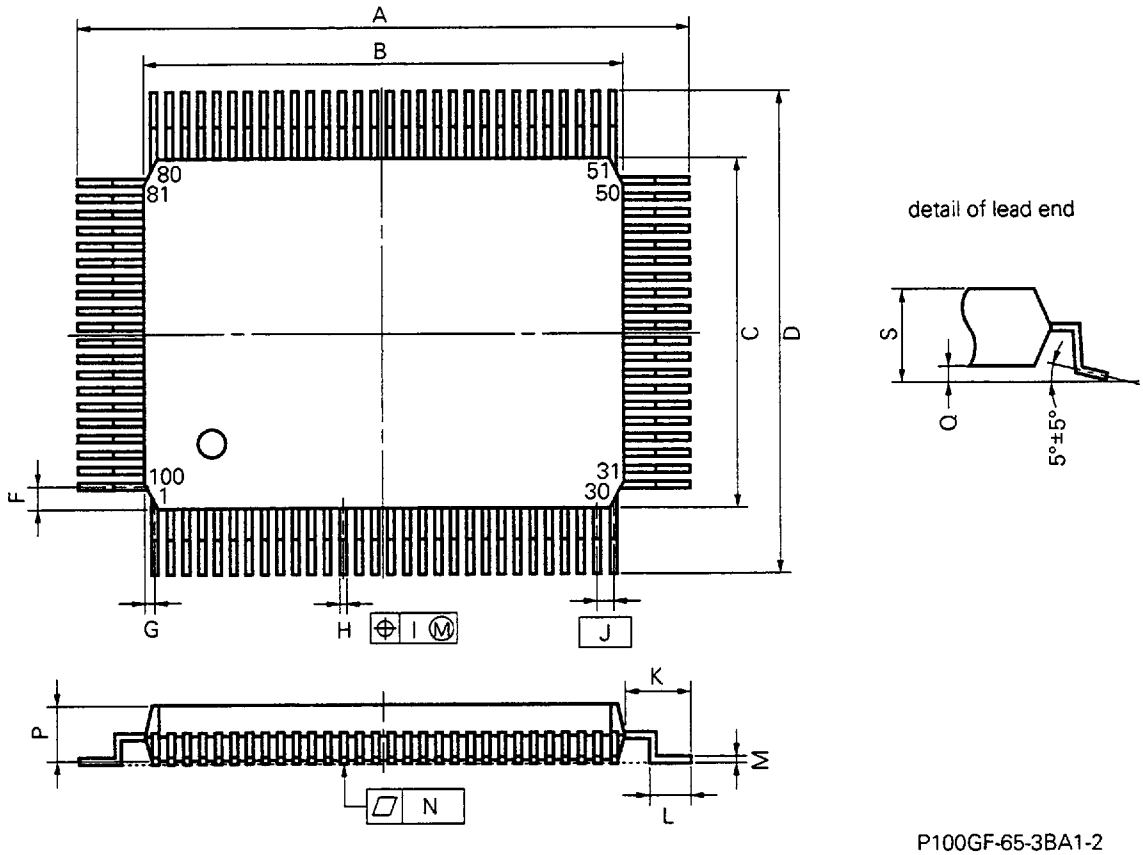


I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



13. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark The shape and material of the ES product is the same as the mass produced product.

14. RECOMMENDED SOLDERING CONDITIONS

μPD78076Y and 78078Y should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (IEI-1207)**.

For soldering methods and conditions other than those recommended below, consult our sales personnel.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD78076YGF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78078YGF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: twice max. <Precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: twice max. <Precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Soldering bath temperature: 260°C max., Duration: 10 sec. max., Number of times: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Cautions 1. Use of more than one soldering methods should be avoided (except in the case of pin part heating).

2. The soldering conditions for μPD78074Y and 78075Y are undefined, since they are still under development.

APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for system development using the μPD78074Y, 78075Y, 78076Y and 78078Y.

Language Processing Software

RA78K/0[Notes 1, 2, 3]	Assembler package used in common for the 78K/0 series
CC78K/0[Notes 1, 2, 3]	C compiler package used in common for the 78K/0 series
DF78078[Notes 1, 2, 3]	Device file used for the μPD78078 subseries
CC78K/0–L[Notes 1, 2, 3]	C compiler library source file used in common for the 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P078GF PA-78P078KL-T	Programmer adapter connected to the PG-1500
PG-1500 controller[Notes 1, 2]	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator used in common for the 78K/0 series
IE-78000-R-BK	Break board used in common for the 78K/0 series
IE-78078-R-EM	Evaluation emulation board for the μPD78078 subseries
EP-78064GC-R EP-78064GF-R	Emulation probe used in common for the μPD78064 subseries
EV-9200GF-100	Socket mounted on the user system board prepared for 100-pin plastic QFP
EV-9900	Tool used for removing the μPD78P078YKL-T from the EV-9200GF-100.
SM78K0[Notes 4, 5]	System simulator used in common for the 78K/0 series
SD78K/0[Notes 1, 2]	Screen debugger for the IE-78000-R
DF78078[Notes 1, 2, 4, 5]	Device file used for the μPD78078 subseries

Real-Time OS

RX78K/0[Notes 1, 2, 3]	Real-time OS used for the 78K/0 series
MX78K0[Notes 1, 2, 3]	OS used for the 78K/0 series

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 5]	Fuzzy knowledge data creating tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. Based on PC-9800 series (MS-DOS™)
2. Based on IBM PC/AT™ (PC DOS™)
3. Based on HP9000 series 300™, HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)
4. Based on PC-9800 series (MS-DOS + Windows™)
5. Based on IBM PC/AT (PC DOS + Windows)

Remarks 1. For development tools supplied by third-party manufacturers, refer to **78K/0 series Selection Guide** (IF-1185).
2. Use the RA78K/0, CC78K/0, SM78K0 and SD78K/0 in combination with the DF78078.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document	Document No.	
	Japanese	English
μPD78078, 78078Y Subseries User's Manual	IEU-874	IEU-1396
78K/0 Series User's Manual-Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Table	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—
μPD78078Y Subseries Special-Function Register Table	IEM-5601	—
78K/0 Series Application Note-Fundamental (III)	IEA-767	10182E

Documents on Development Tools (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programing Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	To be prepared
PG-1500 Controller IBM PC Series (PC-DOS) Base		EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		EEU-978	EEU-1504
EP-78064		EEU-934	EEU-1522
SM78K0 System Simulator	Reference	EEU-5002	To be prepared
SM78K Series System Simulator	External Parts User-open Interface Specification	U10092J	To be prepared
SD78K/0 Screen Debugger	Introduction	EEU-852	—
PC-9800 Series (MS-DOS) Base	Reference	EEU-816	—
SD78 K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Base	Reference	EEU-993	EEU-1413

Caution The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

Documents on Embeded Software (User's Manuals)

Document		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
78K/0 Series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –	MEI-604	—

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