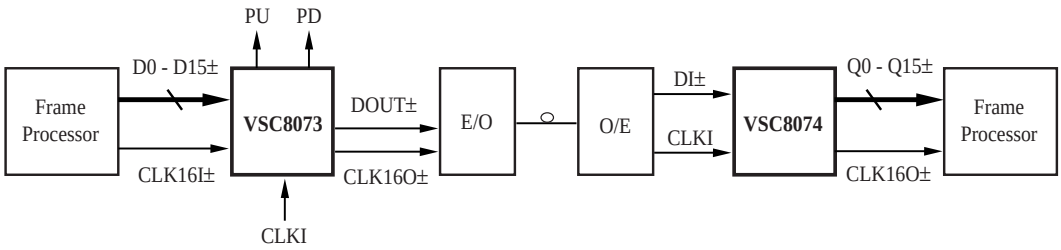
Datasheet
VSC8074

10Gb/s 16-Bit Demultiplexer for STS-192 and STM-64 Applications

Features

- Performs 1:16 DEMUX Between 10Gb/s High-Speed Signal and 16 622Mb/s Low-Speed Signals
- Fully Differential Low-Speed Interface
- Industry Standard –5.2V Power Supply
- 50Ω Output Drive Capability
- Internal Input Terminations
- Industry-Standard 80-Pin PQFP Package
- Proven E/D Mode GaAs Technology
- Supports STS-192 SONET Applications

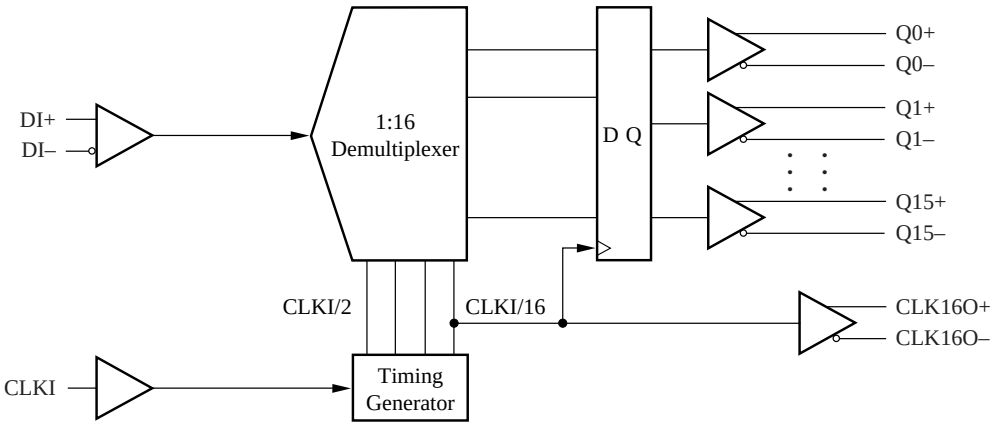
Typical System Block Diagram



General Description

The VSC8074 accepts a differential 10Gb/s serial input data stream (**DI±**). Using a 10GHz clock input (**CLKI**), the high-speed data stream is demultiplexed into 16 differential 622Mb/s parallel outputs (**Q0-Q15±**). In addition to the data outputs, a differential 622MHz clock output (**CLK16O±**) is provided. The device operates using a –5.2V power supply and is packaged in a thermally-enhanced, standard plastic package.

Functional Block Diagram



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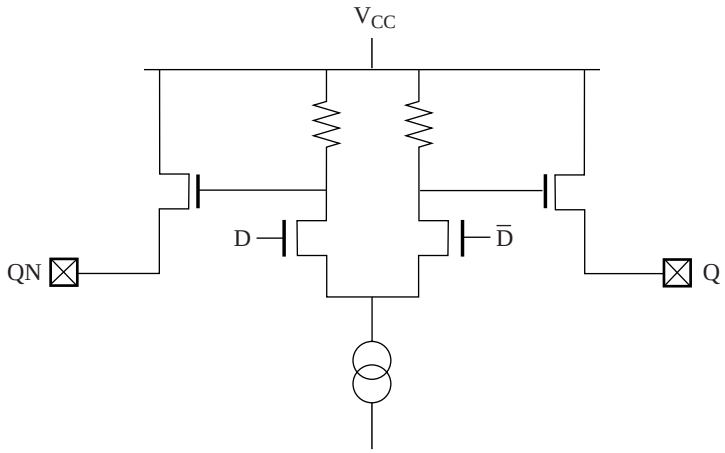
Functional Description

Low-Speed Interface

The deserialized data outputs (**Q0-Q15±**) and divided clock (**CLK16O±**) are ECL-compatible outputs and should be terminated with 50Ω resistors to V_{TT}. These low-speed interfaces are realized using ECL levels as defined in Table 2. The recommended load configuration for the outputs is 50Ω. The internal schematic for the low speed outputs is shown in Figure 1.

Figure 1: Low-Speed ECL- Output Driverr



High-Speed Interface

Serial data inputs (**DI±**) and bit rate clocks (**CLKI**) are internally terminated with 50Ω resistors to V_{CC}. The internal input receiver and termination schemes for the data and clock inputs are shown in Figures 2 and 3, respectively. The high-speed differential data in (**DI±**) requirements appear in Table 3. The high-speed clock input (**CLKI**) requirements appear in Table 4.

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Figure 2: High-Speed Data Input Receiver

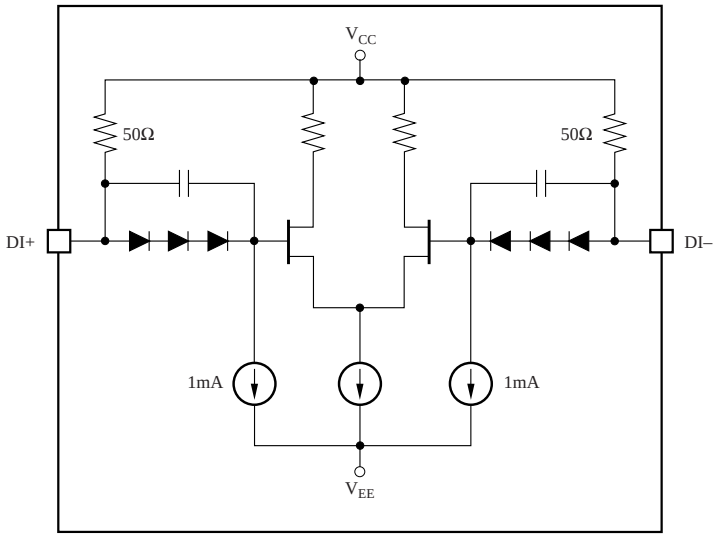
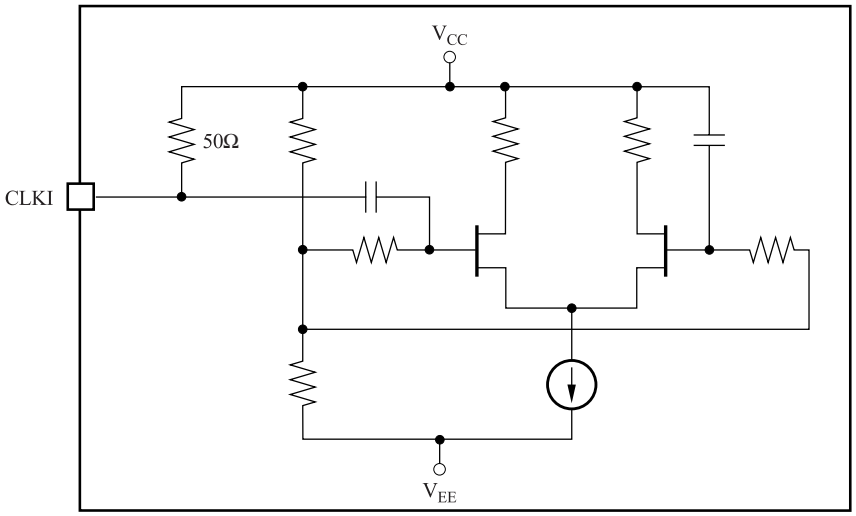


Figure 3: High-Speed Clock Input Receiver



Power Supply

The device is typically operated from a single –5.2V supply (V_{EE}). V_{CC} is typically held at ground potential. Decoupling of the power supply is a critical element in maintaining proper operation of the part. It is recommended that V_{CC} be decoupled using a 0.1µF and a 0.01µF capacitor placed in parallel on each V_{CC} pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors previously mentioned. Recommended capacitors are low-inductance, ceramic SMT X7R devices. A 0603 package should be used for the 0.1µF capacitor; the 0.01µF and 0.001µF capacitors can be either 0603 or 0403 packages.

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Table 1: AC Timing Characteristics (Over Recommended Operating Conditions)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$t_{CLK16OR}$, $t_{CLK16OF}$	CLK16O Rise and Fall Times	—	200	350	ps	See Figure 7, 20% to 80%
t_{CLKI}	High-Speed Input Clock Period	—	100.46	—	ps	—
t_{LCLK}	Low-Speed Clock Period	—	1607	—	ps	—
DC_{HSCLK}	Duty Cycle of High-Speed Clock In	40	—	60	%	—
DC_{LSCLK}	Duty Cycle of Low-Speed Clock In	40	—	60	%	—
tDIR, tDIF	Serial Data Rise and Fall Times	—	30	35	ps	See Figure 7, 20% to 80%
t_{QR}, t_{QF}	Parallel Data Out Rise and Fall Times	—	300	—	ps	See Figure 7
t_{QS}	Output Data Valid Time Before CLK16O	300	—	—	ps	See Figure 4
t_{QH}	Output Data Valid Time After CLK16O	300	—	—	ps	See Figure 4
t_{PM}	Phase Margin	150	180	—	degrees	At (2^{31}– 1) PRBS. See Figure 6.

Figure 4: VSC8074 AC Timing Waveforms

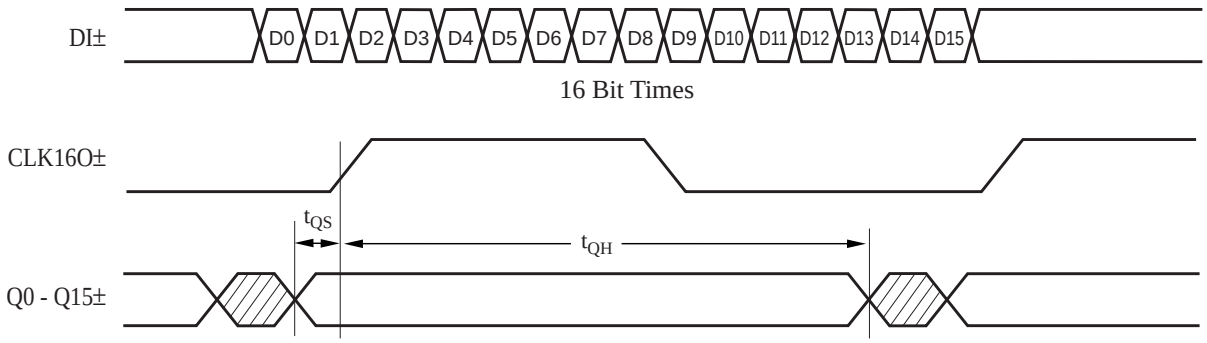

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Figure 5: Input Timing

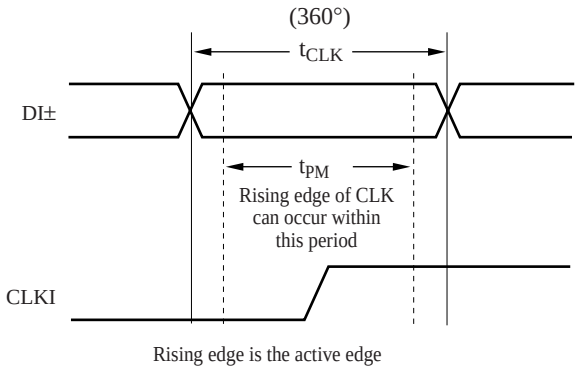


Figure 6: Data Input Sensitivity vs. Phase Margin

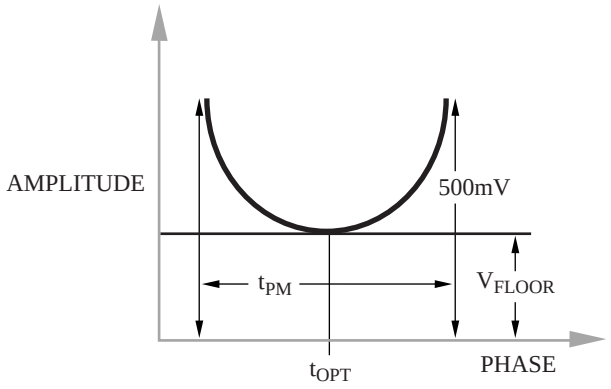
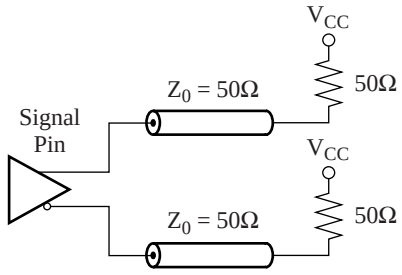
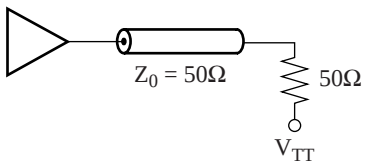


Figure 7: Parametric Measurement Information

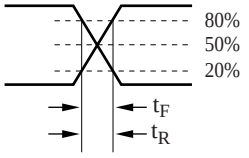
Parametric Test Load Circuit



Serial Output Load



ECL Output Load



Output Rise and Fall Times

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DC Characteristics *(Over Recommended Operating Conditions)*

Table 2: ECL Inputs/Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH Voltage	–1100	—	–700	mV	Measure into 50Ω Load. See Figure 7.
V_{OL}	Output LOW Voltage	-2V	—	–1620	mV	50Ω to V_{TT} Load

Table 3: High-Speed Data Inputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{FLOOR}	Differential Data Input	500	—	—	mV	At $t_{PM} = t_{OPT.}$ See Figure 6.
		200	—	—	mV	At minimum t_{PM}. See Figure 6.
V_{IN}	Input Voltage	–1.8	–0.5	0.5	V	—
R_{TERM}	Termination Resistor	40	50	60	Ω	—

Table 4: High-Speed Clock Inputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IN}	Input Swing, Single-Ended	—	500	—	mV	Peak-to-Peak
R_{INDC}	DC Value of CLKI	–1.8	—	+1.8	V	—
R_{TERM}	Termination Resistor	40	50	60	Ω	—

Table 5: Power Dissipation

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{EE}	Supply Current	—	600	TBD	mA	Outputs Open
P_D	Power Dissipation	—	3.5	—	W	—

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Absolute Maximum Ratings(1)

ECL Power Supply Voltage, (V_{EE}) ..... –7.0V to +0.7V
DC Input Voltage (low-speed inputs, Q0-Q15±) ..... – 2.5V to +0.5V
Input Voltage, CLKI(2) ..... –2.8V to +2.8V
Input Voltage DI± ..... –1.8V to +0.5V
Case Temperature Under Bias ..... –55° to + 125°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions

Power Supply Voltage (V_{EE}) ..... –5.2V ±5%
Operating Case Temperature Range (**T**)(3) ..... 0° to 85°C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Static voltage on CLKI must be within –1.8V to +1.8V.

(3) Lower limit is ambient temperature and upper limit is case temperature.

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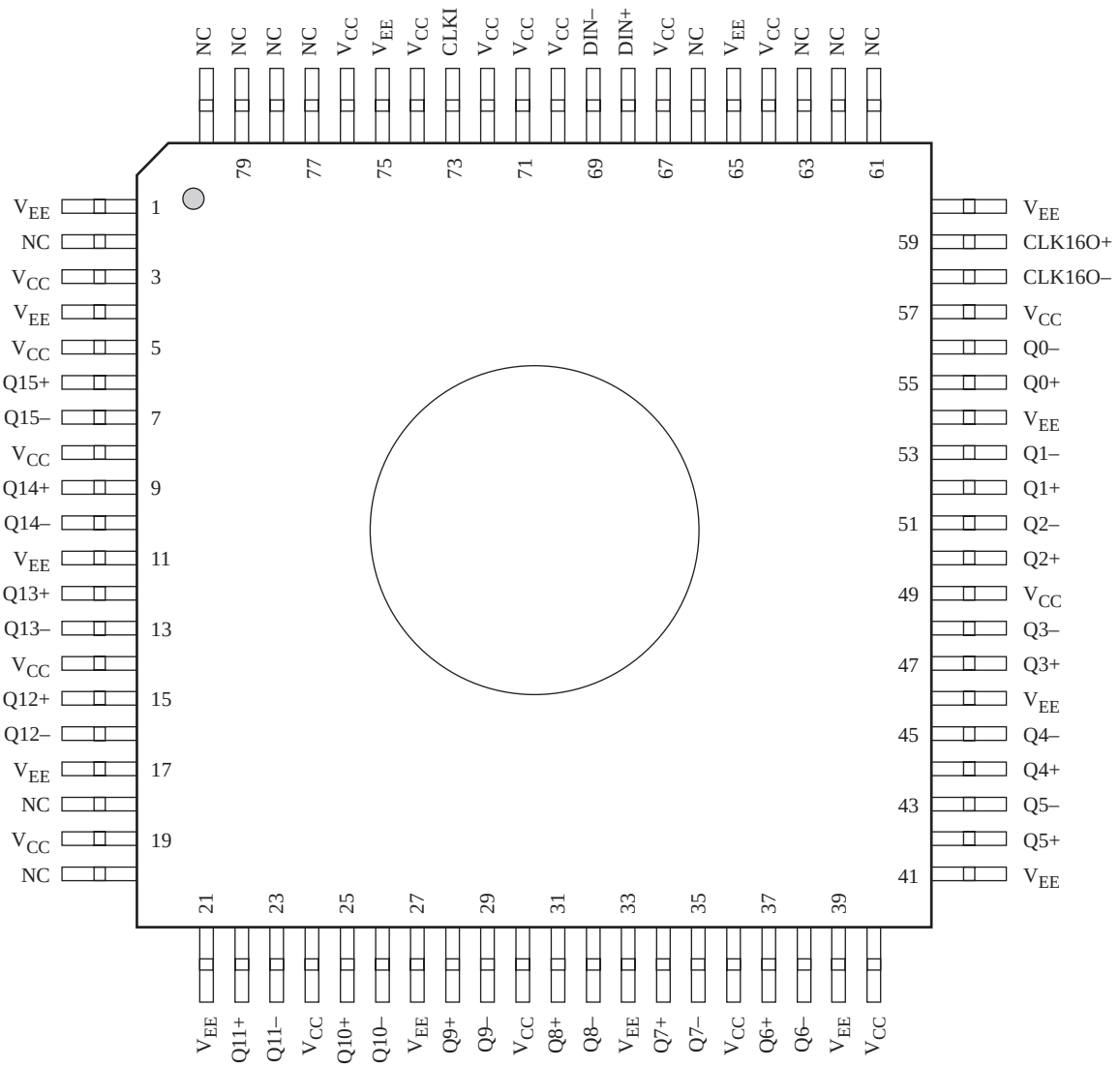
Package Pin Descriptions

Figure 8: Pin Diagram



Top View

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Table 6: Pin Identification

Pin	*I/O*	*Pin Description*
68, 69	DI±	INPUT—HIGH-SPEED DIFFERENTIAL: Serial data input stream. These inputs are internally terminated.
73	CLKI	INPUT—HIGH SPEED CLOCK: Bit rate clock input. This clock is terminated with 50Ω resistors to V_{CC}, and is AC-coupled.
6, 7, 9, 10, 12, 13, 15, 16, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38, 42-45, 47, 48, 50-53, 55, 56	Q0-Q15±	OUTPUT—ECL DIFFERENTIAL: Deserialized parallel data outputs. These outputs are updated at 1/16 of the bit rate.
58, 59	CLK16O±	OUTPUT—ECL DIFFERENTIAL: Bit rate clock divided by 16.
3, 5, 8, 14, 19, 24, 30, 36, 40, 49, 57, 64, 67, 70-72, 74, 76	V_{CC}	GROUND
1, 4, 11, 17, 21, 27, 33, 39, 41, 46, 54, 60, 65, 75	V_{EE}	POWER SUPPLY: –5.2 nominal.
2, 18, 20, 61-63, 66, 77-80	NC	Do not connect, leave open.

Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
1	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
2	NC	NA	NA	Do not connect, leave open.
3	V_{CC}	I	GND	Ground
4	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
5	V_{CC}	I	GND	Ground
6	Q15+	O	ECL	Low-speed differential parallel data
7	Q15–	O	ECL	Low-speed differential parallel data
8	V_{CC}	I	GND	Ground
9	Q14+	O	ECL	Low-speed differential parallel data
10	Q14–	O	ECL	Low-speed differential parallel data
11	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
12	Q13+	O	ECL	Low-speed differential parallel data
13	Q13–	O	ECL	Low-speed differential parallel data
14	V_{CC}	I	GND	Ground
15	Q12+	O	ECL	Low-speed differential parallel data
16	Q12–	O	ECL	Low-speed differential parallel data
17	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal

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Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
18	NC	NA	NA	Do not connect, leave open.
19	V_{CC}	I	GND	Ground
20	NC	NA	NA	Do not connect, leave open.
21	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
22	Q11+	O	ECL	Low-speed differential parallel data
23	Q11–	O	ECL	Low-speed differential parallel data
24	V_{CC}	I	GND	Ground
25	Q10+	O	ECL	Low-speed differential parallel data
26	Q10–	O	ECL	Low-speed differential parallel data
27	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
28	Q9+	O	ECL	Low-speed differential parallel data
29	Q9–	O	ECL	Low-speed differential parallel data
30	V_{CC}	I	GND	Ground
31	Q8+	O	ECL	Low-speed differential parallel data
32	Q8–	O	ECL	Low-speed differential parallel data
33	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
34	Q7+	O	ECL	Low-speed differential parallel data
35	Q7–	O	ECL	Low-speed differential parallel data
36	V_{CC}	I	GND	Ground
37	Q6+	O	ECL	Low-speed differential parallel data
38	Q6–	O	ECL	Low-speed differential parallel data
39	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
40	V_{CC}	I	GND	Ground
41	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
42	Q5+	O	ECL	Low-speed differential parallel data
43	Q5–	O	ECL	Low-speed differential parallel data
44	Q4+	O	ECL	Low-speed differential parallel data
45	Q4–	O	ECL	Low-speed differential parallel data
46	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
47	Q3+	O	ECL	Low-speed differential parallel data
48	Q3–	O	ECL	Low-speed differential parallel data
49	V_{CC}	I	GND	Ground
50	Q2+	O	ECL	Low-speed differential parallel data
51	Q2+	O	ECL	Low-speed differential parallel data
52	Q1+	O	ECL	Low-speed differential parallel data
53	Q1–	O	ECL	Low-speed differential parallel data

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Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
54	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
55	Q0+	O	ECL	Low-speed differential parallel data
56	Q0–	O	ECL	Low-speed differential parallel data
57	V_{CC}	I	GND	Ground
58	CLK16O–	O	ECL	Low-speed differential parallel data
59	CLK16O+	O	ECL	Low-speed differential parallel data
60	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
61	NC	NA	NA	Do not connect, leave open.
62	NC	NA	NA	Do not connect, leave open.
63	NC	NA	NA	Do not connect, leave open.
64	V_{CC}	I	GND	Ground
65	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
66	NC	NA	NA	Do not connect, leave open.
67	V_{CC}	I	GND	Ground
68	DI+	I	HS	High-speed differential clock input
69	DI–	I	HS	High-speed differential clock input
70	V_{CC}	I	GND	Ground
71	V_{CC}	I	GND	Ground
72	V_{CC}	I	GND	Ground
73	CLKI	I	HS	High-speed single-ended clock input
74	V_{CC}	I	GND	Ground
75	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
76	V_{CC}	I	GND	Ground
77	NC	NA	NA	Do not connect, leave open.
78	NC	NA	NA	Do not connect, leave open.
79	NC	NA	NA	Do not connect, leave open.
80	NC	NA	NA	Do not connect, leave open.

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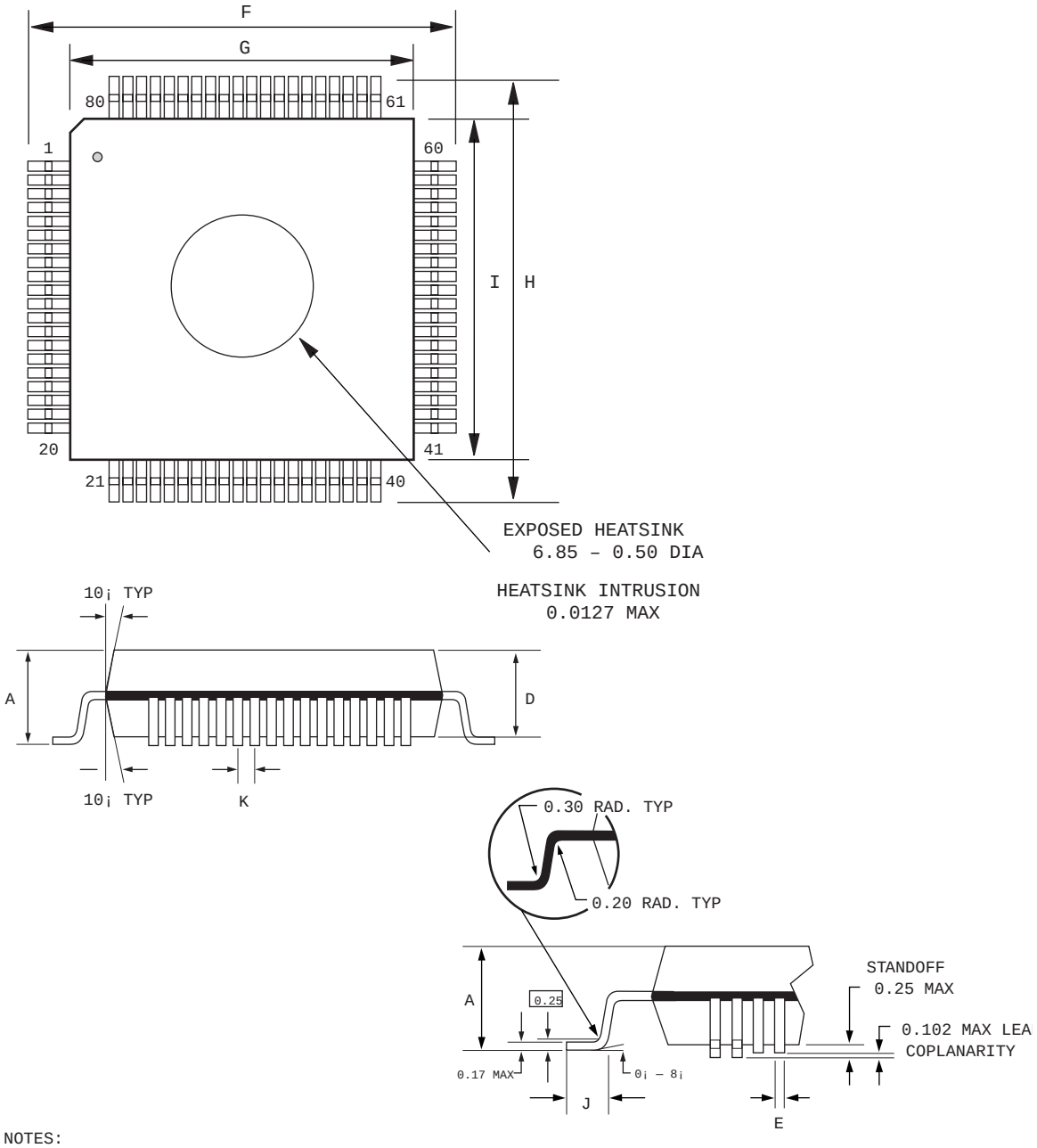
Package Information

80-Pin PQFP Package Drawing



NOTES:
Drawing not scale.
All units in mm unless otherwise noted.

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Package Thermal Conditions

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. Refer to Table 8 for thermal resistance.

Table 8: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{JC}	Thermal resistance from junction-to-case.	2.2
θ_{CA}	Thermal resistance from case-to-ambient with no airflow, including conduction through the leads.	25.8
θ_{JA}	Thermal resistance from junction-to-ambient	28

Thermal Resistance with Airflow

Table 9 shows the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst-case power of the device multiplied by the thermal resistance.

Table 9: Thermal Resistance with Airflow

Airflow (lfpm)	θ_{CA} *(°C/W)*
100	24
200	21
400	19
600	17

Maximum Ambient Temperature Without Heatsink

The worst-case ambient temperature without the use of a heatsink is given by:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\,\theta_{CA}$$

where,

θ_{CA} = Theta case-to-ambient at appropriate airflow

$T_{A\ (MAX)}$ = Ambient air temperature

$T_{C(MAX)}$ = Case temperature (85°C)

$P_{(MAX)}$ = Power (4.0W)

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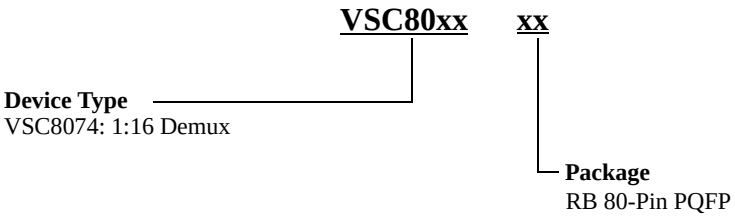
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



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Warning

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