BUK95/96/9E06-55B

N-channel TrenchMOS™ logic level FET

Rev. 03 — 30 November 2004 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology, featuring very low on-state resistance.

1.2 Features

- TrenchMOS™ technology
- 175 °C rated
- Q101 compliant
- Logic level compatible.

1.3 Applications

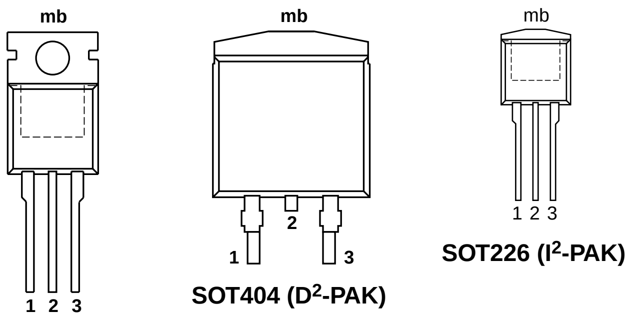
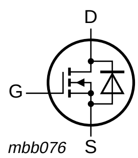
- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 679$ mJ
- $I_D \leq 75$ A
- $R_{DSon} = 5.1$ mΩ (typ)
- $P_{tot} \leq 258$ W.

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	SOT78 (TO-220AB) SOT404 (D²-PAK) SOT226 (I²-PAK)	
2	drain (D) [1]		
3	source (S)		
mb	mounting base; connected to drain (D)		

[1] It is not possible to make a connection to pin 2 of the SOT404 package.

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BUK9506-55B	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78
BUK9606-55B	D^2-PAK	Plastic single-ended surface mounted package (Philips version of D^2-PAK); 3 leads (one lead cropped)	SOT404
BUK9E06-55B	I^2-PAK	Plastic single-ended package (Philips version of I^2-PAK); low-profile 3 lead TO-220AB	SOT226

4. Limiting values

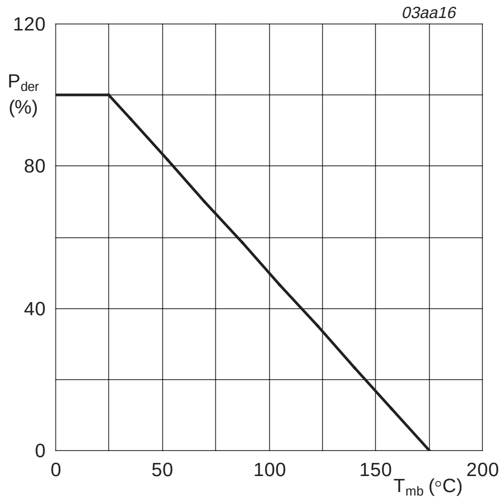
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	55	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage (DC)			-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	[1]	-	146	A
			[2]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	[2]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3		-	587	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	258	W
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[1]	-	146	A
			[2]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	587	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; starting at T_j = 25 °C		-	679	mJ

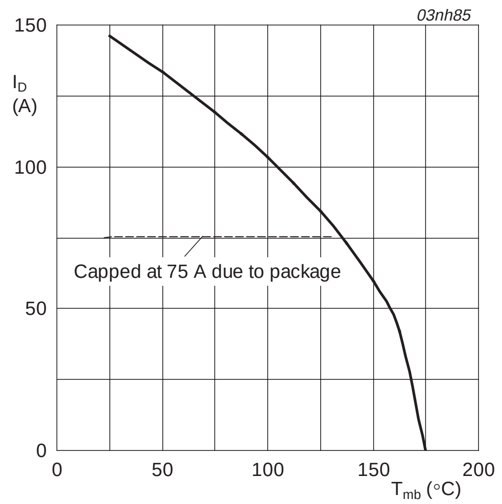
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package



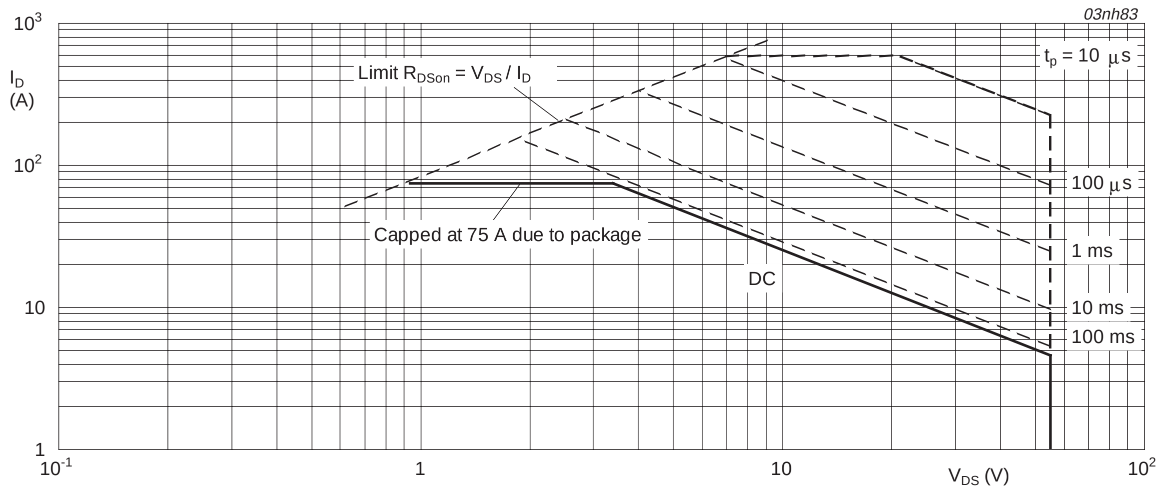
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.58	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78 (TO-220AB) and SOT226 (I^2-PAK)	vertical in free air	-	60	-	K/W
	SOT404 (D^2-PAK)	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

5.1 Transient thermal impedance

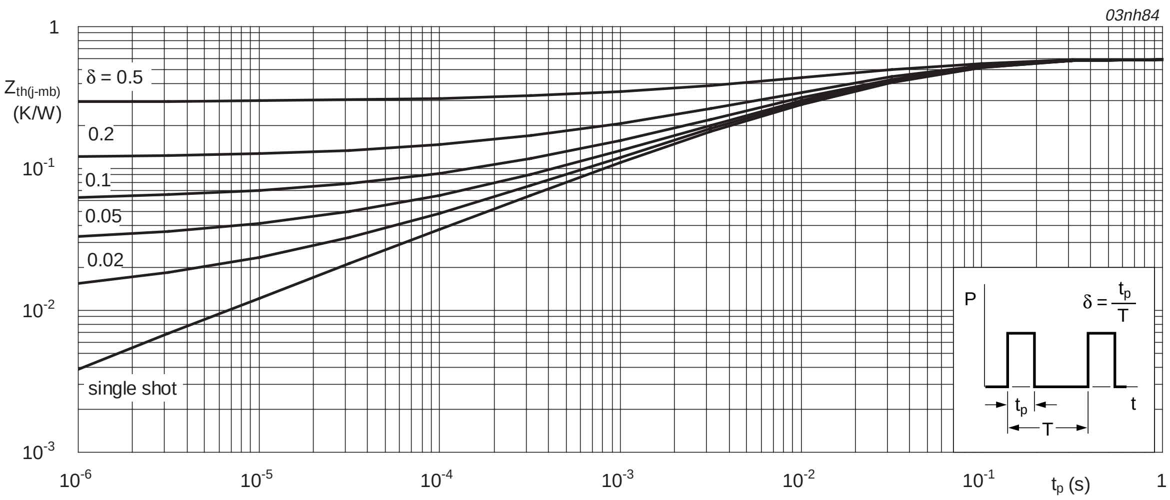


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

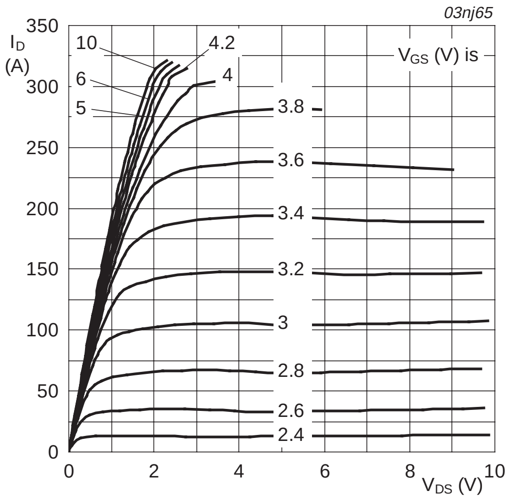
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1.1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 6 and 8				
		T_j = 25 °C	-	5.1	6.0	mΩ
		T_j = 175 °C	-	-	12	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; Figure 6 and 8	-	-	6.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; Figure 6 and 8	-	4.8	5.4	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 25 A; V_{DD} = 44 V; V_{GS} = 5 V; Figure 14 and 16	-	60	-	nC
Q_{gs}	gate-source charge		-	11	-	nC
Q_{gd}	gate-drain (Miller) charge		-	22	-	nC
V_{plat}	plateau voltage		-	2.4	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	5 674	7565	pF
C_{oss}	output capacitance		-	755	906	pF
C_{rss}	reverse transfer capacitance		-	255	350	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	37	-	ns
t_r	rise time		-	95	-	ns
$t_{d(off)}$	turn-off delay time		-	117	-	ns
t_f	fall time		-	106	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT404/SOT226	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH

Table 5: Characteristics

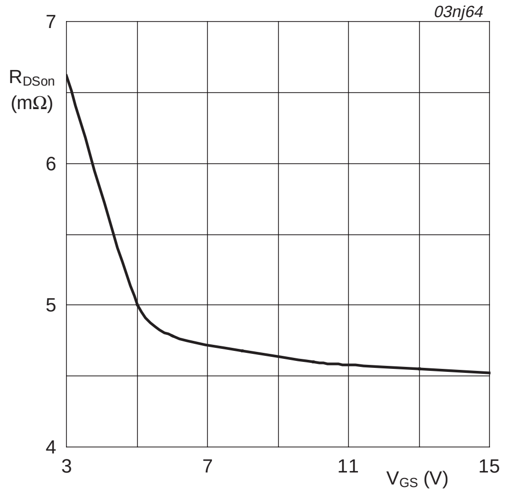
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	64	-	ns
Q_r	recovered charge		-	79	-	nC



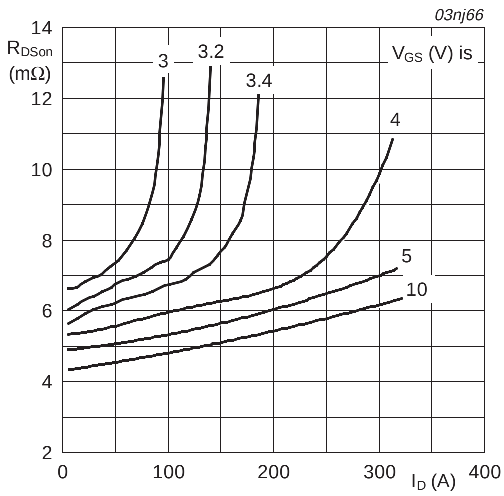
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



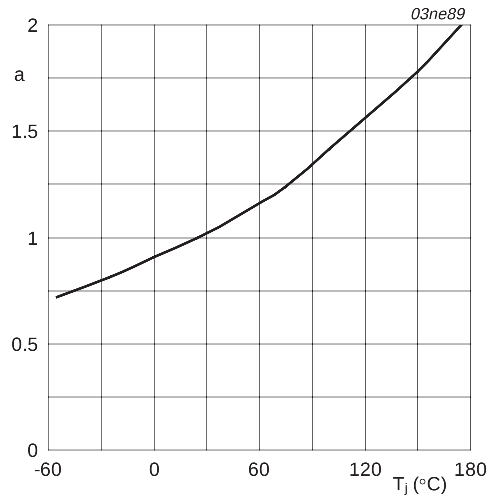
T_j = 25 °C; I_D = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



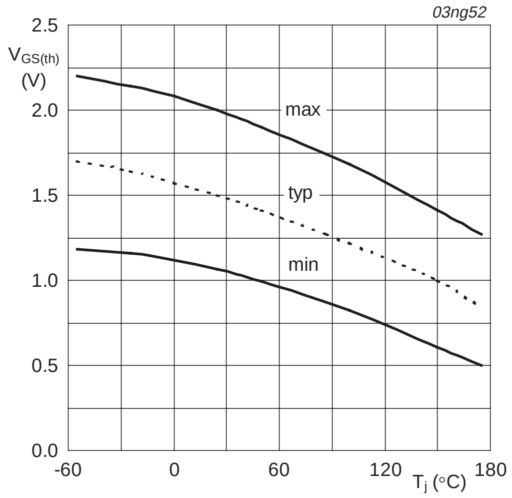
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



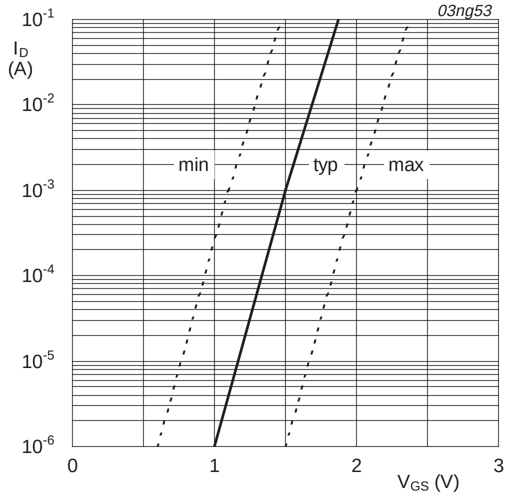
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



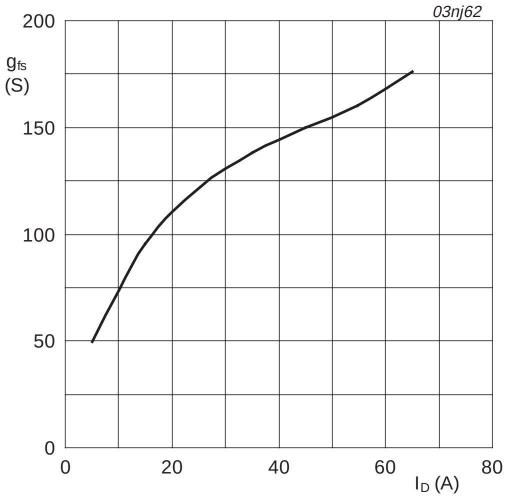
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



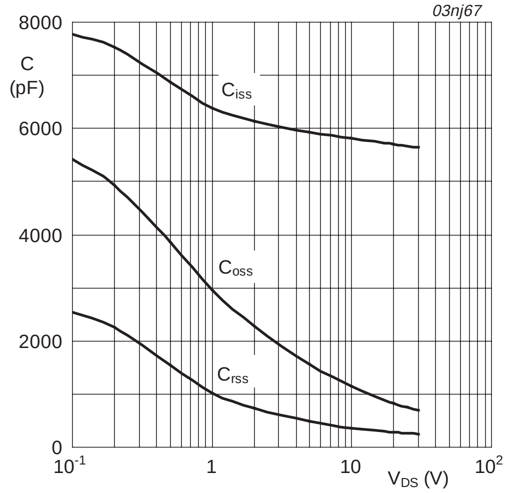
T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



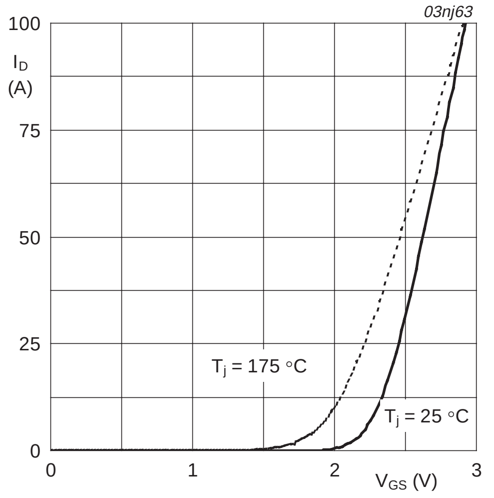
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



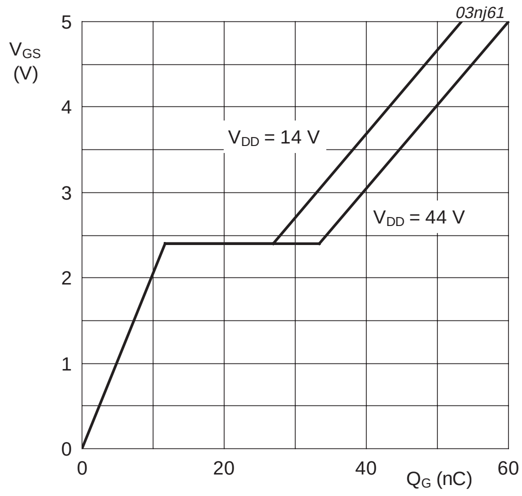
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



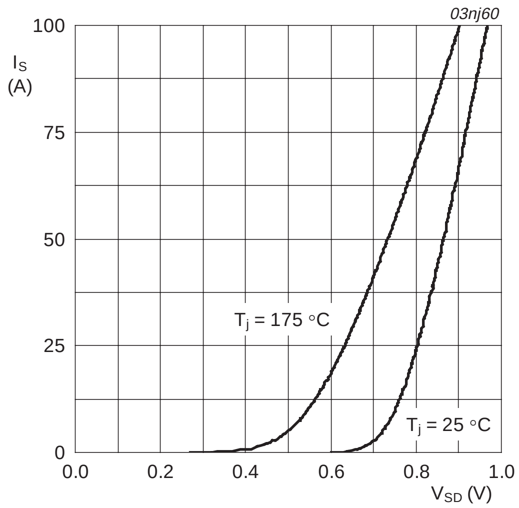
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of gate charge; typical values.



V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

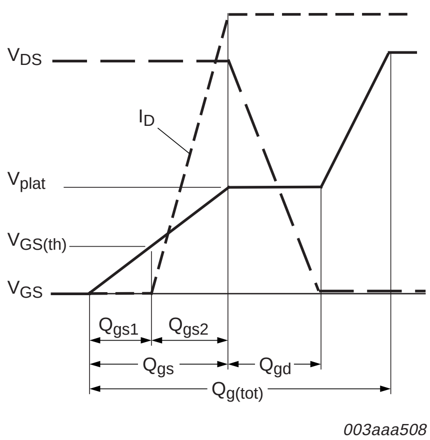
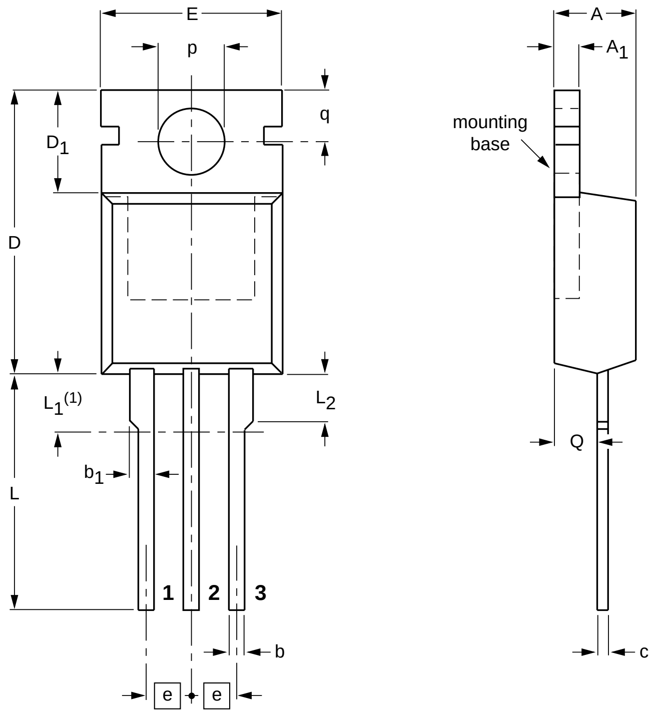


Fig 16. Gate charge waveform definitions.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1(1)	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.6	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

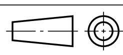
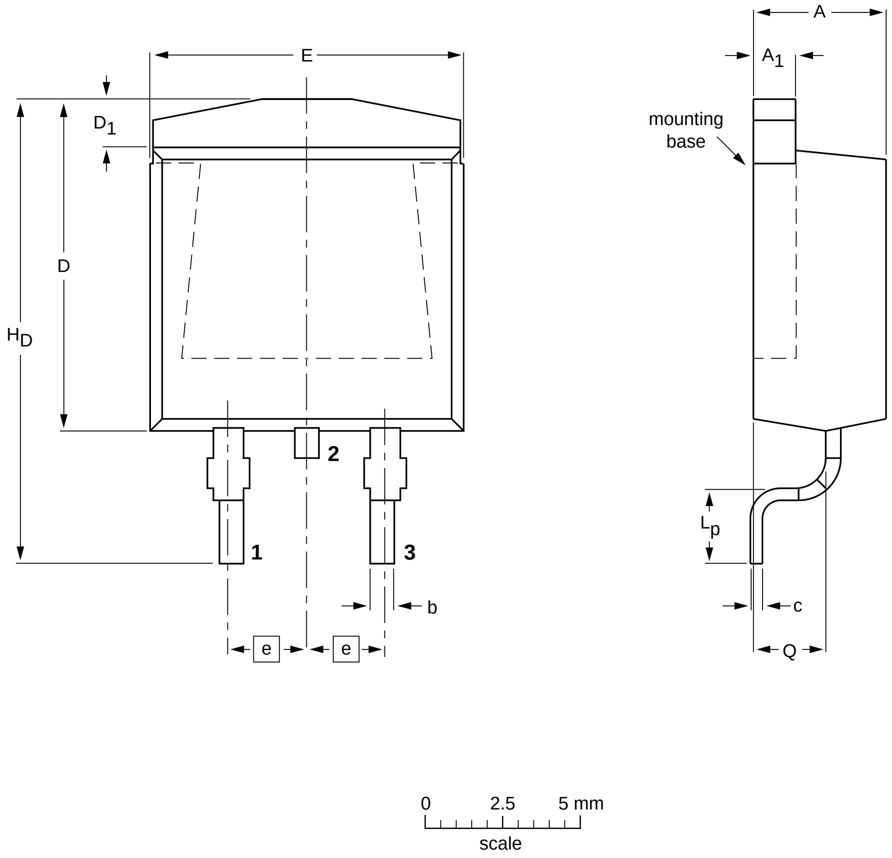
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~01-02-16~~ 03-01-22

Fig 17. Package outline SOT78 (TO-220AB).

Plastic single-ended surface mounted package (D^2-PAK); 3 leads (one lead cropped) **SOT404**



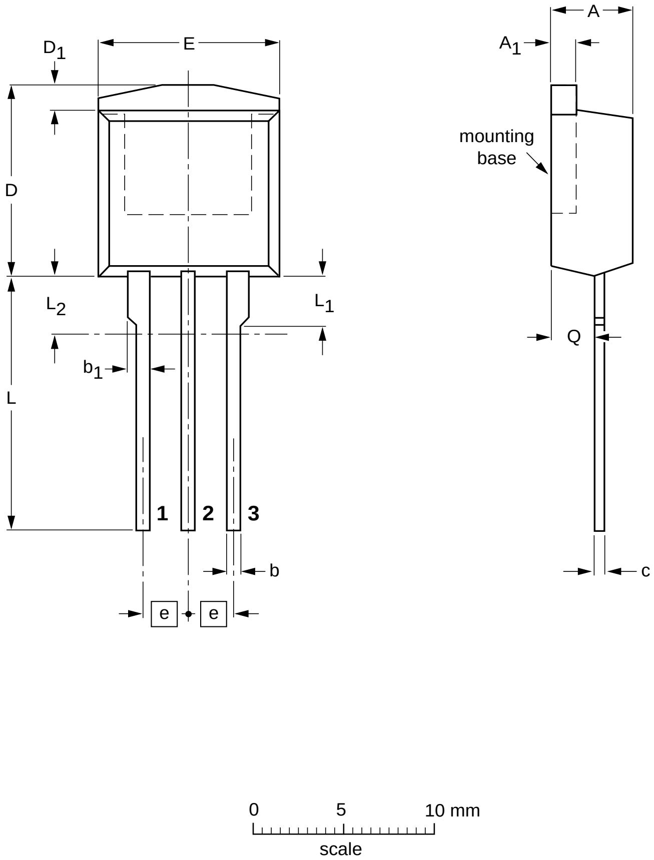
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~01-02-12~~ 04-10-13

Fig 18. Package outline SOT404 (D^2-PAK).

Plastic single-ended package (Philips version of I²-PAK); low-profile 3 lead TO-220AB **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D max	D_1	E	e	L	L_1	L_2(1) max	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	1.3 1.0	0.7 0.4	11	1.6 1.2	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3	2.6 2.2

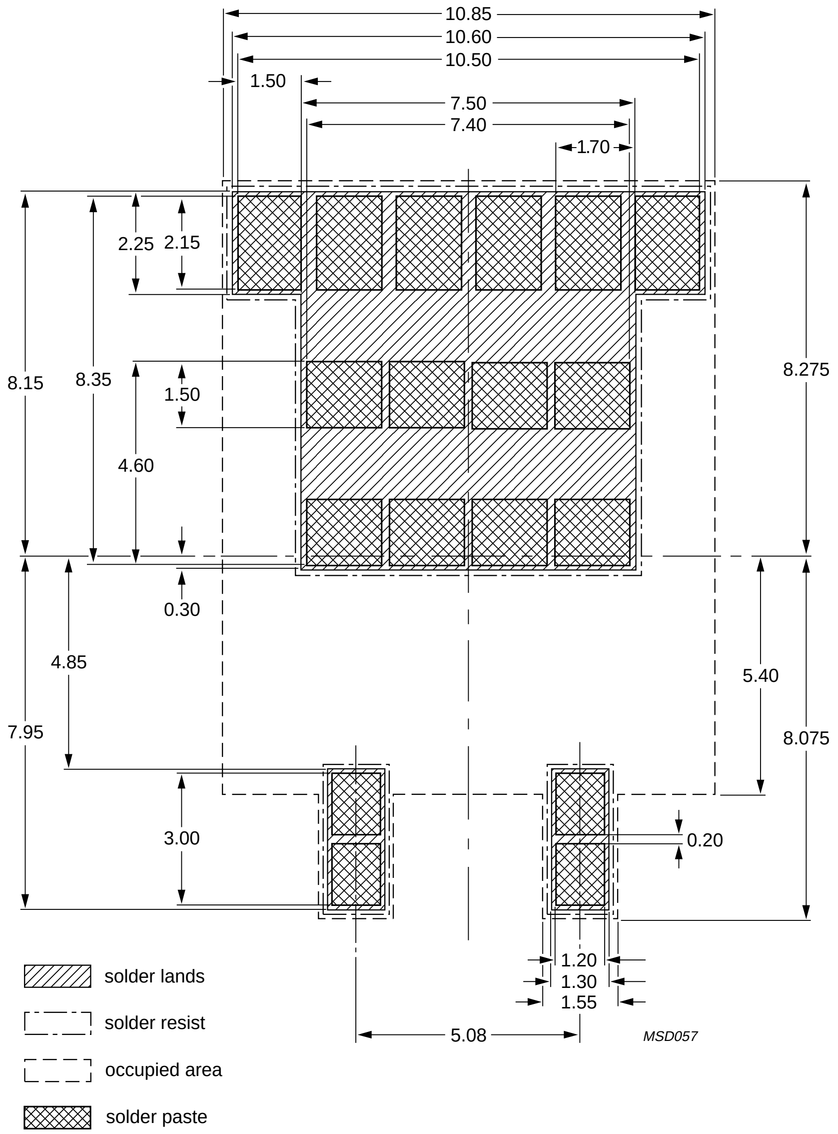
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT226		low-profile 3-lead TO-220AB				~~03-10-14~~ 04-02-24

Fig 19. Package outline SOT226 (I²-PAK).

8. Mounting



Dimensions in mm.

Fig 20. Reflow soldering footprint for SOT404.

9. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc number	Supersedes
BUK95_96_9E06_55B_3	20041130	Product data sheet	-	9397 750 13519	BUK95_96_9E06_55B_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Latest version of package outlines imported into Section 7 of data sheet.				
BUK95_96_9E06_55B-02	20021010	Product data sheet	-	9397 750 10474	BUK95_96_9E06_55B-01
BUK95_96_9E06_55B-01	20020813	Product data sheet	-	9397 750 09946	-

10. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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15. Contents

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