

TMC2067P7C

Dual A/D Demonstration Board for the TMC1185 10-Bit Analog-to-Digital Converter

Features

- Analog Composite and YC input processing
- 10-bit Digital Composite and YC outputs
- Fairchild demo board compatibility

Applications

- Evaluation of TMC1185, 10-bit A/D
- Evaluation of TMC2242, Decimation filter
- Input to the TMC2068P7C Decoder demonstration board.

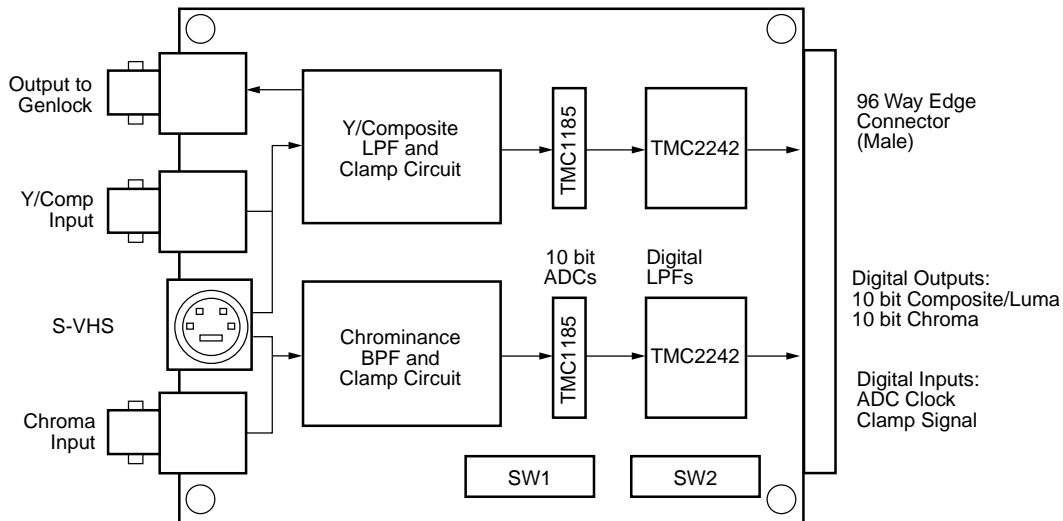
Description

The TMC2067P7C provides a high quality 10-bit front end for the TMC22153 digital decoder.

Composite and YC inputs are clamped and filtered before being oversampled in the TMC1185 10-bit A/D. The A/D outputs are decimated in TMC2242 half band filters to provide the pixel data to the TMC22153 digital decoder demonstration board.

Preliminary Information

Block Diagram



Analog Front End for the TMC22153 Digital Decoder

65-2067-01

Rev. 0.9.0

Functional Description

The Y/COMP (luminance/composite) analog input is buffered to a BNC for connection to the TMC22071A genlocking video digitizer on the TMC2068P7C decoder demonstration board. The Y/COMP signal is also passed through a simple antialiasing low pass filter. The filtered Y/COMP signal is clamped to the back porch level using the Elantec EL4390. The clamp pulse is provided by an FPGA on the TMC2068P7C decoder demonstration board, which is locked to the horizontal sync produced by the TMC22071A. The clamped Y/COMP signal is transformed into the differential input signal required by the TMC1185, 10-bit ADC. The differential Y/COMP signal is oversampled in the TMC1185, using the PXCK clock from the TMC22071A, and then decimated in the TMC2242 digital low pass filter.

The CHROMA (chrominance) analog input is passed through a simple bandsplit filter which acts as both the antialiasing filter for the TMC1185 and suppresses low frequency noise or signals on the CHROMA signal. The filter output is clamped to the chroma black level using the Elantec EL4390 using the same clamp pulse used to clamp the Y/COMP signal. The clamped CHROMA signal is transformed into the differential input signal required by the TMC1185. The differential CHROMA signal is oversampled in the TMC1185, using the PXCK clock from the TMC22071A, and then decimated in the TMC2242 digital low pass filter.

The mode of operation of the TMC2242 digital half band filters can be independently controlled using the two DIP switches, SW1 and SW2, provided.

An S-VHS connector is also provided and is directly coupled to the BNCs, therefore care should be taken not to connect inputs to both the BNCs and the S-VHS connector simultaneously.

12-Bit Option

The footprint for the Burr Brown 12-bit A/D (ADS800) is compatible with the Fairchild TMC1185 10-bit A/D, it is therefore possible to replace the TMC1185 and reconfigure the TMC2242, using the DIP switches, to evaluate the TMC22153 performance with a 12-bit oversampled A/D front end, which is then decimated and rounded to 10-bits. This improves the overall S/N performance by decreasing the noise introduced by the quantization of the video signal.

This option is not presently provided, and requires the board to be purchased and modified by the customer. However, applications support will be provided to assist in any modifications that are required.

Detailed Circuit Description

Composite/Luma Channel

The Y or Composite input from BNC J1 is terminated at R4 and buffered by U1:A to provide a synchronizing output at J2. In addition a second signal is buffered through U1:B to

the edge connector P2B pin 6. Optional AC coupling is provided by C3, C4 and R9. U9:B provides the necessary gain to drive the A-D converter and is provided with a gain adjustment, RV3.

The output of U9:B drives the anti-alias filter consisting of R45, C52, L5, C53, L6, C54 and R47. This filter provides a Butterworth response with about 30dB of attenuation at 13.5MHz. Since the filter introduces some group delay it is followed by an all-pass delay correction circuit consisting of U9:A and its associated components. (Additional correction is provided by the D-A driver/inverter circuit described below.)

The output of the anti-alias filter at U9:A pin 1 connects to one input of the clamp circuit consisting of U3 and its associated components. C18 provides DC isolation and storage of the clamp potential. The clamp pulse at pin 6 of U3 samples the reference potential at pin 14 to establish the clamp point for the A channel. The optimum position for the clamp pulse is immediately after the color burst to avoid phase and amplitude modulation of the burst. The clamp amplifier has a gain of two to compensate for the 6dB loss through the anti-alias filter (set by R24 and R25). The A-D has an input range of 1.25 to 3.25 volts and so the clamp reference voltage is chosen to put the composite signal within this range after a gain of two has been applied.

The second channel of the clamp circuit is used as a buffer for the A-D midpoint (CM) reference signal used by the inverters. This is achieved by connecting the clamp reference input of this channel to the amplifier input and running the amplifier at unity gain.

The clamped A channel signal connects to buffer U10:B and inverter U10:A. Both the buffer and inverter are configured for all-pass operation in order to provide additional group delay correction. The buffer is mainly required to provide delay matching between the normal and inverted inputs of the A-D converter. The inverter, U10:A obtains its invert reference from the buffered CM output of the A-D ensuring that the A channel signal is inverted about the midpoint of the A-D input range. The normal and inverted outputs from U10 connect to the differential inputs of the A-D converter, U11, via the filter networks consisting of R56, C62 and R52, C57.

For a detailed description of the A-D converter operation refer to the Fairchild TMC1185 data sheet.

The digital output of the A-D converter connects to the TMC2242B decimator, U7, where the pixel rate is halved. For more information on the decimator, refer to the Fairchild TMC2242B data sheet.

Chroma Channel

The B Channel is similar to the A channel except that the anti-alias filter is implemented as a bandpass filter and the clamp axis is chosen for a bipolar signal (i.e. A-D midpoint reference). The input stage U2:B is AC coupled from J4 via C5 and R11. The SVHS connector, J3, bridges the

Y/Composite and Chroma inputs so that only one set of inputs can be used at a time. The all-pass sections in his channel are primarily used to match the delay through the two channels.

Engineering Notes

The following notes relate to the ORCAD schematics and are supplemental to the circuit description.

1. The clamp circuit is a simple implementation using an Elantec EL4390 circuit. This circuit provides reasonably good clamping but loads the input during the sample pulse. This can cause a slight phase error if the clamp pulse occurs during the burst period. This can be corrected using the system phase adjustment or eliminated by clamping after the burst. Clamping after the burst requires a shorter clamp pulse (about 1-1.5 uS). Alternately the signal can be sync-tip clamped.
 2. The A-D midpoint reference (CM) for the inverters comes from the A channel A-D. This is done to make use of the available buffer in the EL4390 and avoid having an additional reference buffer. Although there may be a slight difference between the two references the DC level of the chroma channel is not critical since it is re-established in the TMC22x5y.
 3. The schematic has been designed for +/- 12V operation. If it is desired to run the system from +/- 5V supplies, it will be necessary to make the following changes:
 - a. Replace the EL2260 op. amps with EL2270 op. amps.
 - b. Connect two series connected diodes (1N914 or similar) in series with the outputs of the EL4390 at pins 10 and 15 with the cathodes of the diodes towards the output pins of the EL4390. Add a pull up resistor (470 ohms) from the anode of the last diode and the junction of R9 to +5V. Add a similar resistor on the other channel at the junction with R22.
 - c. Adjust the clamp reference voltage by changing R13 to 5.6K.
- Since the positive analog and digital supplies may now be the same, care should be taken to provide adequate filtering for the analog section of the circuit.
4. The power input filtering from the 96 pin connector uses ferrite beads. This should be adequate provided that the supplies do not have excessive low frequency noise. If the +5V digital supply from the main board is questionable it would be better to run a separate trace direct from the power supply to the 96 pin connector. Even using +/- 12V supplies it is still necessary that the +5V supply be reasonably clean since it is driving the A-D converters.
 5. It is assumed that the trace length associated with the decimator outputs is relatively short (<4 inches). If this is not the case it may be desirable to add series resistors in the data lines to correctly terminate the lines and avoid inducing ground currents in the submodule.
 6. When laying out the PC board, care should be taken to avoid placing the filter inductors close together. The optimum placement for horizontally wound inductors is in a T configuration or with a reasonable separation between them. It is preferable to isolate the +5V ground plane in the analog area although this may not be necessary using surface mount components provided the ground plane is situated immediately under the component layer. We recommend returning the analog and digital grounds separately to the power entry point. This may be achieved with a suitable moat on the ground plane. Although in some cases it is desirable to isolate the digital and analog grounds with a bead we do not consider it necessary in this situation. As usual, connections to the inverting inputs of the op amps should be as short as possible as should connections between the positive input and any input resistor.

DIP Switch Configurations

DIP switch	Function when OPEN	Function when CLOSED
SWA	* Correct position for normal operation	Not recommended, reserved for future use
SWB	* Correct position for normal operation	Not recommended, reserved for future use
SWC	* Correct position for normal operation	Not recommended, reserved for future use
SWD	* Correct position for normal operation	Not recommended, reserved for future use
SWE	\overline{DEC} pin HIGH on U7 ¹	\overline{DEC} pin LOW on U7
SWF	\overline{INT} pin HIGH on U7 ¹	\overline{INT} pin LOW on U7
SWG	* Two's complement output on U7	Unsigned output on U7
SWH	* Two's complement output on U8	Unsigned output on U8

DIP switch	Function when OPEN	Function when CLOSED
SWI	Output disabled on U7	* Output enabled on U7
SWJ	Output disabled on U8	* Output enabled on U8
SWK	* Inverts the msbs of YOVER[9:0], YADC[9:0], and CADC[9:0].	No inversion of YOVER[9]
SWL	* Inverts the msb of COVER[9:0]	No inversion of YOVER[9]
SWM	sets RND0 HIGH on U7 and U8	sets RND0 LOW on U7 and U8 ¹
SWN	sets RND1 HIGH on U7 and U8 ¹	sets RND1 LOW on U7 and U8
SWO	sets RND2 HIGH on U7 and U8 ¹	sets RND2 LOW on U7 and U8
SWP	unused	unused

Note:

1. Default value.

Slider Switch and Jumper Configurations

Board ref.	Functional description
E2	Connects the analog composite signal or chrominance signal (*) to the chrominance BPF and gain circuit
JP1	Terminates the video signal on BNC J2 when connected.
E4 & E5	Allows a 12-bit signal into U7 when OPEN, truncates to 10-bits when CLOSED(*)
E7 & E8	Allows a 12-bit signal into U8 when OPEN, truncates to 10-bits when CLOSED(*)
E3	Disconnects the chroma A/D clock, to reduce board noise if required.
E6	Disconnects the SYNC signal from the TMC2242's (*)
JP3	Terminates the buffered analog video signal on BNC J1 when connected.

Test Procedure

This test procedure establishes the correct digital data ranges for a NTSC composite video signal. An adjustment to the black level offset will be required for PAL composite video signals.

1. Set the DIP switches as indicated with (*) in the DIP switch configurations section, and the slider switches as directed with (*) in the slider switch configuration section.
2. Connect a composite video signal to BNC J1. Disconnect any inputs to connectors J3 and J4, or connect a luma signal to BNC J1 and a chroma signal to BNC J4 or a YC input to J3.
3. Verify that a 'clean' composite signal is on TP2 and TP3. It is essential that a 'clean' composite waveform appears on TP2. If TP3 has no signal move the slider on E2.
4. Check that a 'clean' composite signal appears on TP1, this will be twice the amplitude of the signal on TP2 unless the signal is terminated using JP1. For normal operation this signal should be left unterminated.
5. Check that a 'clean' composite signal appears on TP22, this will be twice the amplitude of the signal on TP2 unless the signal is terminated using JP3. For normal operation this signal should be left unterminated.
6. Check that the TTL clamp pulse on TP9 is locked to the analog video signal on TP2. The clamp pulse should be 0.5 uS wide and positioned on the back porch between the burst and the start of active video.
7. To set the composite signal gain, connect a scope probe to TP6. Adjust RV3 (clockwise reduces the gain) to establish a peak white (100 IRE) signal equal to 576mV.
8. Verify that the signal on TP7 is the chrominance signal only, using 75% SMPTE color bars as the composite input signal. Adjust RV1 (clockwise reduces the gain) to establish 340mV on TP7 using the yellow and blue bars as the reference.
9. Adjust the black level offset, using RV2, to set 800mV on C15.
10. Adjust RV4 to provide a voltage on C21 that is equal to half the average of the voltages on TP8 and U3 pin 5.

The following table show the digital data ranges that will be produced if the TMC2076P7C test procedure is followed.

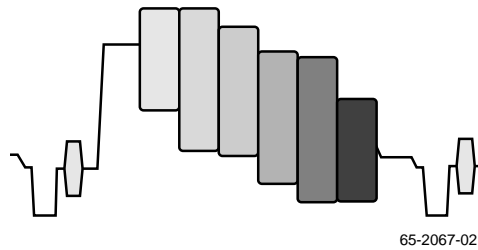


Figure 1. Composite Video Waveform

Table 1. 10-bit Composite Input Data Ranges

Color Bar	NTSC/M		PAL/I	
	Y	C	Y	C
White	824	0	828	0
Yellow	762	+/- 242	763	+/- 257
Cyan	663	+/- 341	657	+/- 362
Green	601	+/- 319	592	+/- 338
Magenta	507	+/- 319	492	+/- 338
Red	445	+/- 341	426	+/- 362
Blue	345	+/- 242	321	+/- 257
Pedestal	284	0	n/a	n/a
Blanking	240	0	256	0
Burst	0	+/- 117	0	+/- 122
Sync Tip	6	0	10	0

Bill of Materials

Item	Quantity	Part Number	Reference
1	1	CR1	Red, +5V
2	1	CR2	Red, +12V
3	1	CR3	Orange, -12V
4	1	CR4	Orange, -5V
5	40	C1, C2, C5, C6, C8, C10, C15, C16, C17, C18, C19, C20, C21, C24, C25, C26, C29, C30, C31, C32, C35, C39, C43, C45, C46, C47, C48, C50, C58, C59, C60, C63, C64, C65, C66, C67, C68, C69, C70, C73	0.1 μ F
6	2	C4, C3	100 μ F/6.3v
7	4	C7, C14, C49, C55	10 μ F/25V
8	2	C9, C53	220pF
9	7	C11, C23, C28, C56, C57, C61, C62	22pF
10	2	C13, C12	120pF
11	2	C27, C22	47pF
12	4	C33, C37, C41, C71	22 μ F/25v
13	4	C34, C38, C42, C72	0.47 μ F/25v
14	4	C36, C40, C44, C74	0.01 μ F
15	1	C51	30pF
16	2	C52, C54	68pF
17	8	D1, D2, D3, D4, D5, D6, D7, D8	MMBD301
18	4	D9, D10, D11, D12	1N4004
19	6	E1, E2, E4, E5, E7, E8	Select
20	1	E3	ADC Clk Disable
21	1	E6	Sync Disable
22	4	FB1, FB2, FB3, FB4	F BEAD
23	5	GND1, GND2, GND3, GND4, GND5	GND
24	2	JP1, JP3	Termination
25	1	JP2	POWER 6
26	3	J1, J2, J4	BNC
27	1	J3	S-VIDEO
28	3	L1, L4, L8	10 μ H
29	1	L2	4.7 μ H
30	1	L3	15 μ H
31	3	L5, L6, L7	6.8 μ H
32	8	PTH1, PTH2, PTH3, PTH4, PTH5, PTH6, PTH7, PTH8	PTH
33	1	P1	Header 96
34	1	P2	EURO96M
35	2	RN2, RN1	4.7K
36	2	RV1, RV3	1K POT
37	1	RV2	1K POT
38	1	RV4	500 POT
39	5	R1, R26, R27, R28, R59	75
40	6	R2, R6, R10, R21, R50, R60	220

Preliminary Information

Bill of Materials (continued)

Item	Quantity	Part Number	Reference
41	3	R3, R4, R12	75 1%
42	22	R5, R7, R8, R14, R15, R20, R34, R36, R37, R38, R40, R41, R43, R44, R49, R51, R53, R54, R55, R57, R58, R61	750
43	4	R9, R11, R62, R63	10K
44	8	R13, R19, R35, R39, R42, R48, R52, R56	47
45	3	R16, R18, R47	200 1%
46	2	R17, R46	1K
47	1	R22	15K
48	1	R23	500
49	5	R24, R25, R31, R32, R33	1.2K 1%
50	2	R30, R29	1K %
51	1	R45	200
52	2	S2, S1	SW DIP-8
53	21	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP26	TP
54	1	TP13	+5V
55	1	TP14	+12V
56	1	TP15	-12V
57	2	TP25, TP24	Coax Mount
58	1	TP27	-5V
59	5	U1, U2, U4, U9, U10	EL2260C
60	1	U3	EL4390C
61	2	U5, U11	TMC1185NDC40
62	1	U6	74F86
63	2	U7, U8	TMC2242BR2

Preliminary Information

Schematics

Preliminary Information

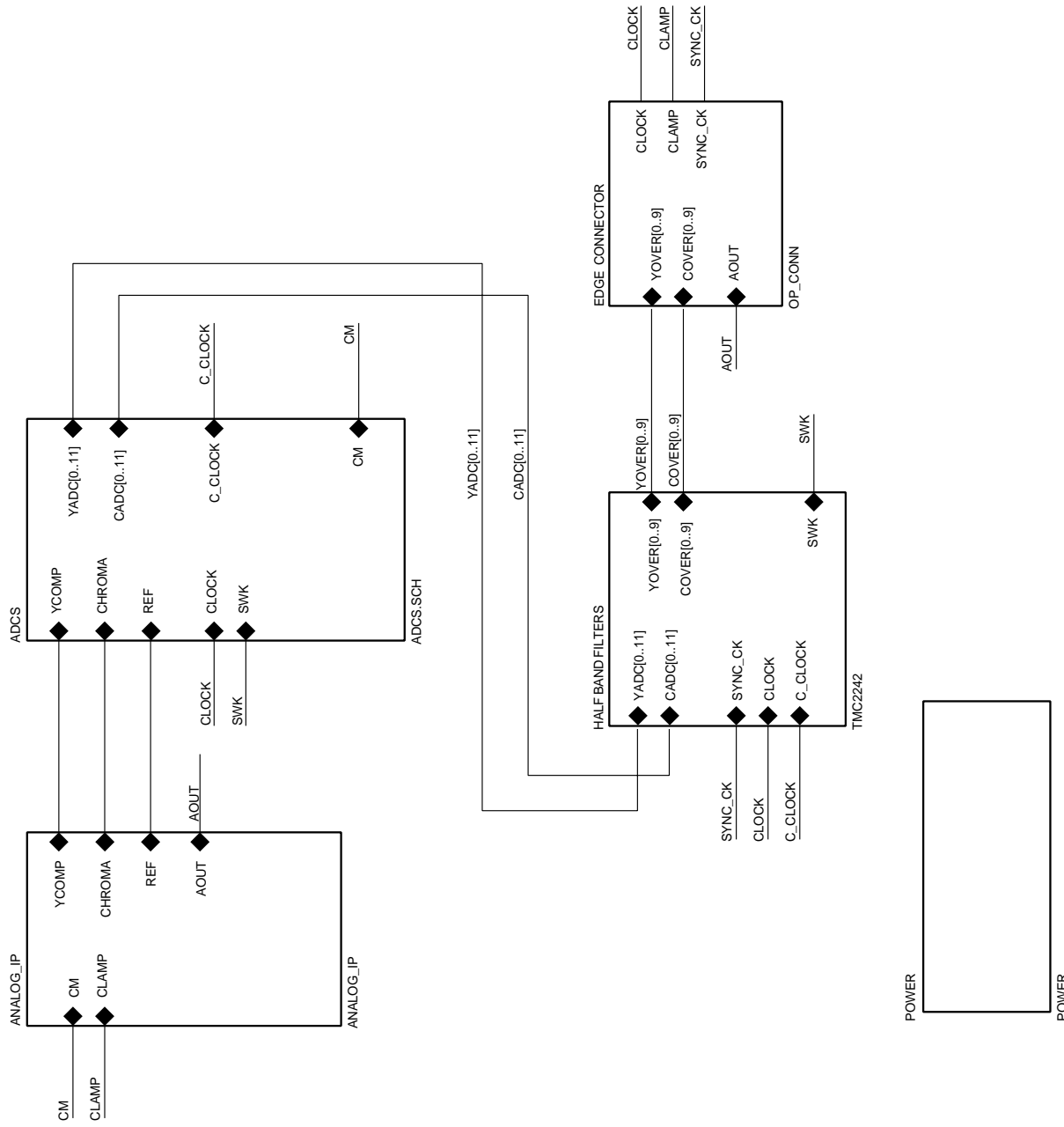


Figure 2. ADC10B

Schematics (continued)

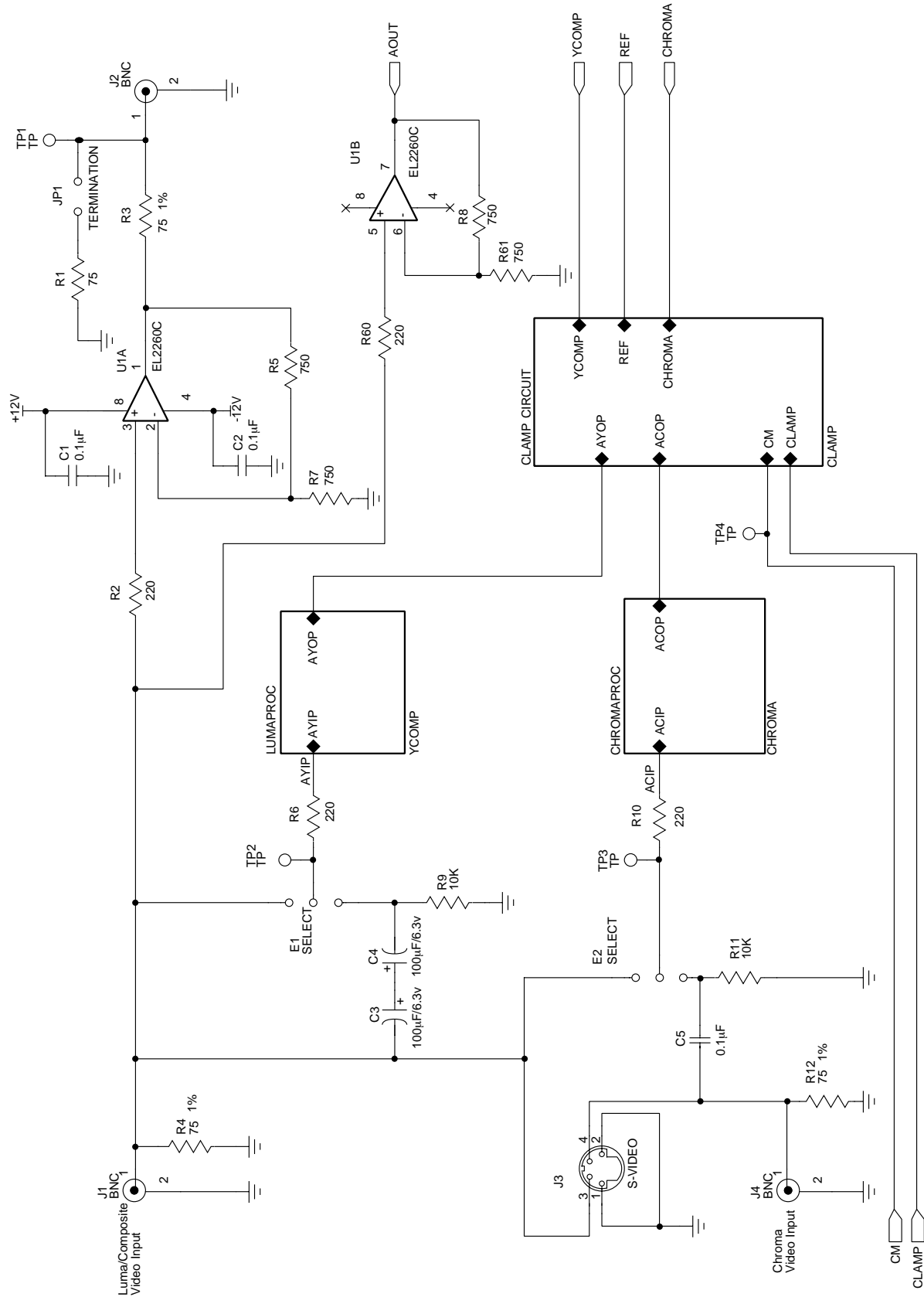


Figure 3. Analog_IP

Preliminary Information

Preliminary Information

Schematics (continued)

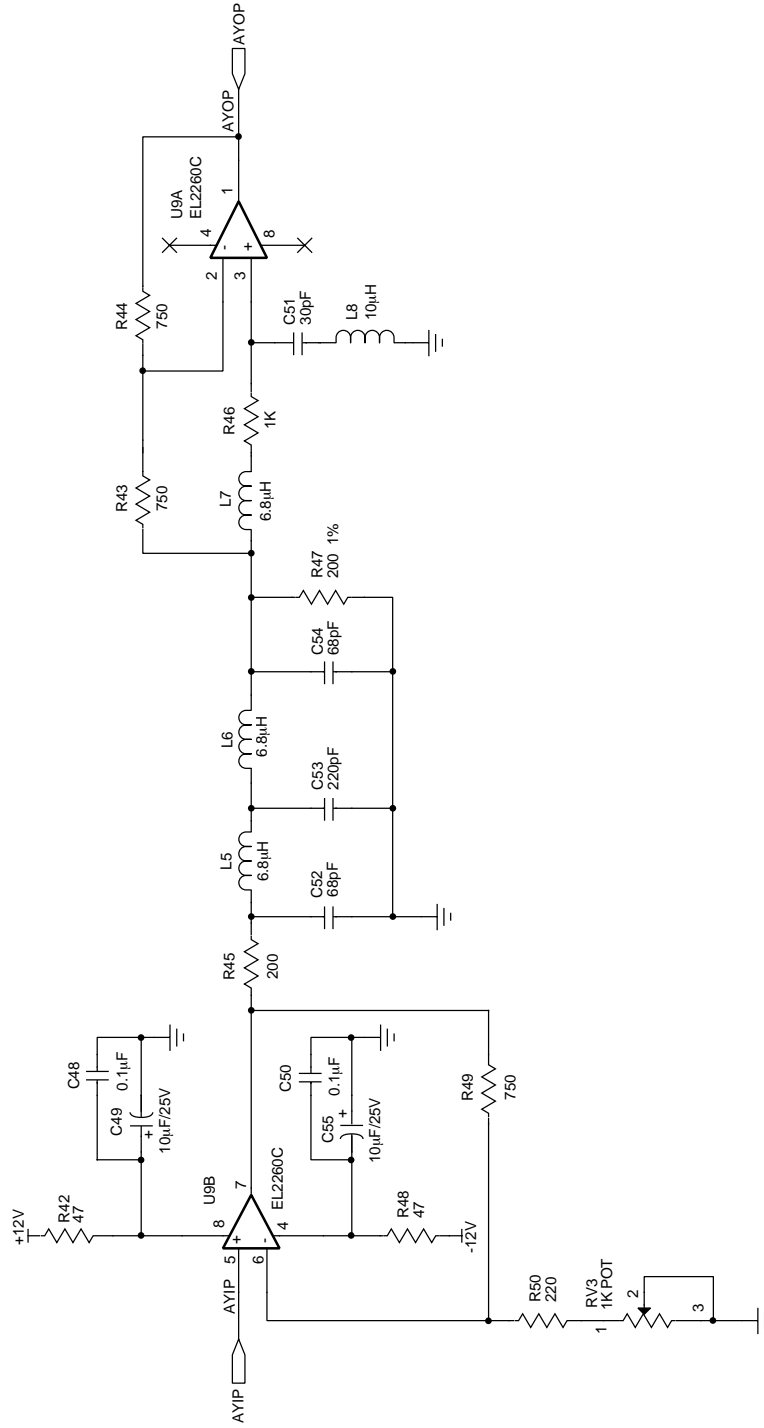


Figure 4. YCOMP.SCII

Schematics (continued)

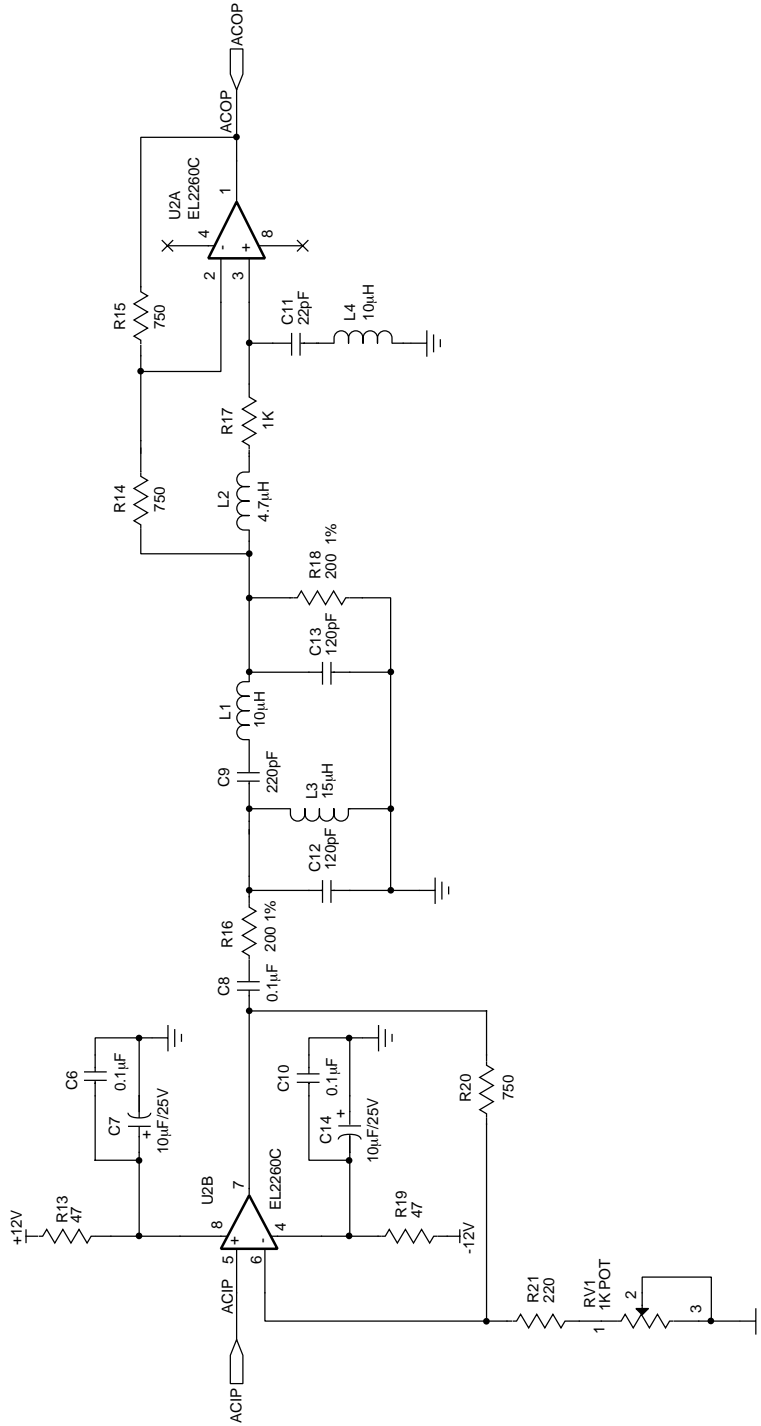


Figure 5. Chroma

Preliminary Information

Schematics (continued)

Preliminary Information

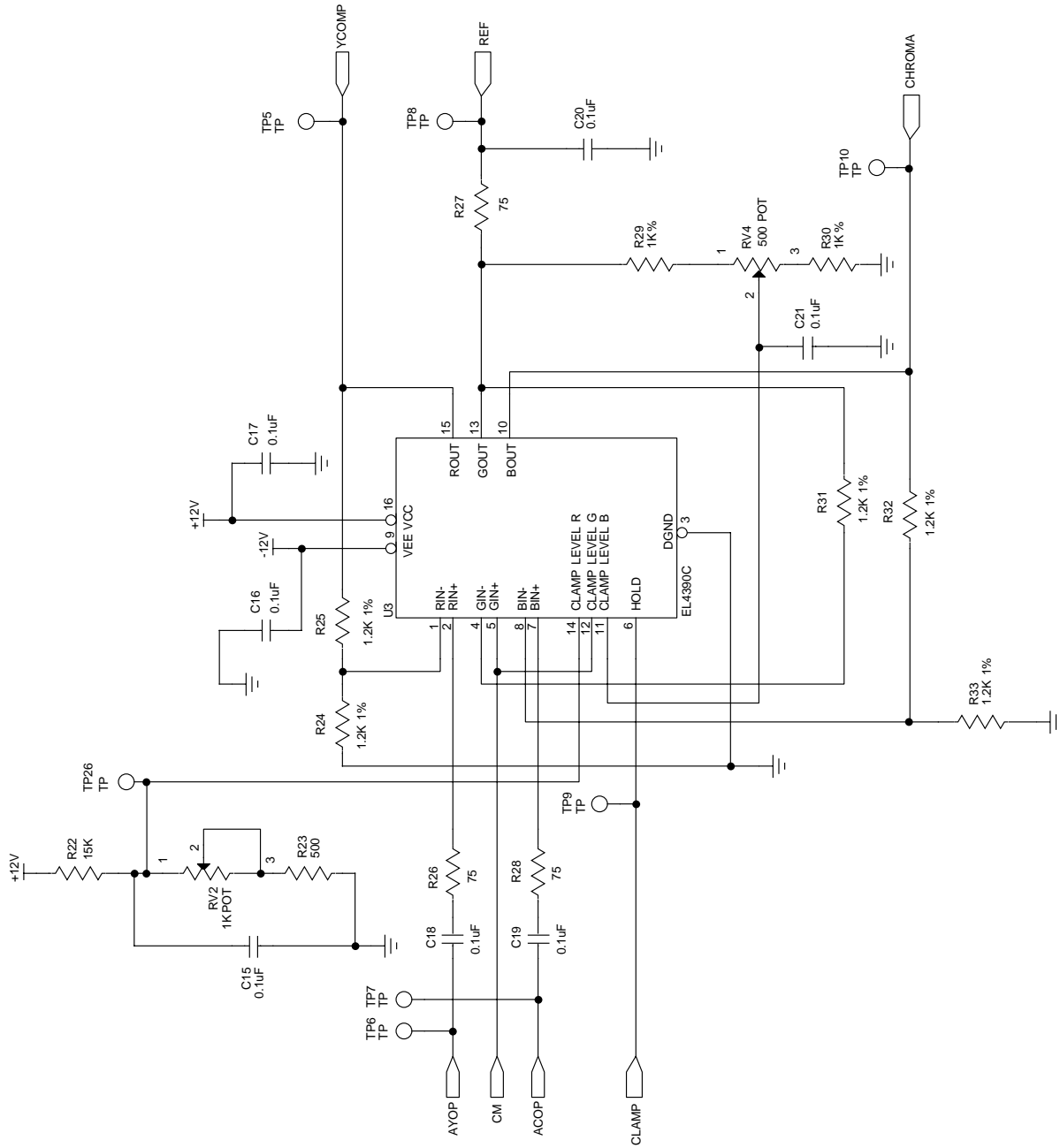


Figure 6. Clamp

Schematics (continued)

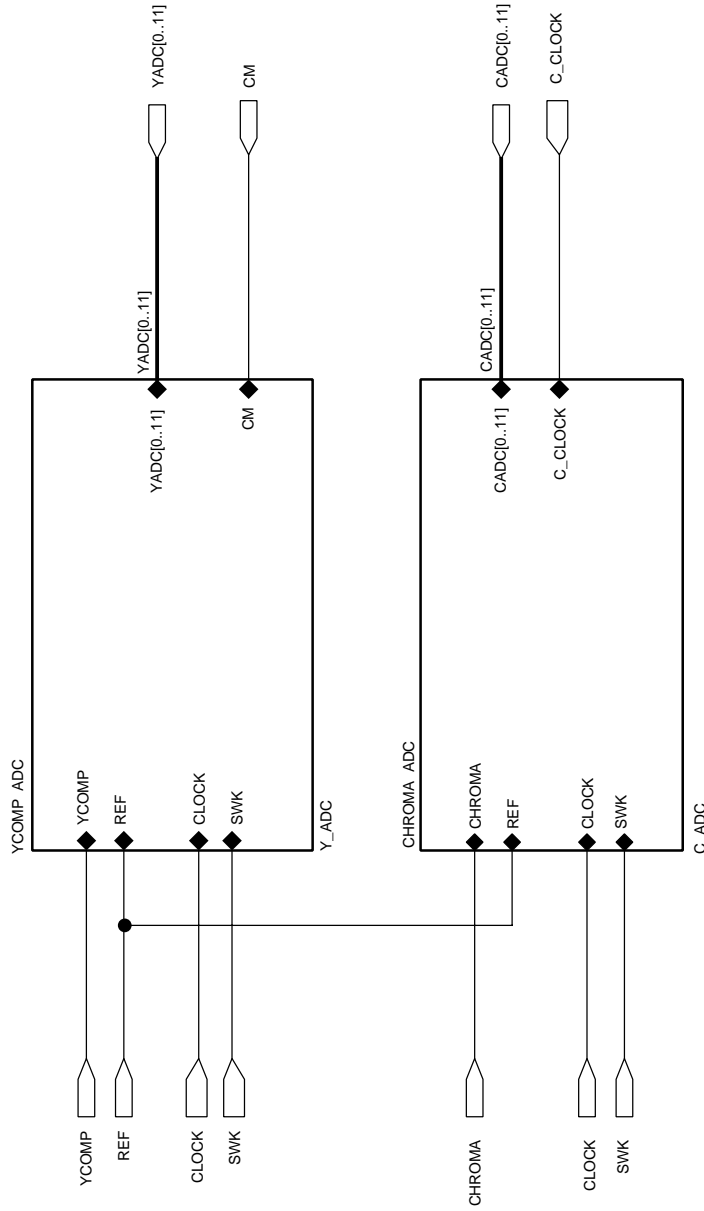


Figure 7. ADCS

Schematics (continued)

Preliminary Information

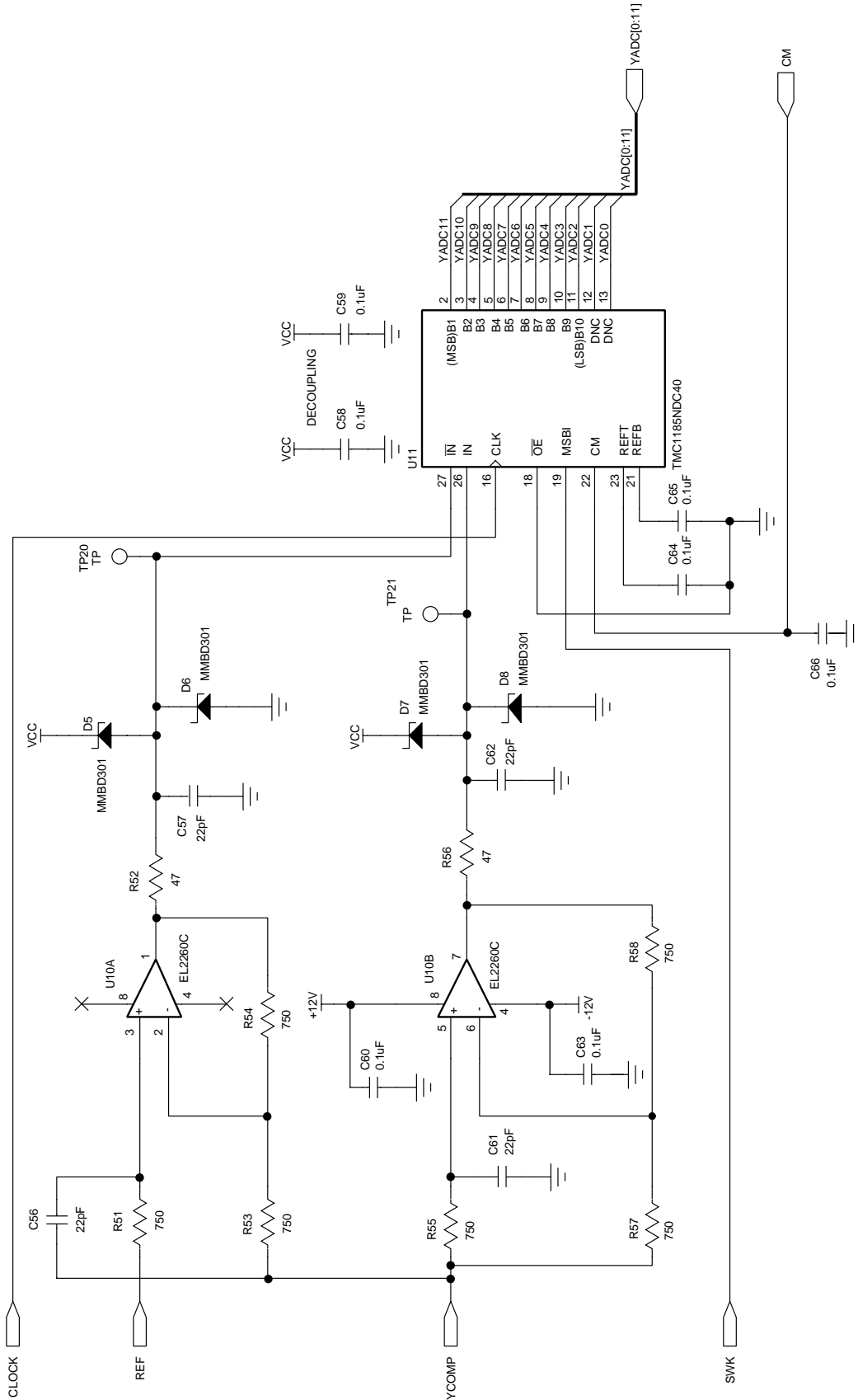


Figure 8. YADC.SCH

Schematics (continued)

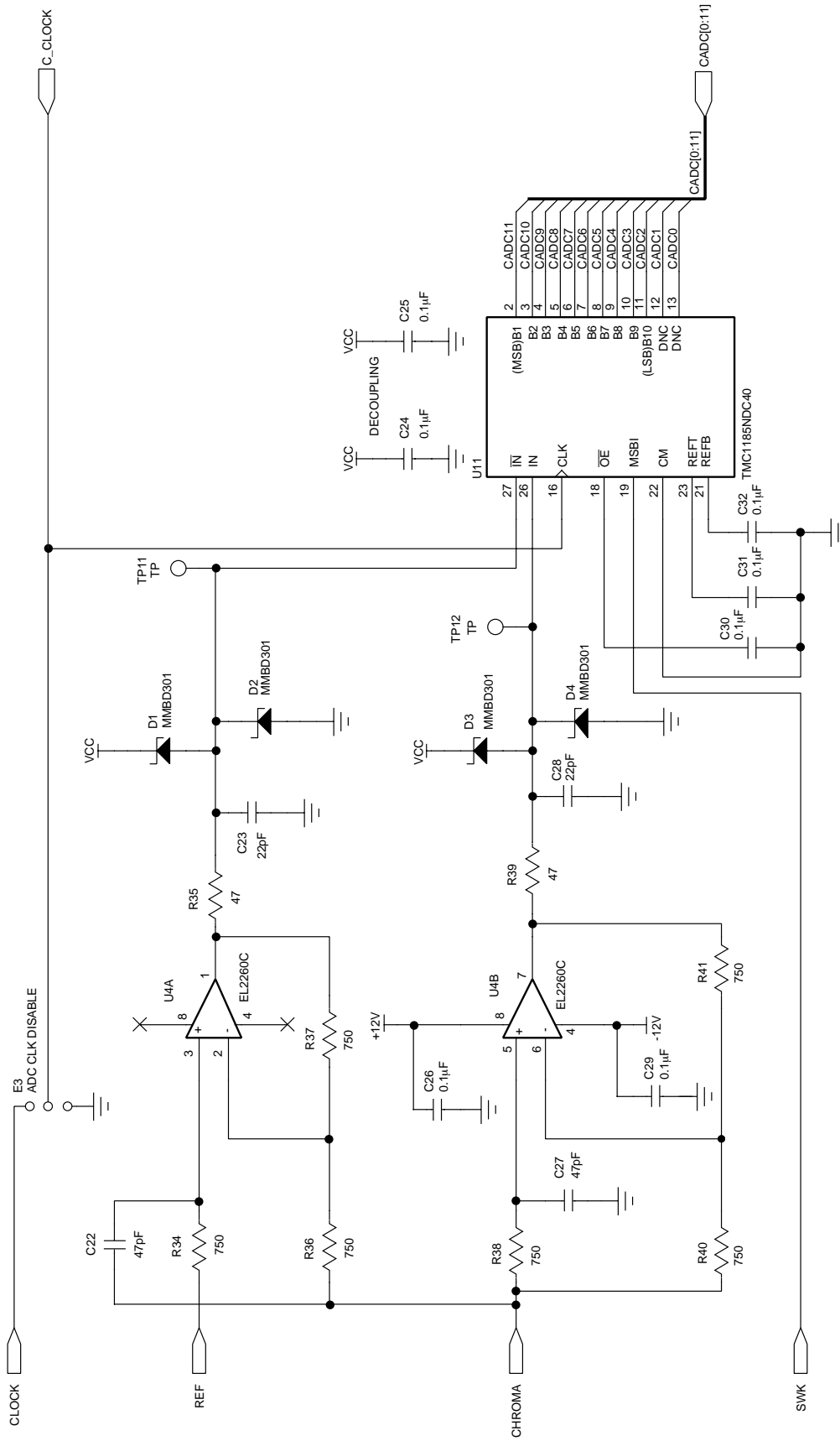


Figure 9. C_ADC

Preliminary Information

Schematics (continued)

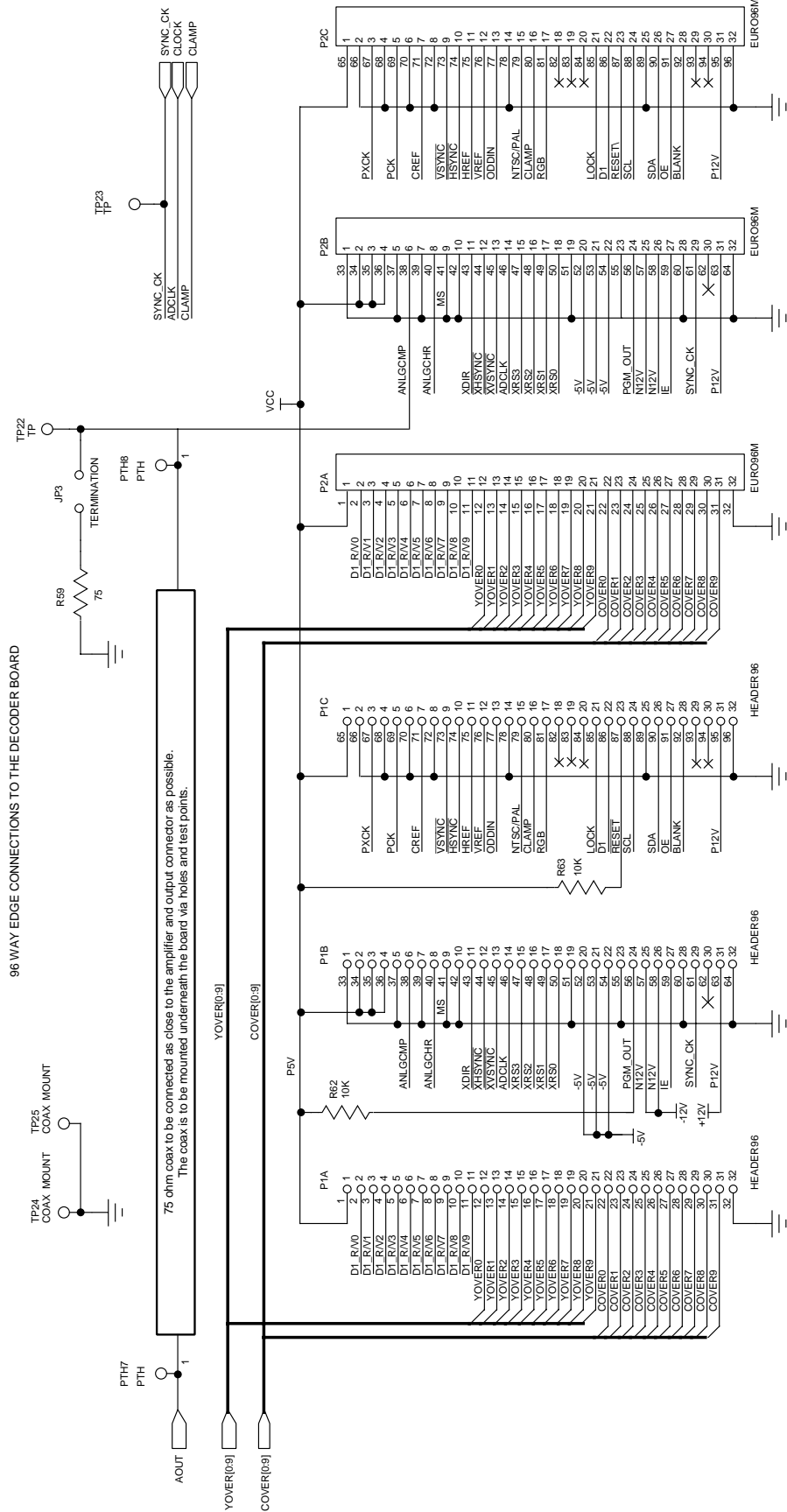


Figure 11. OP_CONN

Preliminary Information

Preliminary Information

Schematics (continued)

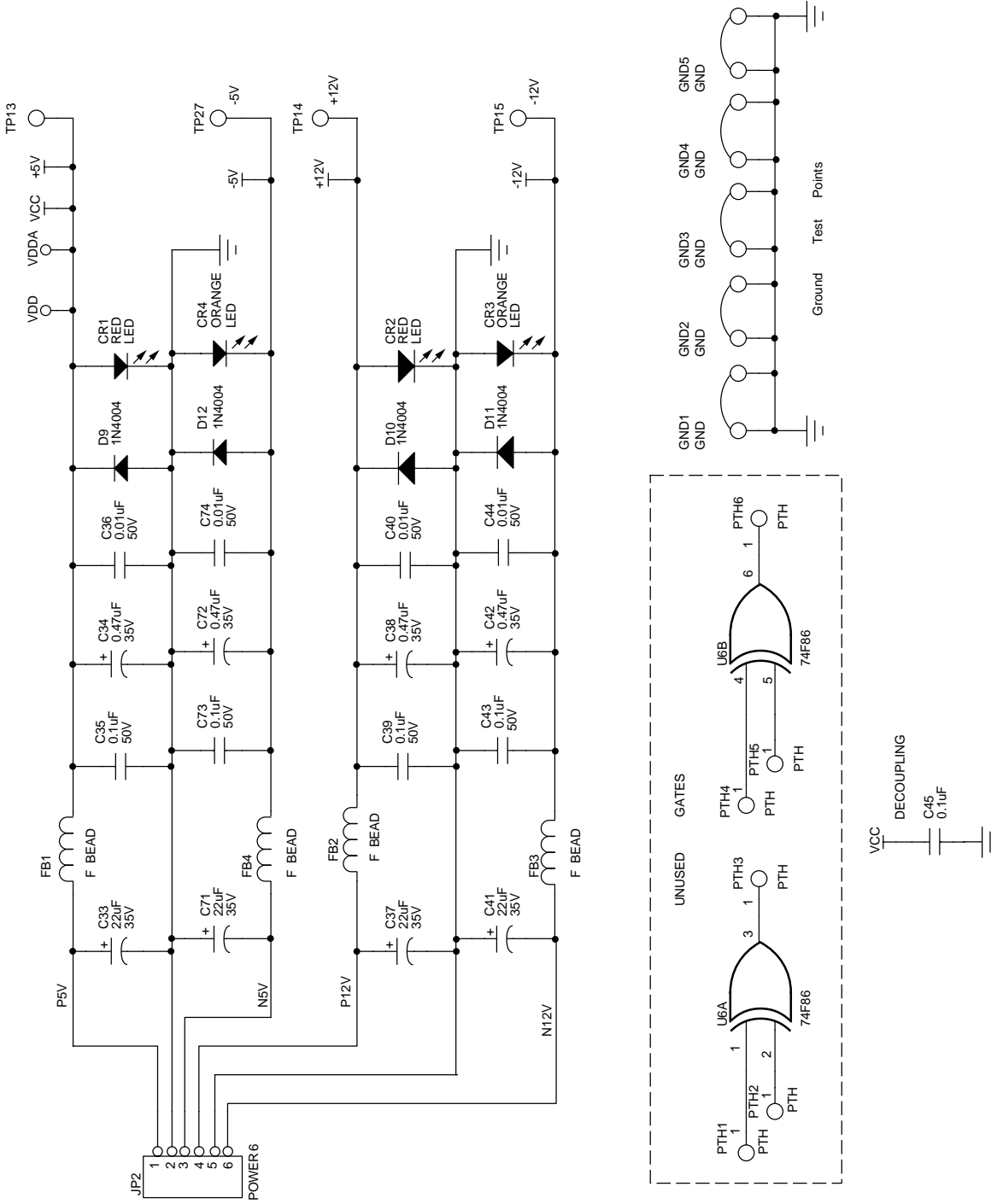


Figure 12. Power

Output Edge Connector Design Notes

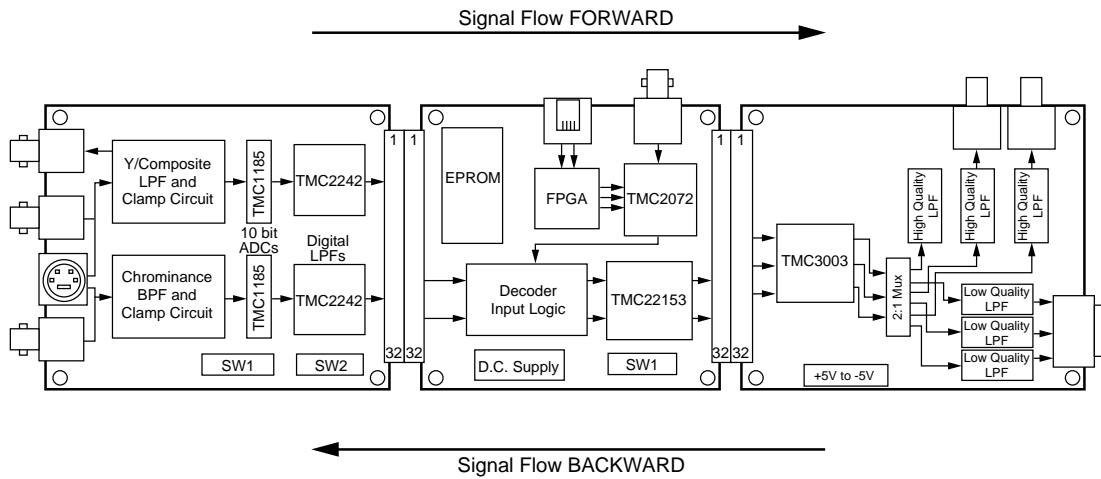


Figure 13.

- Boards with different revision numbers may not be compatible, damage may occur if they are connected together.
- XPXCK is a two times pixel clock fed BACKWARD.
- XHSYNC and XVSYNC are timing reference signals fed BACKWARD.
- The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD. A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc.
- XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
- PGM_OUT negative going signal pulse for initiating programming of down stream boards, generated once the devices on the board have been programmed. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. The Minimum width of PGM_OUT is 1µS.
- The RESET pin on the output edge connector should be connected directly to the RESET pin on the input connector. A link should be used to connect any pulse to the RESET line.
- The MASTER/SLAVE, XDIR, PGM_OUT and RESET pins on the output edge connector should be connected to +5V through a 10k pull up resistor.
- The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

OUTPUT 96 way connector (male)

row A		row B		row C	
1	+5v	1	GND	1	+5v
2	D1 or R/V [bit 0]	2	+5V	2	GND
3	D1 or R/V [bit 1]	3	+5V	3	PXCK
4	D1 or R/V [bit 2]	4	+5V	4	GND
5	D1 or R/V [bit 3]	5	GND	5	PCK
6	D1 or R/V [bit 4]	6	<i>Analog Composite/luma</i>	6	GND
7	D1 or R/V [bit 5]	7	GND	7	CREF
8	D1 or R/V [bit 6]	8	<i>Analog chroma</i>	8	GND
9	D1 or R/V [bit 7]	9	XEN	9	$\overline{\text{VSYNC}}$
10	D1 or R/V [bit 8]	10	GND	10	$\overline{\text{HSYNC}}$
11	D1 or R/V [bit 9]	11	XDIR	11	HREF
12	Comp, G/Y, or Luma [bit 0]	12	$\overline{\text{XHSYNC}}$	12	VREF
13	Comp, G/Y, or Luma [bit 1]	13	$\overline{\text{XVSYNC}}$	13	ODD IN
14	Comp, G/Y, or Luma [bit 2]	14	XPXCK	14	GND
15	Comp, G/Y, or Luma [bit 3]	15	XRS [bit 3]	15	NTSC/PAL
16	Comp, G/Y, or Luma [bit 4]	16	XRS [bit 2]	16	CLAMP pulse
17	Comp, G/Y, or Luma [bit 5]	17	XRS [bit 1]	17	RGB
18	Comp, G/Y, or Luma [bit 6]	18	XRS [bit 0]	18	
19	Comp, G/Y, or Luma [bit 7]	19	GND	19	
20	Comp, G/Y, or Luma [bit 8]	20	-5V	20	
21	Comp, G/Y, or Luma [bit 9]	21	-5V	21	LOCK
22	Chroma or B/U [bit 0]	22	-5V	22	D1
23	Chroma or B/U [bit 1]	23	GND	23	$\overline{\text{RESET}}$
24	Chroma or B/U [bit 2]	24	PGM_OUT	24	SCL
25	Chroma or B/U [bit 3]	25	-12V	25	GND
26	Chroma or B/U [bit 4]	26	-12V	26	SDA
27	Chroma or B/U [bit 5]	27	IE (input enable)	27	OE (output enable)
28	Chroma or B/U [bit 6]	28	GND	28	$\overline{\text{BLANK}}$ (DAC)
29	Chroma or B/U [bit 7]	29		29	
30	Chroma or B/U [bit 8]	30		30	
31	Chroma or B/U [bit 9]	31	+12V	31	+12V
32	GND	32	GND	32	GND

Preliminary Information

Related Products

- TMC2068P7C Decoder demonstration board
 - TMC2069P7C Triple D/A demonstration board
 - RAYDEMO software
- TMC2070P7C R-bus interface board

Notes:

Preliminary Information

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Preliminary Information

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Preliminary Information

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2067P7C	25°C	27 MHz	Commercial	5" by 4" Printed Circuit Board	TMC2067P7C

A schematic database is available in OrCAD™ format, along with EPROM maps. More information on the Altera FPGA is also available. Contact the factory.

The TMC2067P7C Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

FCC Compliance

This board is intended for the evaluation of Fairchild semiconductor components only. This product has not been approved by the Federal Communications Commission (FCC). This product is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.

Preliminary Information

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.