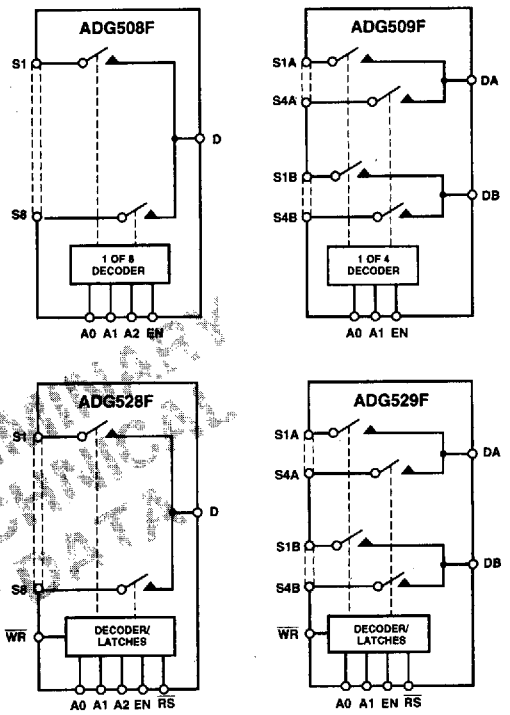
LC²MOS 4/8 Channel Fault-Protected Analog Multiplexers

ADG508F/ADG509F/ADG528F/ADG529F

FEATURES
- Wide Supply Ranges (10.8 V to 16.5 V)
- Low On Resistance (300 Ω max)
- Fast Switching Times
  - t_{ON} 300 ns max
  - t_{OFF} 300 ns max
- Low Power Dissipation (3.3 mW max)
- Fault and Overvoltage Protection
- All Switches OFF with Power Supply OFF
- ON Channel Turns OFF if Overvoltage Occurs
- Latch-Up Proof Construction
- Break-Before-Make Construction
- TTL and CMOS Compatible Inputs
- Superior Alternative to
  - MAX358/MAX359
  - DG458/DG459

APPLICATIONS
- Data Acquisition Systems
- Industrial and Process Control Systems
- Avionics Test Equipment
- Signal Routing Between Systems
- High Reliability Control Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG508F, ADG509F, ADG528F and ADG529F are CMOS analog multiplexers comprising eight single channels and four differential channels respectively which have fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs up to ±35 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources that drive the multiplexer.

The ADG508F/ADG509F/ADG528F/ADG529F are designed on an enhanced LC²MOS, trench-isolated process that provides low power dissipation yet gives high switching speed and low on resistance. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

The ADG508F and ADG528F switch one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG509F and ADG529F switch one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. The ADG528F and ADG529F have on-chip address and control latches that facilitate microprocessor interfacing. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS

1. Fault Protection
   The ADG508F/ADG509F/ADG528F/ADG529F can withstand continuous voltage inputs up to ±35 V. When a fault occurs, due to the power supplies being turned off or due to an overvoltage being applied to the ADG508F/ADG509F/ADG528F/ADG529F, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. Dual Supply Specifications with a Wide Tolerance
   The devices are specified in the 10.8 V to 16.5 V range.
3. Low R_{ON}
4. Fast Switching Times
5. Break-Before-Make Switching
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +10.8 V to +16.5 V, V_{SS} = −10.8 V to −16.5 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} + 3		V_{SS} + 3	V min	
		V_{DD} − 0.7		V_{DD} − 0.7	V max	
R_{ON}	300	400	300	400	Ω max	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 5%, V_{SS} = −15 V ± 5%
	200	250	200	250	Ω typ	−5 V ≤ V_S ≤ +5 V, I_S = 1 mA; V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%
R_{ON} Drift	0.6		0.6		%/°C typ	V_S = 0 V, I_{DS} = 1 mA
R_{ON} Match	5		5		% typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.02		±0.02		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.04		±0.04		nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG508F/ADG528F	±1	±100	±1	±100	nA max	Test Circuit 3
ADG509F/ADG529F	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.04		±0.04		nA typ	V_S = V_D = ±10 V;
ADG508F/ADG528F	±1	±100	±1	±100	nA max	Test Circuit 4
ADG509F/ADG529F	±1	±50	±1	±50	nA max	
FAULT						
Output Leakage Current	±0.02		±0.02		nA typ	V_S = ±33 V, V_D = 0 V
(With Overvoltage)		±2		±2	µA max	
Input Leakage Current	±0.005		±0.005		µA typ	V_S = ±25 V, V_D = ±25 V
(With Overvoltage)	±5		±10		µA max	
Input Leakage Current	±0.001		±0.001		µA typ	V_S = ±25 V, V_D = V_{EN} = 0 V,
(With Power Supplies Off)	±2		±5		µA max	V_{IN} = 0 V or 5 V
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		5		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	200		200		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 5
t_{OPEN}	50		50		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	25	10	25	10	ns max	V_S = +5 V; Test Circuit 6
t_{ON} (EN)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{SETT}, Settling Time						
0.1%		0.6		0.6	µs typ	
0.01%		1.7		1.7	µs typ	
t_W, Write Pulse Width	100	120	100	130	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	
Charge Injection	15		15		pC typ	V_S = 0 V, R_S = 0 Ω, C_L= 1 nF; Test Circuit 8
OFF Isolation	68		68		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	50		50		dB min	V_S = 7 V rms; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; Test Circuit 11
C_S (OFF)	5		5		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG508F/ADG528F	15		15		pF typ	
ADG509F/ADG529F	10		10		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05		0.05		mA typ	V_{IN} = V_{INL} or V_{INH}
	0.1	0.2	0.1	0.2	mA max	
I_{SS}	0.01		0.01		mA typ	
	0.1	0.2	0.1	0.2	mA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ABSOLUTE MAXIMUM RATINGS*

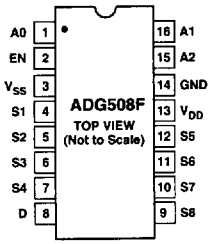
(T_A = +25°C unless otherwise noted)

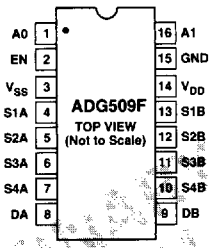
V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
V_{EN}, V_A Digital Input ..... V_{SS} – 4 V to V_{DD} + 4 V
V_S, Analog Input Overvoltage with Power ON. .... V_{SS} – 20 V to V_{DD} + 20 V
V_S, Analog Input Overvoltage with Power OFF ..... –35 V to +35 V
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) ..... 40 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Cerdip Package, Power Dissipation ..... 900 mW
θ_{JA}, Thermal Impedance ..... 76°C/W
Lead Temperature, Soldering (10 sec) ..... +300°C
Plastic Package, Power Dissipation ..... 470 mW
θ_{JA}, Thermal Impedance ..... 117°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 600 mW
θ_{JA}, Thermal Impedance. ..... 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
PLCC Package, Power Dissipation ..... 800 mW
θ_{JA}, Thermal Impedance ..... 90°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

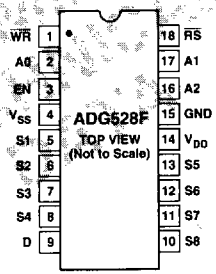
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

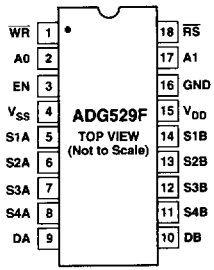
PIN CONFIGURATIONS

DIP

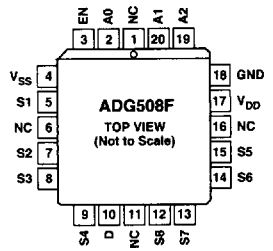


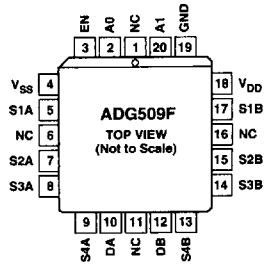


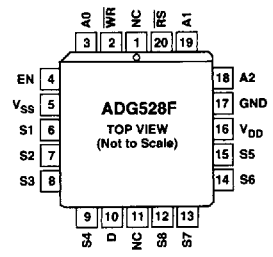


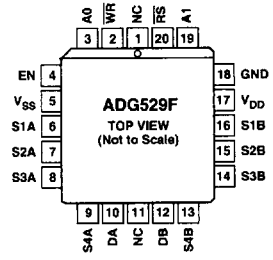


PLCC









NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508FBN	–40°C to +85°C	N-16
ADG508FBR	–40°C to +85°C	R-16A
ADG508FBP	–40°C to +85°C	P-20A
ADG508FTQ	–55°C to +125°C	Q-16
ADG509FBN	–40°C to +85°C	N-16
ADG509FBR	–40°C to +85°C	R-16A
ADG509FBP	–40°C to +85°C	P-20A
ADG509FTQ	–55°C to +125°C	Q-16
ADG528FBN	–40°C to +85°C	N-18
ADG528FBP	–40°C to +85°C	P-20A
ADG528FTQ	–55°C to +125°C	Q-18
ADG529FBN	–40°C to +85°C	N-18
ADG529FBP	–40°C to +85°C	P-20A
ADG529FTQ	–55°C to +125°C	Q-18

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

Table I. ADG508F Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG509F Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

Table III. ADG528F Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	↑	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

Table IV. ADG529F Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	↑	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care