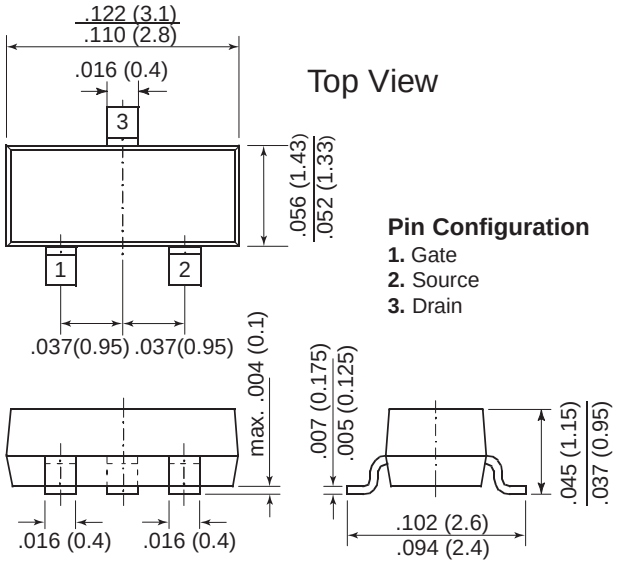
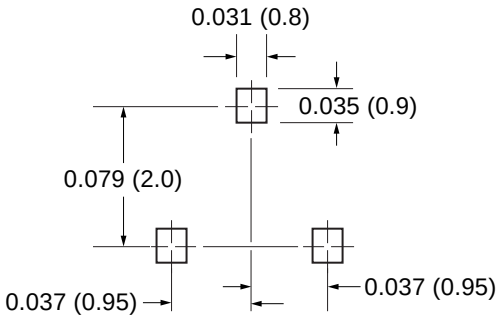
DMOS Transistor (N-Channel)

TO-236AB (SOT-23)



Pin Configuration
1. Gate
2. Source
3. Drain

Dimensions in inches and (millimeters)



Mounting Pad Layout

Features

- High input impedance
- High-speed switching
- No minority carrier storage time
- CMOS logic compatible input
- No thermal runaway
- No secondary breakdown

Mechanical Data

Case: SOT-23 Plastic Package
Weight: approx. 0.008g
Packaging Codes/Options:
E8/10K per 13" reel (8mm tape), 30K/box
E9/3K per 7" reel (8mm tape), 30K/box

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source-Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	250	mA
Power Dissipation at T_{SB} = 50°C	P_{tot}	0.310(1)	W
Thermal Resistance Junction to Substrate Backside	$R_{\theta SB}$	320(1)	°C/W
Thermal Resistance Junction to Ambient Air	$R_{\theta JA}$	450(1)	°C/W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

Note: (1) Ceramic Substrate 0.7mm; 2.5 cm^2 area

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100µA, V_{GS} = 0	60	80	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1.0	2.0	3.0	
Gate-Body Leakage Current	I_{GSS}	V_{GS} = 15V, V_{DS} = 0V	—	—	10	nA
Drain Cutoff Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	—	—	0.5	µA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 200mA	—	3.5	5.0	Ω
Forward Transconductance	g_m	V_{DS} = 10V, I_D = 200mA, f = 1MHz	—	200	—	mS
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0 f = 1MHz	—	30	—	pF
Turn-On Time	t_{on}	V_{GS} = 10V, V_{DS} = 10V R_D = 100Ω	—	5	—	ns
Turn-Off Time	t_{off}		—	25	—	ns

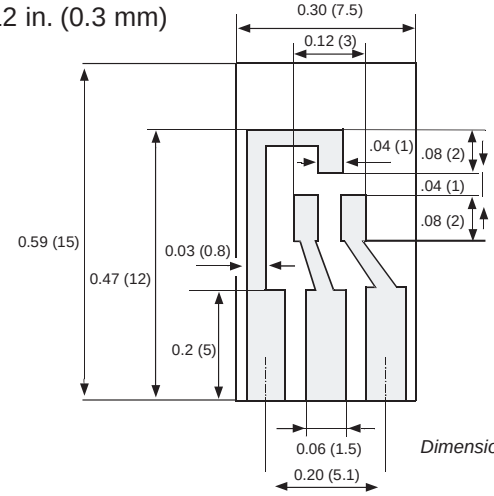
Note:
(1)Device on fiberglass substrate, see layout

Inverse Diode

Parameter	Symbol	Test Condition	Value	Unit
Max. Forward Current (continuous)	I_F	T_{amb} = 25 °C	0.3	A
Forward Voltage Drop (typ.)	V_F	V_{GS}= 0V, I_F = 0.3A T_j = 25°C	0.85	V

Layout for R_{thJA} test

Thickness: Fiberglass 0.059 in. (1.5 mm)
Copper leads 0.012 in. (0.3 mm)

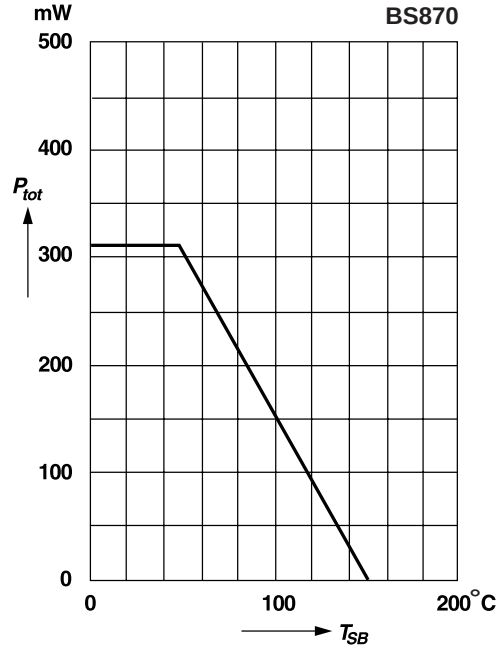


Dimensions in inches and (millimeters)

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

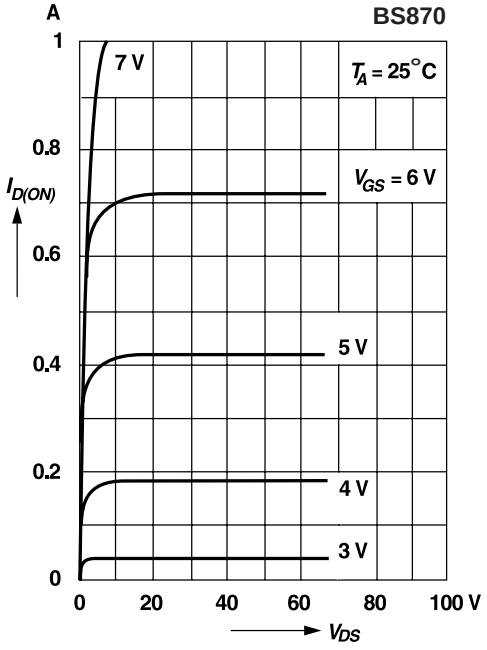
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



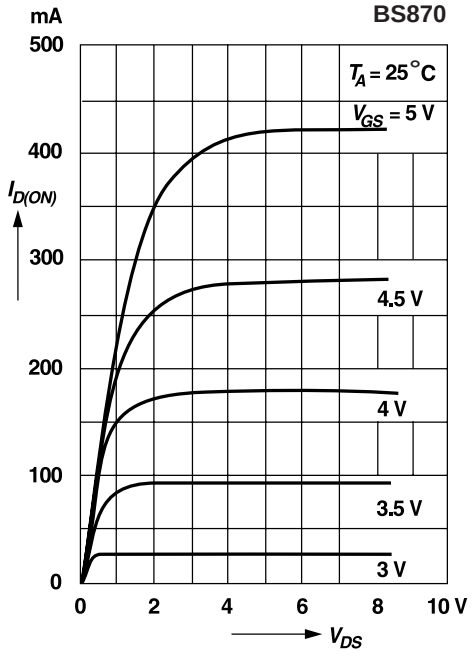
Output characteristics

Pulse test width 80 ms; pulse duty factor 1%.

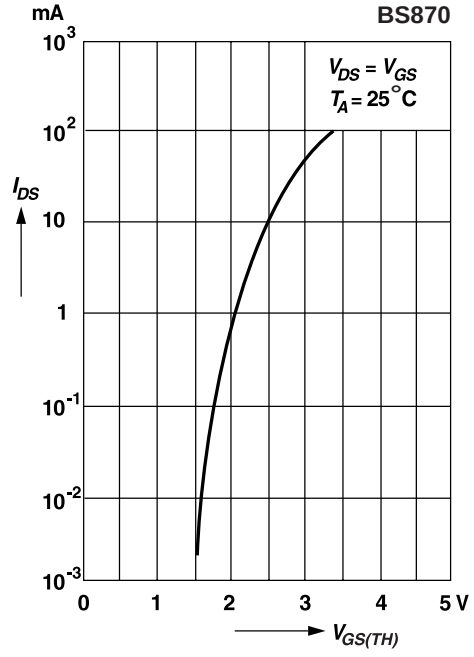


Saturation characteristics

Pulse test width 80 ms; pulse duty factor 1%.



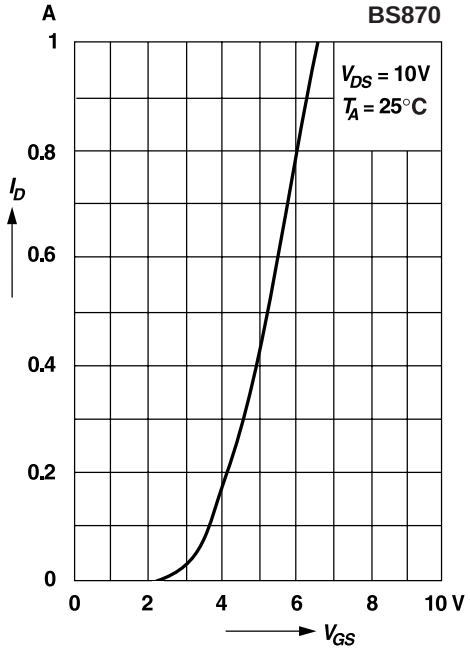
Drain-source current versus gate threshold voltage



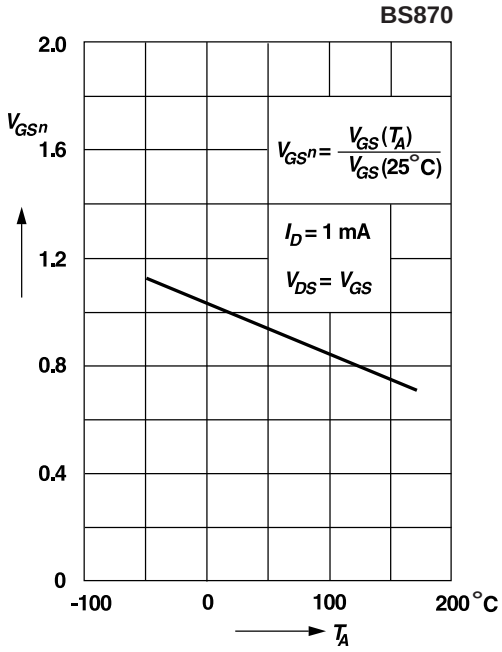
Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Drain current versus gate-source voltage

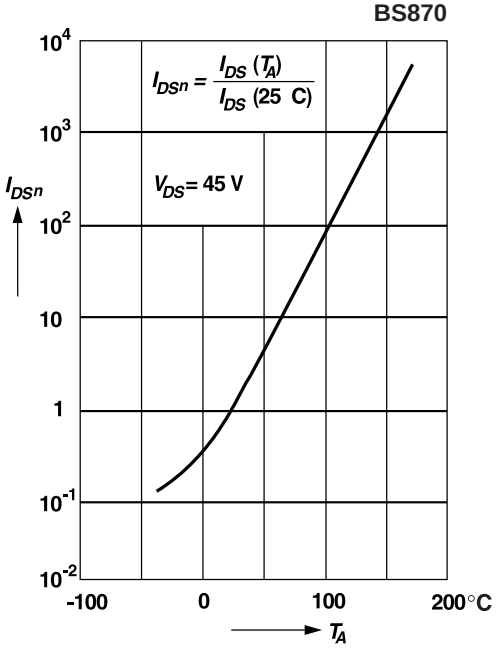
Pulse test width 80 ms; pulse duty factor 1%.



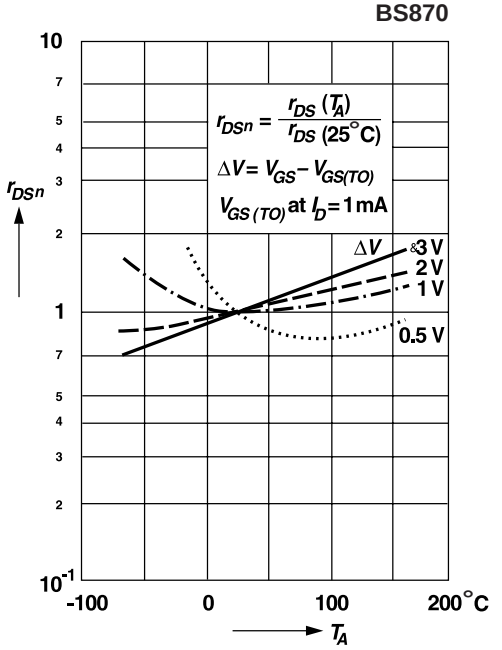
Normalized gate-source voltage versus temperature



Normalized drain-source current versus temperature

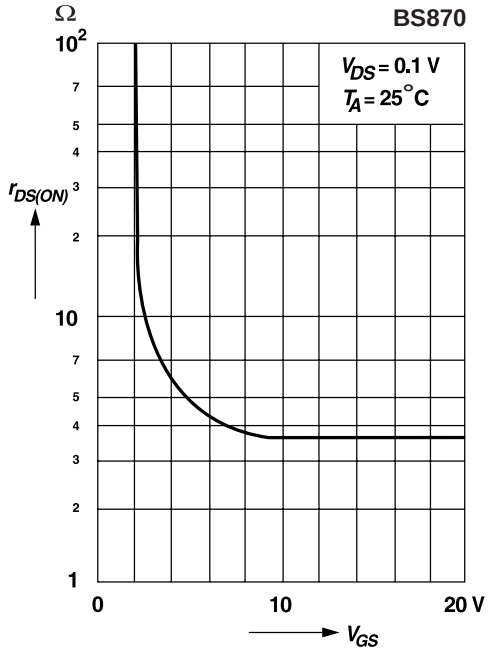


Normalized drain-source resistance versus temperature



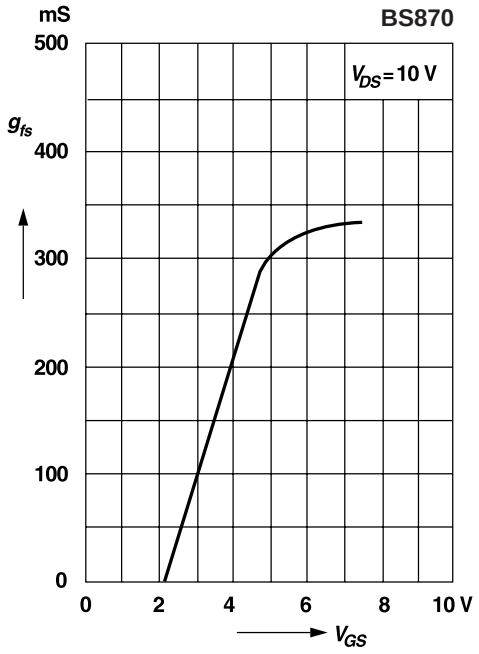
Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Drain-source resistance versus gate-source voltage



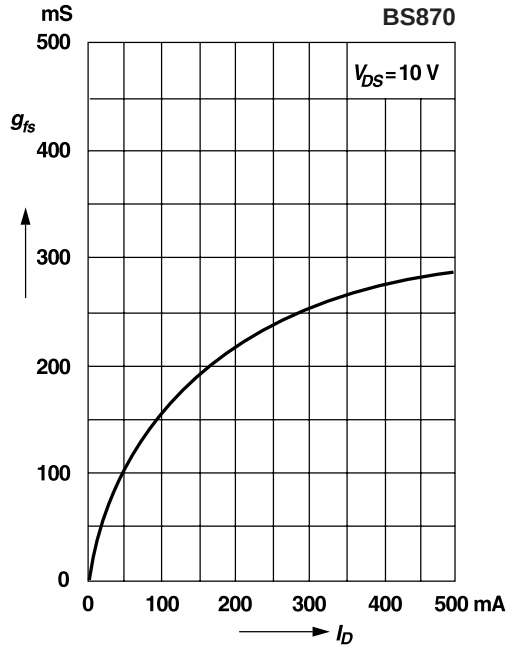
Transconductance versus gate-source voltage

Pulse test width 80 ms; pulse duty factor 1%



Transconductance versus drain current

Pulse test width 80 ms; pulse duty factor 1%



Capacitance versus drain-source voltage