NEC

Preliminary User's Manual

Memory Controller

NT85E500, NDT85E500V10, NT85E502

Target CPU Cores

NU85EA
NU85ET
NDU85ETV14

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Major Revisions in This Edition

Page	Description
Throughout	Addition of NDT85E500V10 (CB-12 Family L Type)
p.18	Addition of **Caution** in **1.1.3 (2) (c) Bus arbitration controller**
p.22	Addition of BUSST in **1.2.1 List of pin functions**
p.29	Addition of description in **1.2.2 (3) (k) DC3 to DC0**
p.30	Addition of **Figure 1-3 DCn Pin Timing**
p.30	Addition of description in **1.2.2 (3) (l) CSZ7 to CSZ0**
p.31	Addition of **1.2.2 (3) (r) BUSST**
pp.32, 33	Addition of description in **1.2.2 (4) NT85E502 connection pins**
pp.59, 60	Addition of **1.3.7 (3) Restriction related to page ROM access**
p.64	Addition of BUSST in **Figure 1-24 SRAM Read Timing (Bus Cycle Period Doubled)**
p.66	Addition of description in **1.4 Test Function**
p.64 in previous edition	Deletion of **1.4.1 Pin processing when in test mode**
p.94	Addition of VPDV in **2.2.3 Recommended connection of unused pins**
p.96	Addition of **Caution 4** in **2.3.1 SDRAM configuration register n (SCRn)**
pp.132, 133	Addition of **APPENDIX C REVISION HISTORY**

The mark ⋆ shows major revised points.

INTRODUCTION

Target Readers

This manual is intended for users who wish to understand the functions of the memory controllers (NT85E500, NDT85E500V10, NT85E502) for the NU85EA, NU85ET, and NDU85ETV14 CPU cores for CBICs and who design application systems using these CPU cores.

Memory Controller	Target CPU Core
NT85E500, NT85E502 (CB-10 Family VX Type)	NU85EA, NU85ET
NDT85E500V10 (CB-12 Family L Type)	NDU85ETV14

Purpose

This manual's purpose is to help the user understand the functions of the NT85E500, NDT85E500V10, and NT85E502.

Organization

This manual consists of the following.

CHAPTER 1 NT85E500

This chapter explains the NT85E500, which is the basic macro for controlling external memory.

The NT85E500 is a memory controller for the NU85EA, NU85ET, and NDU85ETV14. The NT85E500 and NDT85E500V10 contain an on-chip SRAM, I/O controller, and page ROM controller.

CHAPTER 2 NT85E502

This chapter explains the NT85E502, which is an SDRAM controller.

How to Use This Manual

This manual assumes that the reader has general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

To gain a general understanding of the NT85E500, NDT85E500V10, and NT85E502 functions:

→ Read this manual according to the **CONTENTS**.

To confirm details of a function, etc. when the name is known

→ Refer to **APPENDIX B INDEX**.

To know the functions of the NU85EA in detail:

→ Refer to **NU85E Hardware User's Manual (A14874E).**

To know the functions of the NU85ET and NDU85ETV14 in detail:

→ Refer to **NU85ET Hardware User's Manual (A15015E)**.

In this manual, unless specified otherwise, the NT85E500 and NT85E502 are described as the representative memory controller. When using the NDT85E500V10, read “NDT85E500V10” for the macro name of the memory controller (NT85E500).
The NU85EA is described as the representative CPU core. When using the NU85ET or NDU85ETV14, read “NU85ET” or “NDU85ETV14” for the CPU core name.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Z is appended to pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary … xxxx or xxxxB
	Decimal … xxxx
	Hexadecimal … xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data types:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- NU85E Hardware User’s Manual (A14874E)
- NU85ET Hardware User’s Manual (A15015E)
- CB-10 Family VX Type NU85E, NU85ET Design Manual (A15401E)
- CB-10 Family VX Type Core Library CPU Core, Peripheral Design Manual (A15133E)
- How to use SDRAM User’s Manual (E0123N[Note])
- Synchronous DRAM User’s Manual (E0124N[Note])

Note This is a document published by Elpida Memory, Inc. (http://www.elpida-memory.com/).

The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

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CHAPTER 1 NT85E500

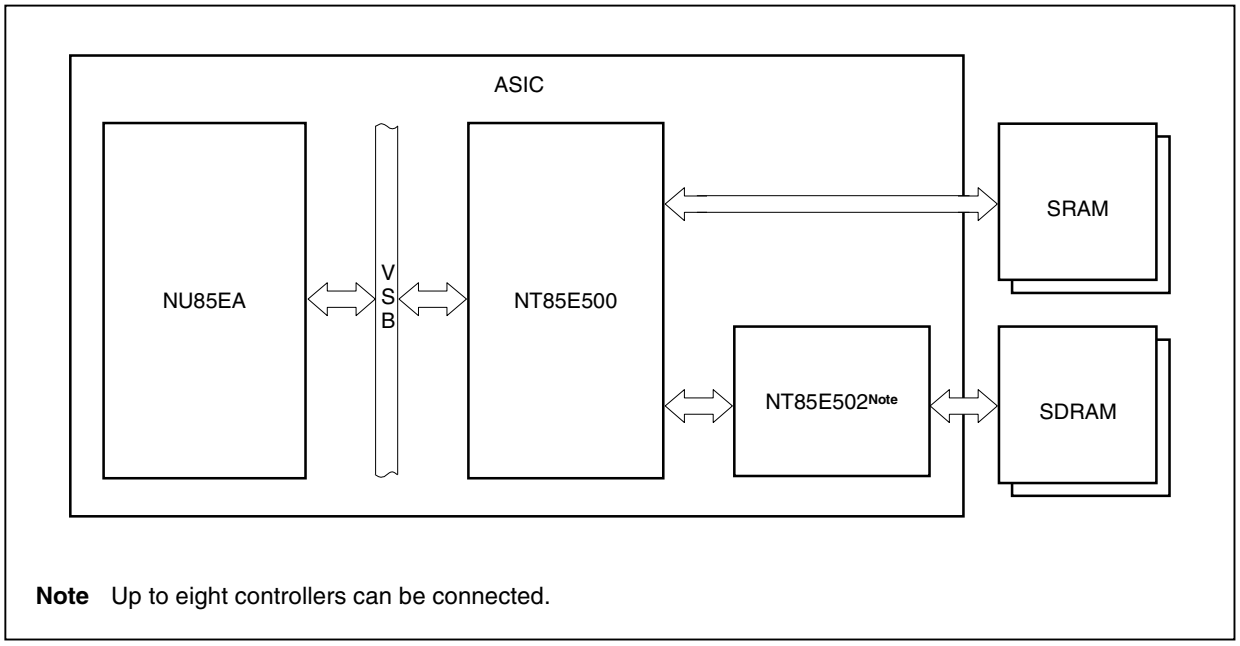
1.1 Outline

The NT85E500, which is the basic macro for controlling external memory, contains an on-chip SRAM, I/O controller, and page ROM controller.

An external bus cycle can be started by connecting the NT85E500 to the NU85EA via the VSB.

Also, SDRAM can be controlled by connecting the SDRAM controller (NT85E502) to the NT85E500 (see **Figure 1-1**).

Figure 1-1. SRAM and SDRAM Connection Example



Note Up to eight controllers can be connected.

1.1.1 Features

(1) SRAM-and-I/O controller

The NT85E500 has one on-chip SRAM-and-I/O controller, which controls access to all CSn areas (n = 7 to 0). Its main features are as follows.

- SRAM can be accessed in at least 2 states.
- Up to 7 programmable data wait states can be inserted by means of DWC0 and DWC1 register settings.
- Up to 3 address setting wait states can be inserted by means of an ASC register setting.
- The data wait can be controlled by WAITZ input.
- Up to 3 idle states can be inserted after a read/write cycle by means of a BCC register setting.
- A DMA flyby cycle[Note] (SRAM → I/O or I/O → SRAM) can be started.

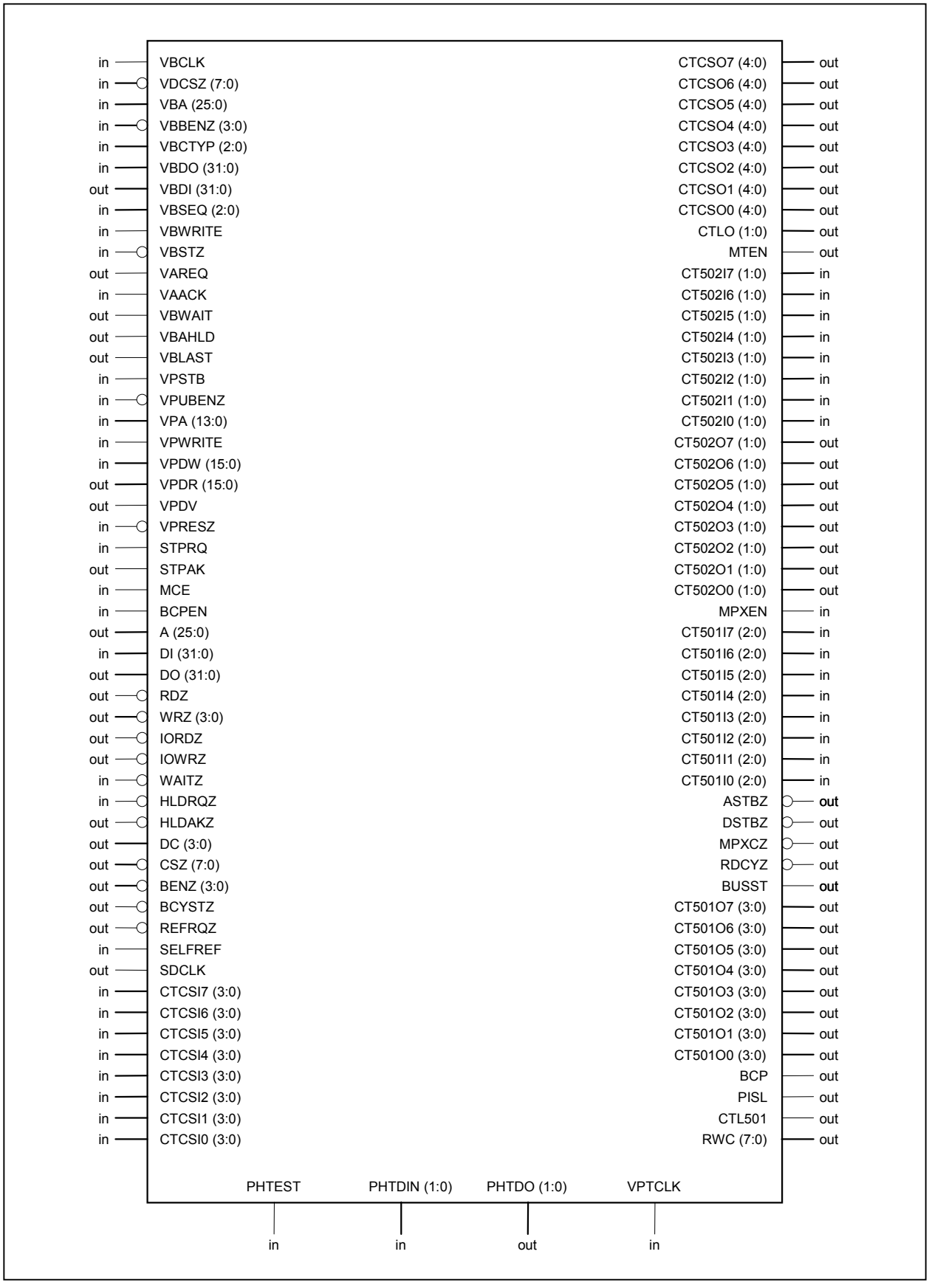
Note Flyby transfer using SDRAM is not supported.

(2) Page ROM controller

The NT85E500 has one on-chip page ROM controller, which controls access to all CSn areas (n = 7 to 0). The basic bus cycles are the same as those of the SRAM-and-I/O controller, but this controller has a page access function. Its main features are as follows.

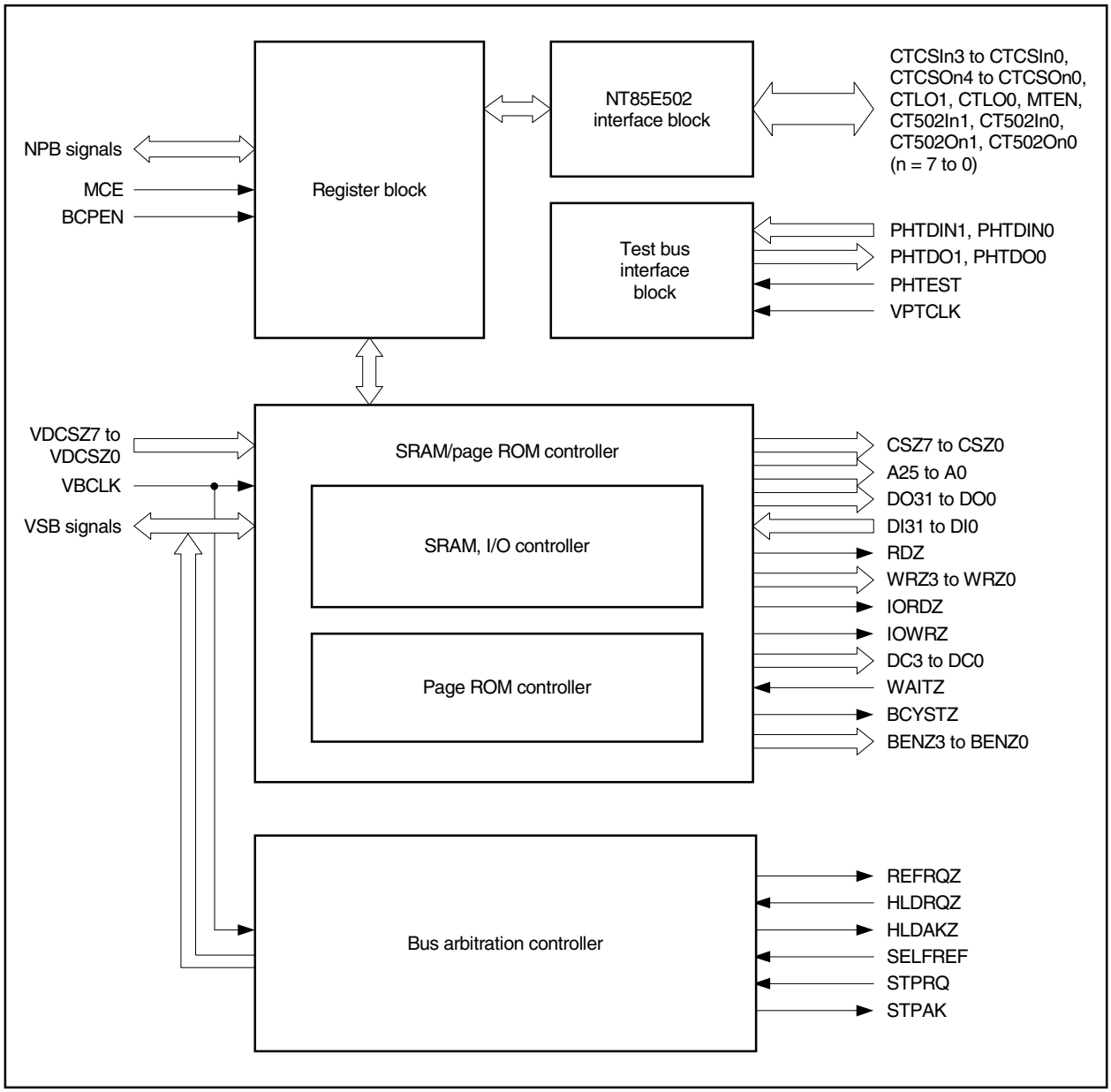
- Page ROM can be accessed in at least 2 states.
- An on-page judgement function is available.
- The address to be compared can be changed by means of a PRC register setting.
- For an on-page cycle, the active level (low level) for the RDZ signal is maintained while the VBSEQ2 to VBSEQ0 signals indicate consecutive transfer (except the value “VBSEQ2 to VBSEQ0 = 000”) until the VBSEQ2 to VBSEQ0 = 000 cycle is terminated.
- Up to 7 programmable data wait states can be inserted during an off-page cycle by means of DWC0 and DWC1 register settings.
- Up to 7 programmable data wait states can be inserted during an on-page cycle by means of a PRC register setting.
- The data wait can be controlled by WAITZ input.
- A DMA flyby cycle (page ROM → I/O) can be started.
- When there is a write cycle request for the CSn area to which the page ROM is connected, an SRAM write cycle is executed.

1.1.2 Symbol diagram



1.1.3 Block diagram

(1) Internal block diagram



(2) Internal units

(a) Register block

The register block contains on-chip registers for controlling the bus cycle. These registers can be used to select external memory, set the number of idle or wait states, or set the number of consecutive reads of page ROM.

Reading from or writing to the registers is done via the NPB.

(b) SRAM/page ROM controller

The SRAM/page ROM controller controls read and write operations for SRAM, page ROM, and external I/O. Access to all CSn areas can be controlled by this controller alone (n = 7 to 0).

(c) Bus arbitration controller

This controller controls the bus mastership. When one of the following signals is received by the NT85E500, the controller activates the bus mastership request signal (VAREQ) to establish the NT85E500 as the bus master.

- STOP mode request signal (STPRQ) from the NU85EA
- Self-refresh request signal (SELFREF)
- External bus hold request signal (HLDRQZ)
- CBR refresh request from the NT85E502

When the STPRQ signal is received, an acknowledge signal for the STPRQ signal (STPAK) is output to the NU85EA, and operation of the MEMC is stopped.

Also, if the STPRQ signal is received when the NT85E502 is connected, the STPAK signal will be output after execution of a self-refresh cycle.

The bus priority order is as follows.

External bus hold request > Refresh request > Bus request from inside the NU85EA

★ **Caution The NT85E500 does not output the VSB bus lock signal (VMLOCK). Therefore, when designing a bus arbiter in a system in which multiple master devices exist on the VSB, design it to assign top priority to the NT85E500, so that bus mastership is not passed to another master device while the NT85E500 has the bus mastership.**

(d) NT85E502 interface block

This is a block for interfacing with the NT85E502. It has a control signal for each CSn area (n = 7 to 0).

(e) Test bus interface block

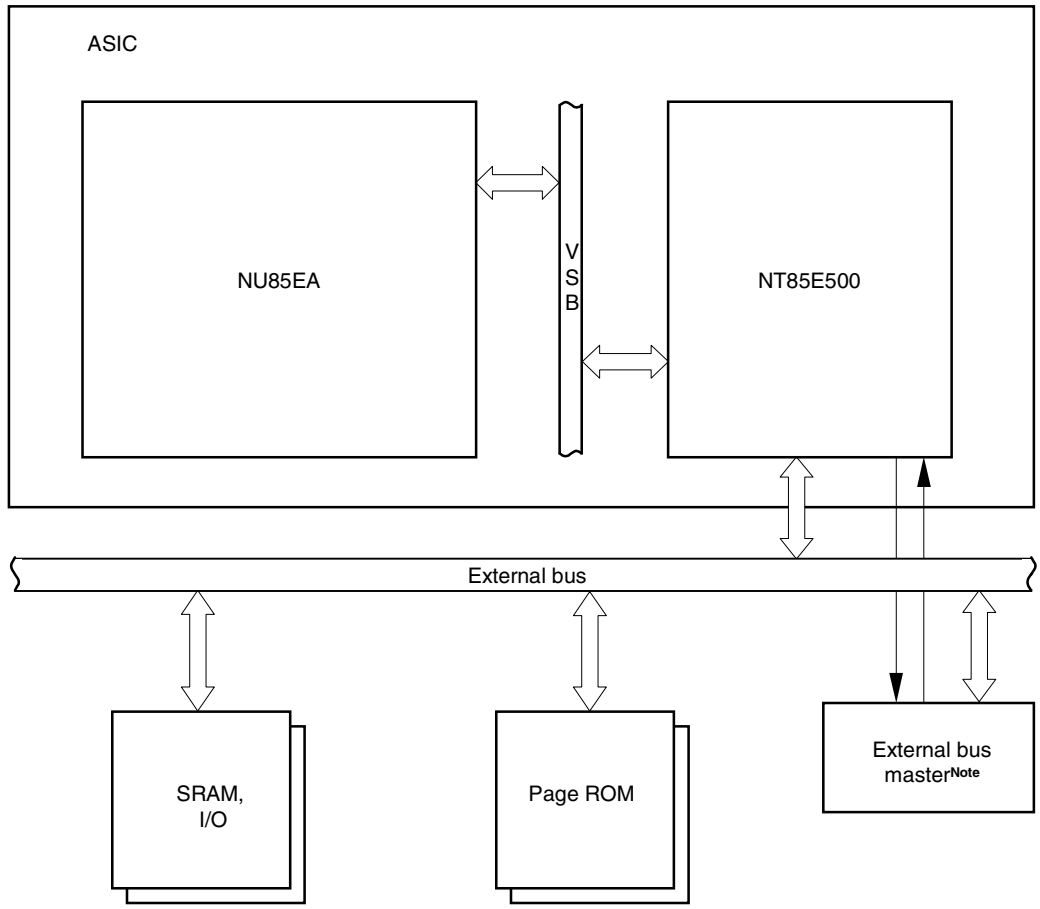
This is a block for interfacing with signals used for testing the NT85E500. The NT85E500 can be tested by using the CPU core test mode.

1.1.4 Configuration example

The NT85E500 starts bus cycles for external memory.

The following figure shows an application example using the NT85E500.

Figure 1-2. Application Example



Note The NT85E500 has an external bus master arbitration function, which is controlled by the HLDRQZ and HLDAKZ signals.

1.1.5 Functional differences between NT85E500 and NU85E500

Item		NT85E500	NU85E500
Target CPU core		NU85EA, NU85ET, NDU85ETV14	NB85E, NB85ET
VSB data bus (n = 31 to 0)		VBDIn (output), VBDOn (input)	VBDn (I/O)
NPB data bus (n = 15 to 0)		VPDWn (input), VPDRn (output)	VPDn (I/O)
NPB data output bus control pin		VPDV	(None)
VSB control pin		(None)	VBLOCK (I/O)
		(None)	VBTTYP1, VBTTYP0 (I/O)
		(None)	VBBSTR (I/O)
		(None)	VDSELPZ (I/O)
		VBBENZ3 to VBBENZ0 (input)	VBBENZ3 to VBBENZ0 (I/O)
		VBWRITE (input)	VBWRITE (I/O)
		VBSTZ (input)	VBSTZ (I/O)
		VDCSZ7 to VDCSZ0 (input)	VDCSZ7 to VDCSZ0 (I/O)
I/O timing	Data bus (n = 31 to 0)	VBDOn, VBDIn	VBDn
	Transfer response signal	VBWAIT, VBLAST, VBAHLD	
Pin status after reset, during idle	VBDI31 to VBDI0, VBWAIT, VBAHLD, VBLAST, VPDR15 to VPDR0	Low-level output	High impedance
	DO31 to DO0	Undefined	

1.2 Pin Functions

1.2.1 List of pin functions

(1/3)

Pin Name		I/O	Function
NU85EA connection pins	VBCLK	Input	Internal system clock input
	VDCSZ7 to VDCSZ0	Input	Chip select input (for VSB)
	VBA25 to VBA0	Input	Address input (for VSB)
	VBBENZ3 to VBBENZ0	Input	Byte enable input (for VSB)
	VBCTYP2 to VBCTYP0	Input	Bus cycle status input (for VSB)
	VBDO31 to VBDO0	Input	Data input (for VSB)
	VBDI31 to VBDI0	Output	Data output (for VSB)
	VBSEQ2 to VBSEQ0	Input	Sequential status input (for VSB)
	VBWRITE	Input	Read/write status input (for VSB)
	VBSTZ	Input	Transfer start input (for VSB)
	VAREQ	Output	Bus mastership request output (for VSB)
	VAACK	Input	Bus mastership request acknowledge input (for VSB)
	VBWAIT	Output	Wait response output (for VSB)
	VBAHLD	Output	Address hold response output (for VSB)
	VBLAST	Output	Last response output (for VSB)
	VPSTB	Input	Data strobe input (for NPB)
	VPUBENZ	Input	Higher byte enable input (for NPB)
	VPA13 to VPA0	Input	Address input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPDW15 to VPDW0	Input	Data input (for NPB)
	VPDR15 to VPDR0	Output	Data output (for NPB)
	VPDV	Output	Data output (VPDR15 to VPDR0) control output (for NPB)
	VPRESZ	Input	Reset input
	STPRQ	Input	STOP mode request input
	STPAK	Output	Acknowledge output for STPRQ input
Initialization pins	MCE	Input	BCT register MEn bit reset value control input (n = 7 to 0)
	BCPEN	Input	BCP register BCP bit reset value control input
External memory connection pins	A25 to A0	Output	External memory address output
	DI31 to DI0	Input	External memory data input
	DO31 to DO0	Output	External memory data output
	RDZ	Output	SRAM/page ROM read strobe output

(2/3)

Pin Name		I/O	Function
External memory connection pins	WRZ3 to WRZ0	Output	SRAM/page ROM write strobe output
	IORDZ	Output	External I/O read strobe output
	IOWRZ	Output	External I/O write strobe output
	WAITZ	Input	Wait request input
	HLDRQZ	Input	External bus hold request input
	HLDAKZ	Output	External bus hold request acknowledge output
	DC3 to DC0	Output	Data bus control output
	CSZ7 to CSZ0	Output	Chip select output
	BENZ3 to BENZ0	Output	Byte enable output
	BCYSTZ	Output	Bus cycle start status output
	REFRQZ	Output	Refresh status output
	SELFREF	Input	Self-refresh request input
	SDCLK	Output	SDRAM synchronization clock output
★	BUSST	Output	Bus strobe output
NT85E502 connection pins	CTCSI73 to CTCSI70	Input	Control input from NT85E502 (for CS7 area)
	CTCSI63 to CTCSI60	Input	Control input from NT85E502 (for CS6 area)
	CTCSI53 to CTCSI50	Input	Control input from NT85E502 (for CS5 area)
	CTCSI43 to CTCSI40	Input	Control input from NT85E502 (for CS4 area)
	CTCSI33 to CTCSI30	Input	Control input from NT85E502 (for CS3 area)
	CTCSI23 to CTCSI20	Input	Control input from NT85E502 (for CS2 area)
	CTCSI13 to CTCSI10	Input	Control input from NT85E502 (for CS1 area)
	CTCSI03 to CTCSI00	Input	Control input from NT85E502 (for CS0 area)
	CTCSO74 to CTCSO70	Output	Control output to NT85E502 (for CS7 area)
	CTCSO64 to CTCSO60	Output	Control output to NT85E502 (for CS6 area)
	CTCSO54 to CTCSO50	Output	Control output to NT85E502 (for CS5 area)
	CTCSO44 to CTCSO40	Output	Control output to NT85E502 (for CS4 area)
	CTCSO34 to CTCSO30	Output	Control output to NT85E502 (for CS3 area)
	CTCSO24 to CTCSO20	Output	Control output to NT85E502 (for CS2 area)
	CTCSO14 to CTCSO10	Output	Control output to NT85E502 (for CS1 area)
	CTCSO04 to CTCSO00	Output	Control output to NT85E502 (for CS0 area)
	CTLO1, CTLO0	Output	Control output to NT85E502
	MTEN	Output	Test mode enable output to NT85E502
	CT502I71, CT502I70	Input	Control input from NT85E502 (for CS7 area)
	CT502I61, CT502I60	Input	Control input from NT85E502 (for CS6 area)
	CT502I51, CT502I50	Input	Control input from NT85E502 (for CS5 area)
	CT502I41, CT502I40	Input	Control input from NT85E502 (for CS4 area)
	CT502I31, CT502I30	Input	Control input from NT85E502 (for CS3 area)
	CT502I21, CT502I20	Input	Control input from NT85E502 (for CS2 area)
	CT502I11, CT502I10	Input	Control input from NT85E502 (for CS1 area)

(3/3)

Pin Name		I/O	Function
NT85E502 connection pins	CT502I01, CT502I00	Input	Control input from NT85E502 (for CS0 area)
	CT502O71, CT502O70	Output	Control output to NT85E502 (for CS7 area)
	CT502O61, CT502O60	Output	Control output to NT85E502 (for CS6 area)
	CT502O51, CT502O50	Output	Control output to NT85E502 (for CS5 area)
	CT502O41, CT502O40	Output	Control output to NT85E502 (for CS4 area)
	CT502O31, CT502O30	Output	Control output to NT85E502 (for CS3 area)
	CT502O21, CT502O20	Output	Control output to NT85E502 (for CS2 area)
	CT502O11, CT502O10	Output	Control output to NT85E502 (for CS1 area)
	CT502O01, CT502O00	Output	Control output to NT85E502 (for CS0 area)
Test mode pins (connected to NU85EA)	PHTEST	Input	Peripheral test mode status input
	PHTDIN1, PHTDIN0	Input	Peripheral macro test input
	PHTDO1, PHTDO0	Output	Peripheral macro test output
	VPTCLK	Input	Test clock input
NEC reserved pins	MPXEN	Input	NEC reserved pin (Input low level)
	CT501I72 to CT501I70	Input	
	CT501I62 to CT501I60	Input	
	CT501I52 to CT501I50	Input	
	CT501I42 to CT501I40	Input	
	CT501I32 to CT501I30	Input	
	CT501I22 to CT501I20	Input	
	CT501I12 to CT501I10	Input	
	CT501I02 to CT501I00	Input	
	ASTBZ	Output	NEC reserved pin (Leave open)
	DSTBZ	Output	
	MPXCZ	Output	
	RDCYZ	Output	
	BUSST	Output	
	CT501O73 to CT501O70	Output	
	CT501O63 to CT501O60	Output	
	CT501O53 to CT501O50	Output	
	CT501O43 to CT501O40	Output	
	CT501O33 to CT501O30	Output	
	CT501O23 to CT501O20	Output	
	CT501O13 to CT501O10	Output	
	CT501O03 to CT501O00	Output	
	BCP	Output	
	PISL	Output	
	CTL501	Output	
	RWC7 to RWC0	Output	

1.2.2 Explanation of pin functions

(1) NU85EA connection pins

(a) VBCLK (input)

This is the external clock input pin for the internal system clock. A 50% duty stable clock is input from an external clock controller.

(b) VDCSZ7 to VDCSZ0 (input)

These are chip select pins and are connected to the VDCSZ7 to VDCSZ0 pins of the NU85EA.

The NU85EA's chip area select control registers (CSC0, CSC1) are used to set the VDCSZn signal corresponding to the relevant bank of the data area and set multiple blocks (CSn area) consisting of arbitrary bank combinations (n = 7 to 0). For further details, refer to the **NU85E Hardware User's Manual (A14874E).**

(c) VBA25 to VBA0 (input)

These pins constitute an address input bus for the VSB and are connected to the VMA25 to VMA0 pins of the NU85EA.

(d) VBBENZ3 to VBBENZ0 (input)

These are low-level active pins that indicate the valid byte data out of the four data bus (VBDI31 to VBDI0, VBDO31 to VBDO0) parts and are connected to the VMBENZ3 to VMBENZ0 pins of the NU85EA.

Table 1-1. VBBENZ3 to VBBENZ0 Signals

Active (Low Level) Signal	Valid Byte Data
VBBENZ3	VBDI31 to VBDI24, VBDO31 to VBDO24
VBBENZ2	VBDI23 to VBDI16, VBDO23 to VBDO16
VBBENZ1	VBDI15 to VBDI8, VBDO15 to VBDO8
VBBENZ0	VBDI7 to VBDI0, VBDO7 to VBDO0

(e) VBCTYP2 to VBCTYP0 (input)

These are pins that input the current bus cycle status and are connected to the VMCTYP2 to VMCTYP0 pins of the NU85EA.

Table 1-2. VBCTYP2 to VBCTYP0 Signals

VBCTYP2	VBCTYP1	VBCTYP0	Bus Cycle Status
0	0	0	Opcode fetch
0	0	1	Data access
0	1	0	Misalign access
0	1	1	Read modify write access
1	0	0	Opcode fetch of jump address due to branch instruction
1	1	0	DMA 2-cycle transfer
1	1	1	DMA flyby transfer
1	0	1	(Reserved for future function expansion)

Remark 0: Low-level input 1: High-level input

(f) VBDO31 to VBDO0 (input)

These pins constitute a data input bus for macro connected to VSB and are connected to the VBDO31 to VBDO0 pins of the NU85EA.

(g) VBDI31 to VBDI0 (output)

These pins constitute a data output bus for macro connected to VSB and are connected to the VBDI31 to VBDI0 pins of the NU85EA.

(h) VBSEQ2 to VBSEQ0 (input)

These are pins that input the sequential status indicating the transfer size during burst transfer and are connected to the VMSEQ2 to VMSEQ0 pins of the NU85EA.

These pins indicate “burst transfer length” at the start of burst transfer, “continuous” during burst transfer, and “single transfer” at the end of burst transfer.

Table 1-3. VBSEQ2 to VBSEQ0 Signals

VBSEQ2	VBSEQ1	VBSEQ0	Sequential Status
0	0	0	Single transfer
0	0	1	Continuous (indicates that the next transfer address is related to the current transfer address)[Note]
0	1	0	Continuous 4 times (burst transfer length: 4)
0	1	1	Continuous 8 times (burst transfer length: 8)
1	0	0	Continuous 16 times (burst transfer length: 16)
1	0	1	Continuous 32 times (burst transfer length: 32)
1	1	0	Continuous 64 times (burst transfer length: 64)
1	1	1	Continuous 128 times (burst transfer length: 128)

Note This is output during continuous 2 times, or continuous 4, 8, 16, 32, 64, or 128 times transfer.

Remark 0: Low-level input 1: High-level input

(i) VBWRITE (input)

This is an input pin that indicates the transfer direction and is connected to the VMWRITE pin of the NU85EA.

It inputs a high level during write.

(j) VBSTZ (input)

This is an input pin that indicates the start of transfer and is connected to the VMSTZ pin of the NU85EA.

(k) VAREQ (output)

This is the pin that outputs the bus mastership request signal and is connected to the VAREQ pin of the NU85EA.

(l) VAACK (input)

This is an input pin that indicates the reception of the bus mastership request signal (VAREQ) and is connected to the VAACK pin of the NU85EA.

(m) VBWAIT (output)

This is the wait response pin and is connected to the VMWAIT pin of the NU85EA.

This signal is output to the bus master to request additional bus cycles because the data output preparations have not completed.

When this signal becomes high level, the bus cycle changes to the wait status.

(n) VBAHLD (output)

This is the address hold response pin and is connected to the VMAHLD pin of the NU85EA.

This signal is output to the bus master to request additional bus cycles when the data output preparations have completed. When this signal and the VBWAIT signal become high level, the bus cycle goes into the address hold status.

Since, in the address hold status, addresses do not change even during the data read and write cycles, there is no need to latch addresses and the circuit can thus be kept simple.

When the number of idle states is set to 1 or more (BCn1 and BCn0 bits of BCC register = 01B or more), the NT85E500 activates the VBAHLD signal during the idle state at the end of the read cycle of an SRAM or page ROM.

(o) VBLAST (output)

This is the last response pin and is connected to the VMLAST pin of the NU85EA. This pin is used when the bus decoder requires a decode cycle.

In the case of a system where several slave devices are connected externally and a bus decoder has been added to select slaves, decoding for bus slave selection is normally performed during non-sequential transfer. Thus even when attempts to change a slave device are made during sequential transfer such as burst transfer, the decode cycle for slave selection cannot be issued.

In such a case, the slave device outputs a last response notifying the fact that the slave selection signal has changed to the bus master. When there is a last response from the slave device, the bus master makes the next bus cycle non-sequential transfer to enable decode cycle issuance.

The NT85E500 cannot activate the VBLAST signal.

(p) VPSTB (input)

This is the data strobe input pin for the VPDW15 to VPDW0 signals and is connected to the VPSTB pin of the NU85EA.

(q) VPUBENZ (input)

This is the higher byte enable input pin and is connected to the VPUBENZ pin of the NU85EA.
It inputs a low level during a halfword data access or a byte data access to an odd address.
It inputs a high level during a byte access to an even address.

(r) VPA13 to VPA0 (input)

These are address input pins for NPB and are connected to the VPA13 to VPA0 pins of the NU85EA.
They specify the lower 14 bits.

(s) VPWRITE (input)

This is the write access strobe input pin for the VPDO15 to VPDO0 signals output from the NU85EA and is connected to the VPWRITE pin of the NU85EA.
It inputs a high level during write.

(t) VPDW15 to VPDW0 (input)

These pins constitute a bus for data input from the NU85EA and are connected to the VPDO15 to VPDO0 pins of the NU85EA.

(u) VPDR15 to VPDR0 (output)

These pins constitute a bus for data output to the NU85EA and are connected to the VPDI15 to VPDI0 pins of the NU85EA.

(v) VPDV (output)

This is the data output (VPDR15 to VPDR0) control pin. It outputs a high level during read. To configure a bidirectional data bus, connect this pin to the 3-state buffer enable pin connected to the data bus for data output control.
This pin is not used when connecting with the NU85EA, therefore leave this pin open.

(w) VPRESZ (input)

This is the input pin for a system reset output from the NU85EA and is connected to the VPRESZ pin of the NU85EA.

(x) STPRQ (input)

This is the input pin for a hardware/software STOP mode request from the NU85EA and is connected to the STPRQ pin of the NU85EA.

(y) STPAK (output)

This is the output pin from which the acknowledge signal is sent to the NU85EA upon receipt of the STPRQ signal and is connected to the STPAK pin of the NU85EA.

(2) Initialization pins

(a) MCE (input)

This is a pin for specifying whether MEMC operation is enabled when a reset occurs.
The reset value of the MEn bit of the BCT0 or BCT1 register is as follows according to the level input to this pin (n = 7 to 0).
Make sure that the level of this pin does not change before and after reset.

- Low level: 0 (MEMC operation is disabled)
- High level: 1 (MEMC operation is enabled)

(b) BCPEN (input)

This is a pin for specifying the length of the bus cycle period when a reset occurs.
The reset value of the BCP bit of the BCP register is as follows according to the level input to this pin.
Make sure that the level of this pin does not change before and after reset.

- Low level: 0 (normal)
- High level: 1 (double)

(3) External memory connection pins

(a) A25 to A0 (output)

These pins constitute the external memory address bus.
When the NT85E502 is active, all of the pins A25 to A0 output a low-level signal.

(b) DI31 to DI0 (input)

These pins constitute the data input bus for external memory.

(c) DO31 to DO0 (output)

These pins constitute the data output bus for external memory.

(d) RDZ (output)

This is the read strobe output pin for making SRAM or page ROM active.

(e) WRZ3 to WRZ0 (output)

These are the write strobe output pins for making SRAM or external I/O active.

WRZ3 … For DO31 to DO24
WRZ2 … For DO23 to DO16
WRZ1 … For DO15 to DO8
WRZ0 … For DO7 to DO0

(f) IORDZ (output)

This is the read strobe output pin for making external I/O active during a DMA flyby cycle.

(g) IOWRZ (output)

This is the write strobe output pin for making external I/O active during a DMA flyby cycle.

(h) WAITZ (input)

This is the pin to which a wait request is input from external memory.

(i) HLDRQZ (input)

This is the pin to which a bus hold request is input from an external source.
An active level must be retained during a bus hold.

(j) HLDAKZ (output)

This is the pin from which a bus hold acknowledge is output to an external source.
It indicates that a bus hold is permitted.

★ **(k) DC3 to DC0 (output)**

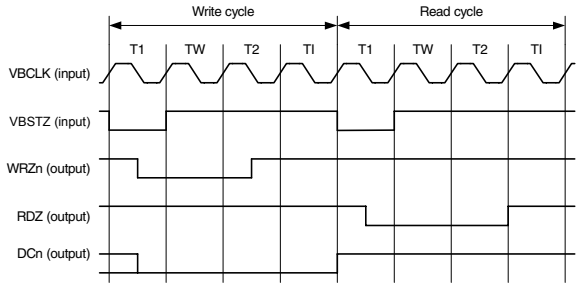
These are the output pins for controlling the data bus I/O buffer direction.
They output a high level when a read is performed and a low level when a write is performed.
They output a high level during a DMA flyby transfer.

DC3 … For DI31 to DI24, DO31 to DO24
DC2 … For DI23 to DI16, DO23 to DO16
DC1 … For DI15 to DI8, DO15 to DO8
DC0 … For DI7 to DI0, DO7 to DO0

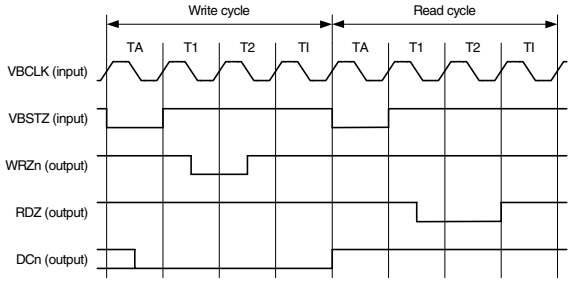
The DCn pin retains a low level for a write cycle and a high level for a read cycle during the TI cycle (n = 3 to 0). This pin becomes high level at the rising edge of the first VBCLK in the read cycle and low level at the falling edge of the first VBCLK in the write cycle (unaffected by the TA state and TI state).
This pin outputs a low level for the consecutive write cycle of SRAM (see **Figure 1-3 (c)**).

★ **Figure 1-3. DCn Pin Timing**

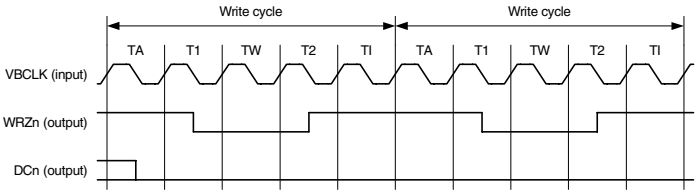
(a) Write cycle → read cycle (TA = 0, TW = 1)



(b) Write cycle → read cycle (TA = 1, TW = 0)



(c) Consecutive write cycle of SRAM



Remark n = 3 to 0

(l) CSZ7 to CSZ0 (output)

These are the chip select output pins.

The values input to the VDCSZ7 to VDCSZ0 pins are output from these pins.

★ However, when the NT85E502 is connected and executes a register write cycle or refresh cycle, the values input to the CT502I71 to CT502I01 pins are output from these pins.

CSZ7 ... For CS7 area
CSZ6 ... For CS6 area
CSZ5 ... For CS5 area
CSZ4 ... For CS4 area
CSZ3 ... For CS3 area
CSZ2 ... For CS2 area
CSZ1 ... For CS1 area
CSZ0 ... For CS0 area

(m) BENZ3 to BENZ0 (output)

These are the byte enable output pins. The values input to the VBBENZ3 to VBBENZ0 pins are output from these pins.

(n) BCYSTZ (output)

This is the pin for indicating the bus cycle start status.

(o) REFRQZ (output)

This is the pin for indicating the execution status of the refresh cycle to SDRAM. It is used when an NT85E502 is connected.

This pin outputs a low level when a refresh cycle is executed and a high level when a refresh cycle is not executed.

If this pin outputs a low level during a bus hold, it indicates that a refresh request has been generated for the external bus master.

(p) SELFREF (input)

This is the self-refresh request input pin. It is used when an NT85E502 is connected.

The input level to this pin indicates whether or not there is a self-refresh request.

- Low level: There is no self-refresh request.
- High level: There is a self-refresh request.

(q) SDCLK (output)

This is the synchronization clock output pin for external SDRAM. It is used when an NT85E502 is connected.

★ **(r) BUSST (output)**

This is the bus strobe output pin (1/2 frequency of VBCLK).

It rises at the TD cycle and falls at the T1, T2, TA, TW, or TI cycle.

★ **(4) NT85E502 connection pins**

(a) CTCSIn3 (n = 7 to 0) (input)

This is the status signal input pin indicating that a refresh cycle is under execution. It is input from the NT85E502 for each CSn area (n = 7 to 0).

(b) CTCSIn2 (n = 7 to 0) (input)

This is the input pin indicating the end of self-refresh. It is input from the NT85E502 for each CSn area (n = 7 to 0).

(c) CTCSIn1 (n = 7 to 0) (input)

This is the refresh request signal input pin. It is input from the NT85E502 for each CSn area (n = 7 to 0).

(d) CTCSIn0 (n = 7 to 0) (input)

This is the test input pin. It is input from the NT85E502 for each CSn area (n = 7 to 0).

(e) CTCSOn4 (n = 7 to 0) (output)

This is the BCn1 bit output pin of the BCC register of the NT85E500. It is output to the NT85E502 for each CSn area (n = 7 to 0).

(f) CTCSOn3 (n = 7 to 0) (output)

This is the BCn0 bit output pin of the BCC register of the NT85E500. It is output to the NT85E502 for each CSn area (n = 7 to 0).

(g) CTCSOn2 (n = 7 to 0) (output)

This is the refresh enable signal output pin. It is output to the NT85E502 for each CSn area (n = 7 to 0).

(h) CTCSOn1 (n = 7 to 0) (output)

This is the BTn0 bit output pin of the BCT1 and BCT0 registers of the NT85E500. It is output to the NT85E502 for each CSn area (n = 7 to 0). When this pin becomes low level, the refresh counter of the NT85E502 is initialized asynchronously. An SDRAM cycle is not generated during low level.

(i) CTCSOn0 (n = 7 to 0) (output)

This is the MEn bit output pin of the BCT1 and BCT0 registers of the NT85E500. It is output to the NT85E502 for each CSn area (n = 7 to 0). When this pin becomes low level, the NT85E502 state is initialized asynchronously. An SDRAM cycle is not generated during low level.

(j) CTLO1 and CTLO0 (output)

These are pins for controlling output to the NT85E502.

(k) MTEN (output)

This is the output pin for specifying whether test mode is enabled for the NT85E502.

(l) CT502In1 (n = 7 to 0) (input)

This is the CSn input pin from the NT85E502 when a refresh is generated (n = 7 to 0).
The CSZn signal of the NT85E500 selects whether CSn from VDCSZ or CSn from the NT85E502 is input with this signal.

(m) CT502In0 (n = 7 to 0) (input)

This is the input pin indicating the status of the power-on sequence. It is input from the NT85E502 for each CSn area (n = 7 to 0).

This pin outputs a high level during SDRAM power-on sequence execution after the SCRn register is written.

(n) CT502On1 (n = 7 to 0) (output)

This is the output pin for selecting the SCRn register. It is output to the NT85E502 for each CSn area (n = 7 to 0).

A write operation is performed to the internal registers of the NT85E502 using the ANDed signal of this signal and the VPSTB signal.

(o) CT502On0 (n = 7 to 0) (output)

This is the output pin for selecting the RFSn register. It is output to the NT85E502 for each CSn area (n = 7 to 0).

A write operation is performed to the internal registers of the NT85E502 using the ANDed signal of this signal and the VPSTB signal.

(5) Test mode pins

(a) PHTEST (input)

This is the status input pin, which indicates the test mode status of the MEMC.

It is connected to the PHTEST pin of the NU85EA.

(b) PHTDIN1 and PHTDIN0 (input)

These are the test input pins.

(c) PHTDO1 and PHTDO0 (output)

These are the test output pins.

(d) VPTCLK (input)

This is the test clock input pin.

(6) NEC reserved pins

(a) MPXEN, CT501In2 to CT501In0 (n = 7 to 0) (input)

These are NEC reserved pins. Be sure to input a low level.

(b) ASTBZ, DSTBZ, MPXCZ, RDCYZ, CT501On3 to CT501On0 (n = 7 to 0), BCP, PISL, CTL501, and RWC7 to RWC0 (output)

These are NEC reserved pins. Leave open.

1.2.3 Recommended connection of unused pins

Pin Name		I/O	Recommended Connection Method
NU85EA connection pins	VBCLK, VDCSZ7 to VDCSZ0,VBA25 to VBA0, VBBENZ3 to VBBENZ0,VBCTYP2 to VBCTYP0, VBDO31 to VBDO0, VBSEQ2 to VBSEQ0, VBWRITE, VBSTZ, VAACK, VPSTB, VPUBENZ, VPA13 to VPA0, VPWRITE, VPDW15 to VPDW0, VPRESZ, STPRQ	Input	Always connected
	VBDI31 to VBDI0, VAREQ, VBWAIT, VBAHLD, VBLAST, VPDR15 to VPDR0, STPAK	Output	
	VPDV	Output	Leave open.
Initialization pins	MCE	Input	Input high level.
	BCPEN	Input	Input low level.
External memory connection pins	A25 to A0, DO31 to DO0, RDZ, WRZ3 to WRZ0, IORDZ, IOWRZ, HLDAKZ, DC3 to DC0, CSZ7 to CSZ0, BENZ3 to BENZ0, BCYSTZ, REFRQZ, SDCLK	Output	Leave open.
	DI31 to DI0	Input	Input low level or high level.
	WAITZ, HLDRQZ	Input	Input high level.
	SELFREF	Input	Input low level.
NT85E502 connection pins (n = 7 to 0)	CTCSIn3 to CTCSIn0, CT502In1, CT502In0	Input	Input low level.
	CTCSOn4 to CTCSOn0, CTLO1, CTLO0, MTEN, CT502On1, CT502On0	Output	Leave open.
Test mode pins	PHTEST, PHTDIN1, PHTDIN0, VPTCLK	Input	—
	PHTDO1, PHTDO0	Output	
NEC reserved pins (n = 7 to 0)	MPXEN, CT501In2 to CT501In0	Input	Input low level.
	ASTBZ, DSTBZ, MPXCZ, RDCYZ, BUSST, CT501On3 to CT501On0, BCP, PISL, CTL501, RWC7 to RWC0	Output	Leave open.

1.2.4 Pin status

The following table shows the status in each operating mode of the pins that have output functions.

Table 1-4. Pin Status in Each Operating Mode

Pin Name		Pin Status				
		Reset	STOP Mode	HALT Mode	Bus Hold	Test Mode
NU85EA connection pins	VBDI31 to VBDI0	L	L	Operating	L	Operating
	VAREQ	L	H	Operating	H	Operating
	VBWAIT	L	L	Operating	L	Operating
	VBAHLD	L	L	Operating	L	Operating
	VBLAST	L	L	Operating	L	Operating
	VPDR15 to VPDR0	L	L	Operating	L	Operating
	VPDV	L	L	Operating	L	Operating
	STPAK	L	H	Operating	L	Operating
External memory connection pins	A25 to A0	Undefined	Retained	Operating	L	Operating
	DO31 to DO0	Undefined	Undefined	Operating	L	Operating
	RDZ	H	H	Operating	H	Operating
	WRZ3 to WRZ0	H	H	Operating	H	Operating
	IORDZ	H	H	Operating	H	Operating
	IOWRZ	H	H	Operating	H	Operating
	HLDAKZ	H	H	Operating	L	Operating
	DC3 to DC0	H	H	Operating	H	Operating
	CSZ7 to CSZ0	H	H	Operating	H	Operating
	BENZ3 to BENZ0	H	H	Operating	H	Operating
	BCYSTZ	H	H	Operating	H	Operating
	REFRQZ	H	L	Operating	H[Note 1]	Operating
	SDCLK	Operating	Same as VBCLK	Operating	Operating	Operating
NT85E502 connection pins (n = 7 to 0)	CTCSOn4, CTCSOn3	H	Retained	Operating	Retained	Operating
	CTCSOn2	L	L	Operating	L	Operating
	CTCSOn1	L	Retained	Operating	Retained	Operating
	CTCSOn0	**Note 2**	Retained	Operating	Retained	Operating
	CTLO1	L	H	Operating	L	Operating
	CTLO0	L	L	Operating	L	Operating
	MTEN	L	L	L	L	H
	CT502On1, CT502On0	L	L	Operating	L	Operating
Test mode pins	PHTDO1, PHTDO0	L	L	L	L	Operating

Notes 1. If there is a refresh request from the NT85E502 during a bus hold, the pin status becomes a low-level output.

2. The status varies as follows depending on the input level of the MCE pin.
When a high level is input to the MCE pin: H
When a low level is input to the MCE pin: L

Remark L: Low-level output
H: High-level output
Retained: Retains the previous status

1.3 Bus Cycle Function

In the bus cycle function of the NT85E500, the operation settings are made using the operation mode setting pins and the following control registers, which are assigned to the peripheral I/O area of the NU85EA.

Table 1-5. List of Control Registers

Address	Register Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FFFFF480H	Bus cycle type configuration register 0	BCT0	R/W			√	8888H/ 0000H
FFFFF482H	Bus cycle type configuration register 1	BCT1	R/W			√	8888H/ 0000H
FFFFF484H	Data wait control register 0	DWC0	R/W			√	7777H
FFFFF486H	Data wait control register 1	DWC1	R/W			√	7777H
FFFFF488H	Bus cycle control register	BCC	R/W			√	FFFFH
FFFFF48AH	Address setting wait control register	ASC	R/W			√	FFFFH
FFFFF48CH	Bus cycle period control register	BCP	R/W	√	√		80H/ 00H
FFFFF49AH	Page ROM configuration register	PRC	R/W			√	7000H

Remark The settings of the NT85E500 control registers shown above are invalid for the ROM and RAM connected to the NU85EA's VFB (V850E fetch bus) and VDB (V850E data bus) respectively.

1.3.1 Bus cycle type configuration registers 0 and 1 (BCT0 and BCT1)

The NT85E500 can connect four types of external memory (when connecting SDRAM, the NT85E502 is necessary).

The BCT0 and BCT1 registers specify the controller and set whether operation is enabled for each CSn area (n = 7 to 0).

The BCT0 and BCT1 registers can be read or written in 16-bit units.

Figure 1-4. Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
BCT0	ME3	0	BT31	BT30	ME2	0	BT21	BT20	ME1	0	BT11	BT10	ME0	0	BT01	BT00	Address FFFFF480H	After reset **Note**
BCT1	ME7	0	BT71	BT70	ME6	0	BT61	BT60	ME5	0	BT51	BT50	ME4	0	BT41	BT40	Address FFFFF482H	After reset **Note**

Bit position	Bit name	Description
15, 11, 7, 3	MEn	Enable/disable operation of the MEMC for each CSn area. 0: Operation disabled (no response to the NU85EA) 1: Operation enabled
13, 12, 9, 8, 5, 4, 1, 0	BTn1, BTn0	Set the type of external memory to be connected for each CSn area.

BTn1	BTn0	External memory type
0	0	SRAM, I/O
0	1	Page ROM
1	0	Setting prohibited
1	1	SDRAM (when the NT85E502 is connected)

Note When a high level is input to the MCE pin: 8888H
When a low level is input to the MCE pin: 0000H

Caution Bits BTn1 and BTn0 of the BCT0 and BCT1 registers should be set immediately after reset, and their settings should not be subsequently changed (the MEn bit can be changed).

Remark n = 7 to 0

1.3.2 Address setting wait control register (ASC)

The NT85E500 can insert address setting wait states at the beginning of an SRAM or page ROM cycle. The number of address setting wait states to be inserted can be set for each CSn area by using the ASC register (n = 7 to 0).

The ASC register can be read or written in 16-bit units.

Remarks 1. The settings of this register are invalid during an SDRAM cycle.

2. The external wait function using the WAITZ input is invalid during an address setting wait period.

Figure 1-5. Address Setting Wait Control Register (ASC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ASC	AC7 1	AC7 0	AC6 1	AC6 0	AC5 1	AC5 0	AC4 1	AC4 0	AC3 1	AC3 0	AC2 1	AC2 0	AC1 1	AC1 0	AC0 1	AC0 0	Address FFFFF48AH	After reset FFFFH

Bit position	Bit name	Description
15 to 0	ACn1, ACn0	Set the number of address setting wait states to be inserted before an SRAM or page ROM cycle for each CSn area.

ACn1	ACn0	Number of wait states
0	0	None
0	1	1
1	0	2
1	1	3

Remark n = 7 to 0

1.3.3 Bus cycle control register (BCC)

The NT85E500 can insert idle states at the end of a read or write cycle of an SRAM or page ROM, and at the end of a read cycle of an SDRAM. The number of idle states to be inserted can be set for each CSn area by using the BCC register (n = 7 to 0).

These idle states are used to guarantee the interval until the external data bus is released by memory. The next bus cycle is started after the idle state(s).

The BCC register can be read or written in 16-bit units.

Figure 1-6. Bus Cycle Control Register (BCC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
BCC	BC7 1	BC7 0	BC6 1	BC6 0	BC5 1	BC5 0	BC4 1	BC4 0	BC3 1	BC3 0	BC2 1	BC2 0	BC1 1	BC1 0	BC0 1	BC0 0	Address FFFFF488H	After reset FFFFH

Bit position	Bit name	Description
15 to 0	BCn1, BCn0	Set the number of idle states to be inserted after a memory read or write cycle for each CSn area.

BCn1	BCn0	Number of idle states
0	0	None
0	1	1
1	0	2
1	1	3

Remark n = 7 to 0

1.3.4 Data wait control registers 0 and 1 (DWC0 and DWC1)

The NT85E500 can insert programmable data wait states for each CSn area (n = 7 to 0). The DWC0 and DWC1 registers control the data wait states when accessing SRAM, I/O, and page ROM (off-page cycle).

The DWC0 and DWC1 registers can be read or written in 16-bit units.

Figure 1-7. Data Wait Control Registers 0 and 1 (DWC0 and DWC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DWC0	0	DW32	DW31	DW30	0	DW22	DW21	DW20	0	DW12	DW11	DW10	0	DW02	DW01	DW00	Address FFFFF484H	After reset 7777H
DWC1	0	DW72	DW71	DW70	0	DW62	DW61	DW60	0	DW52	DW51	DW50	0	DW42	DW41	DW40	Address FFFFF486H	After reset 7777H

Bit position	Bit name	Description
14 to 12, 10 to 8, 6 to 4, 2 to 0	DWn2 to DWn0	Set the number of wait states when accessing SRAM, I/O or page ROM for each CSn area.

DWn2	DWn1	DWn0	Number of wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Remark n = 7 to 0

(1) External wait function

When the NT85E500 is connected to a low-speed device or I/O, or to an asynchronous system, wait states can be inserted in the bus cycle by using the external wait input pin (WAITZ).

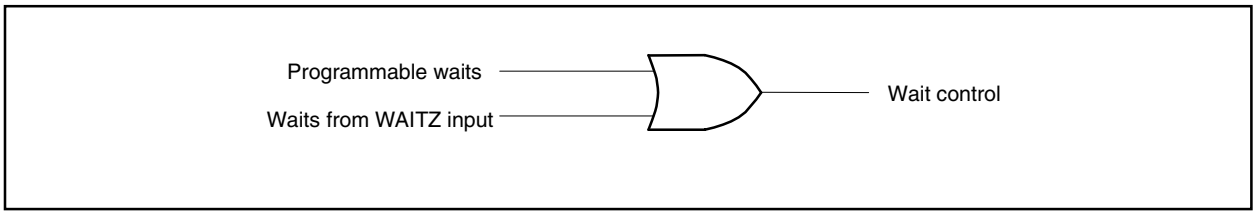
External wait states are inserted only for the data wait cycle.

External waits are sampled at the rising edge of the VBCLK signal.

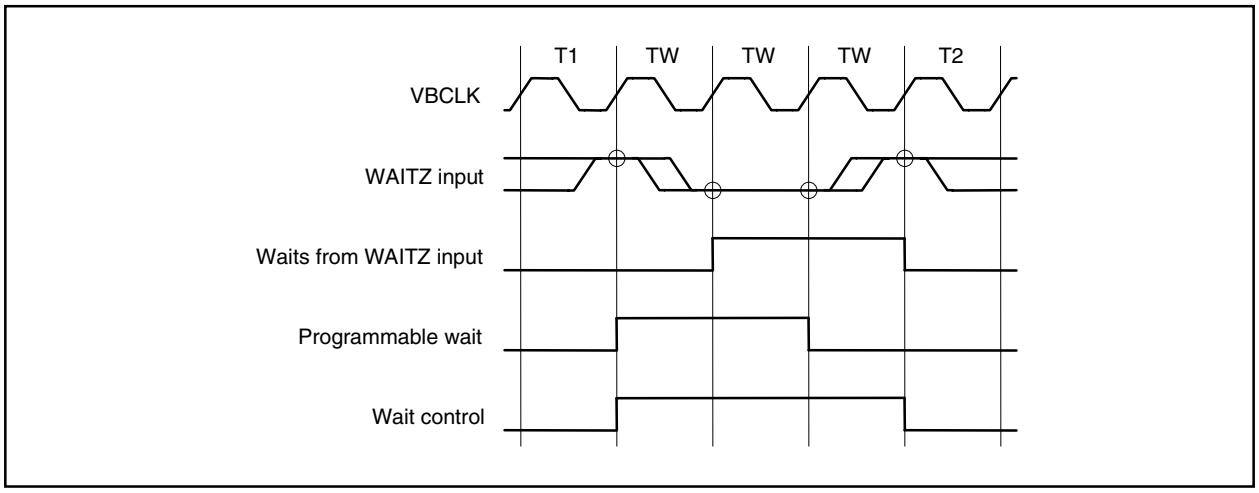
The WAITZ input is sampled at the rising edge of the VBCLK signal between the T1 cycle (or TW cycle) and the next cycle, and waits are only inserted in the data wait cycle.

(2) Data wait control registers and external waits

The logical sum (OR) of the number of waits set by data wait control registers 0 and 1 (DWC0 and DWC1) and the number of external waits from the WAITZ input is inserted for the wait cycle. Therefore, the number of wait cycles that are inserted is equal to the larger of these two numbers of waits.



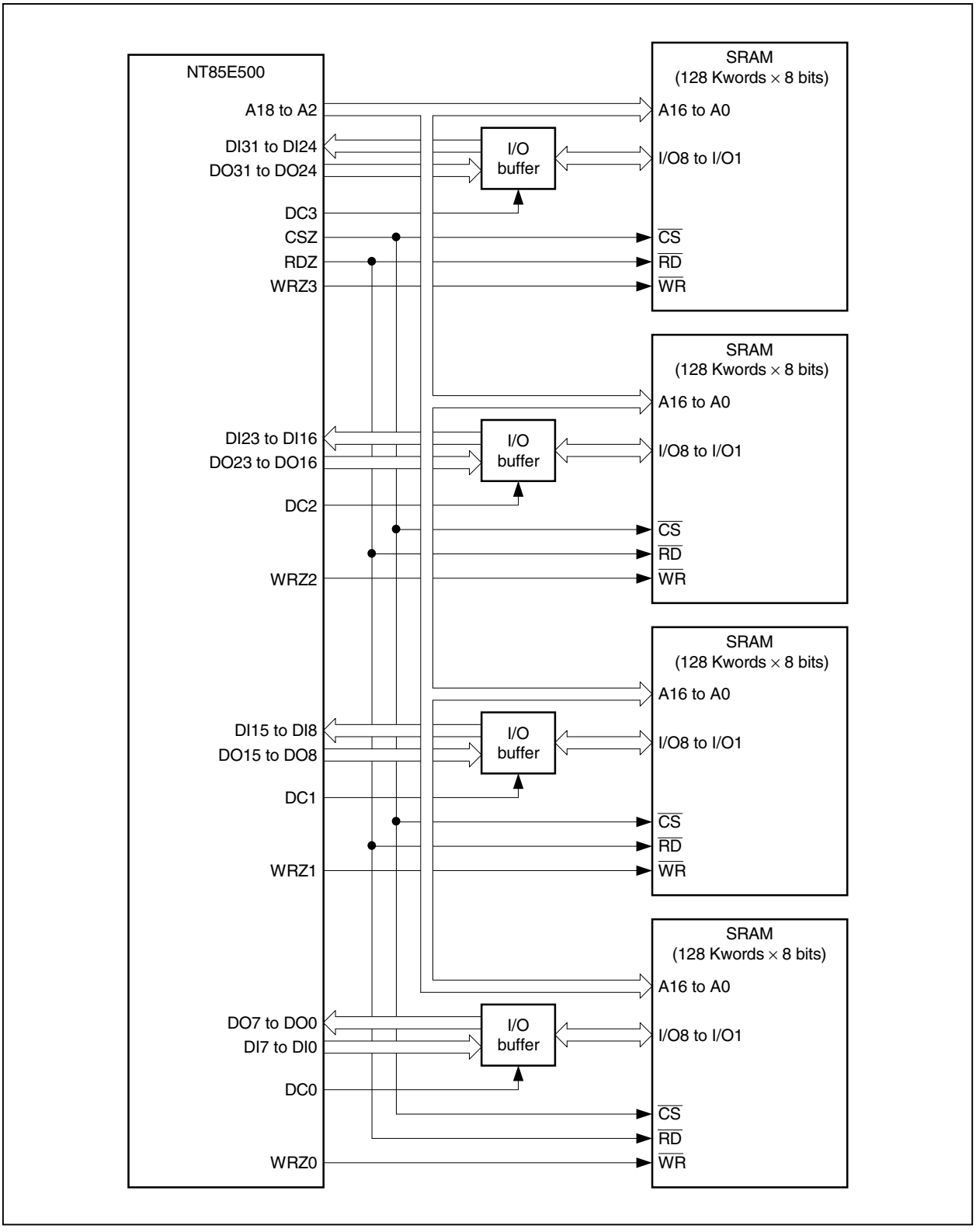
For example, when the programmable wait and the WAITZ input have the following timings, the bus cycle contains 3 waits.



1.3.5 SRAM cycle

(1) Connection example

Figure 1-8. SRAM Connection Example



(2) Bus timing

Examples of the bus timing for an SRAM read or write are shown below. An SRAM bus cycle consists of the following states.

- T1 and T2 states: Basic states for access by the NT85E500.
- T3 state: Basic state that is added during a flyby transfer.
- TA state: Address setting wait state that is inserted according to the ASC register settings.
- TI state: Idle state that is inserted according to the BCC register settings.
- TW1 state: Wait state that is inserted according to the DWC0 and DWC1 register settings.
- TW2 state: Wait state caused by WAITZ input.

Remarks 1. Circles indicate sampling timing.

2. XXX : Unknown state (output) or any level (input).

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 1-9. SRAM Read Timing

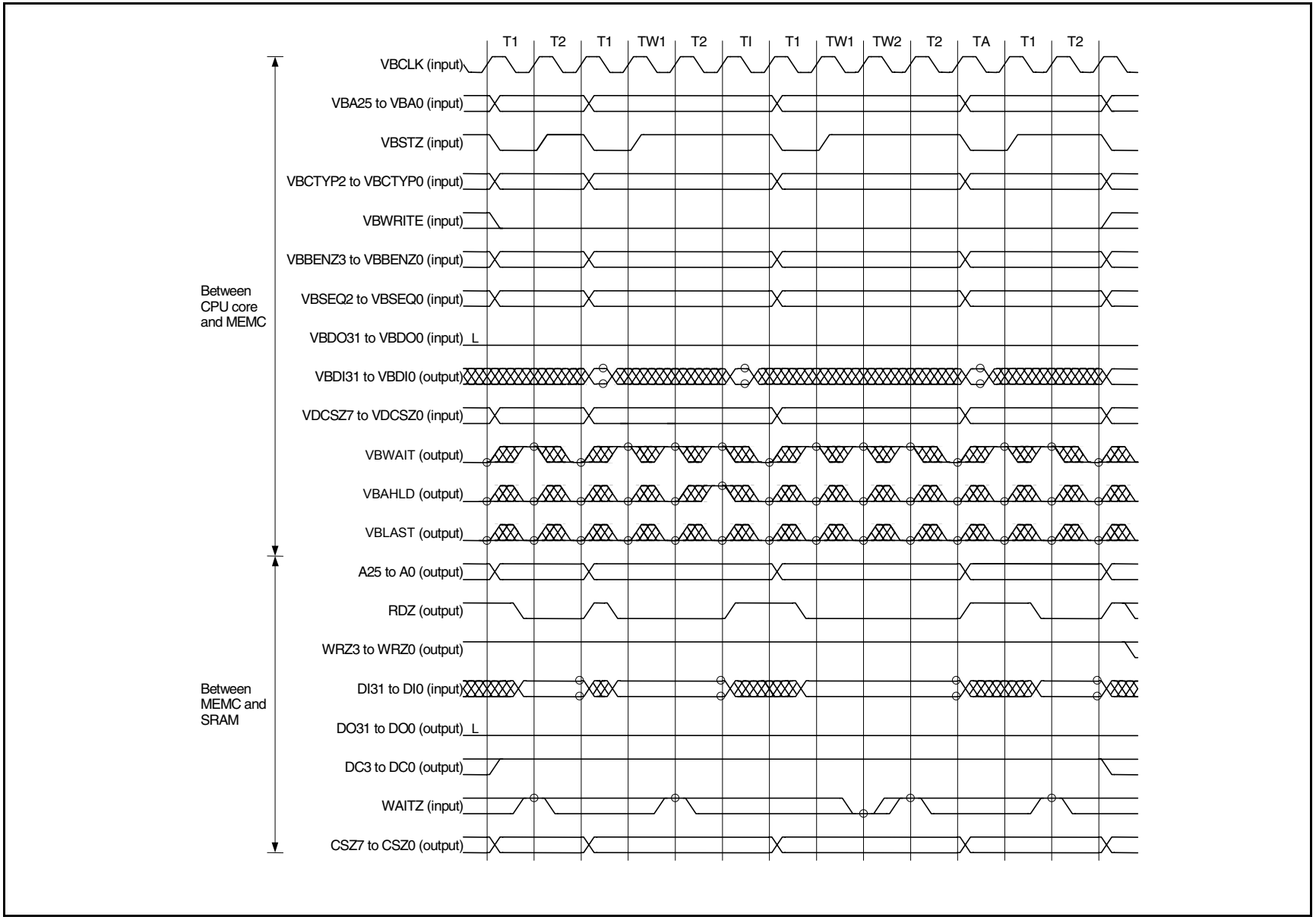


Figure 1-10. SRAM Write Timing

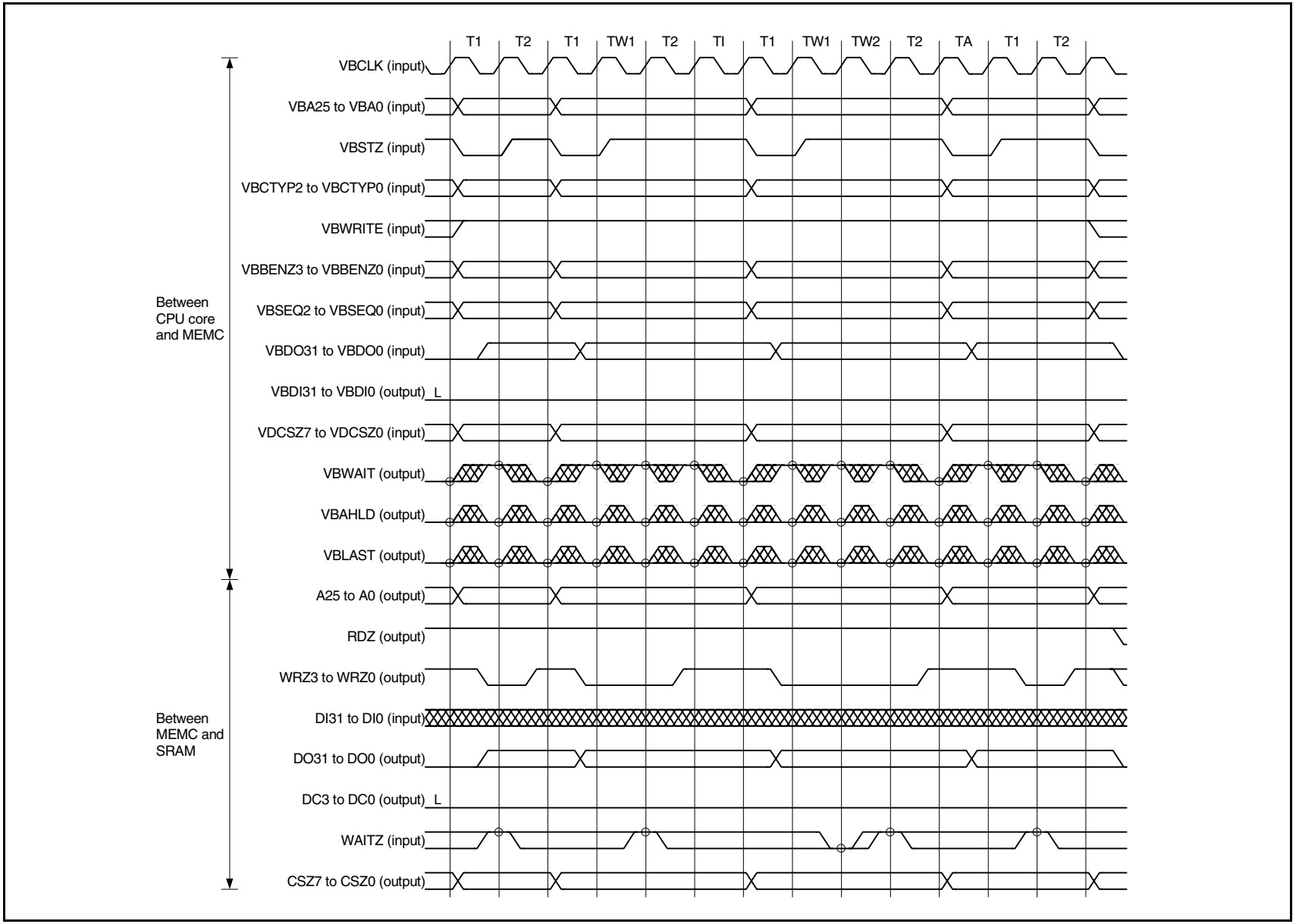
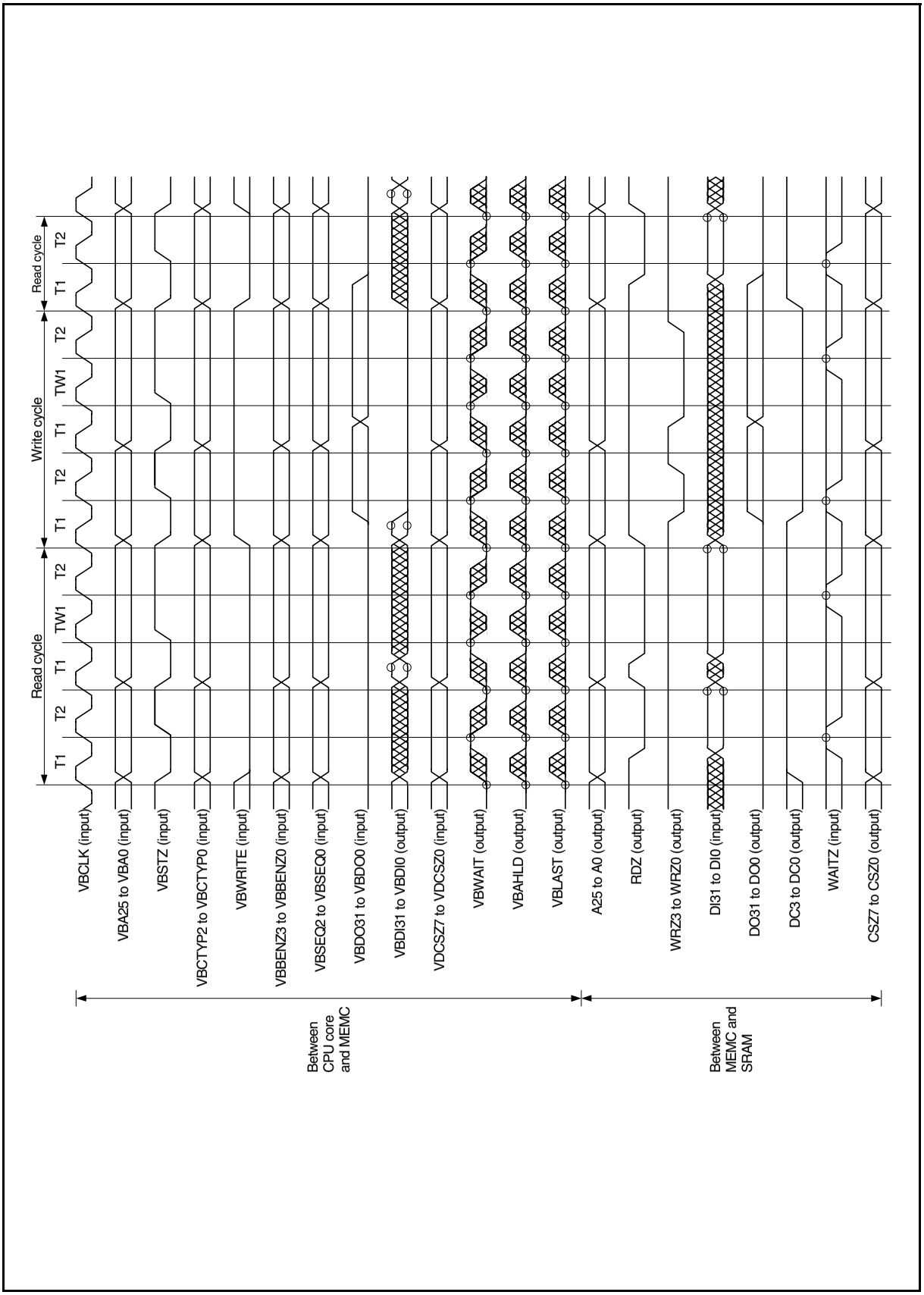


Figure 1-11. SRAM Read/Write Timing



Examples of DMA flyby cycle timing are shown below.

A DMA flyby cycle transfers data between external memory and I/O on a request from the DMA controller.

Figure 1-12. SRAM Flyby Cycle Timing (SRAM → I/O)

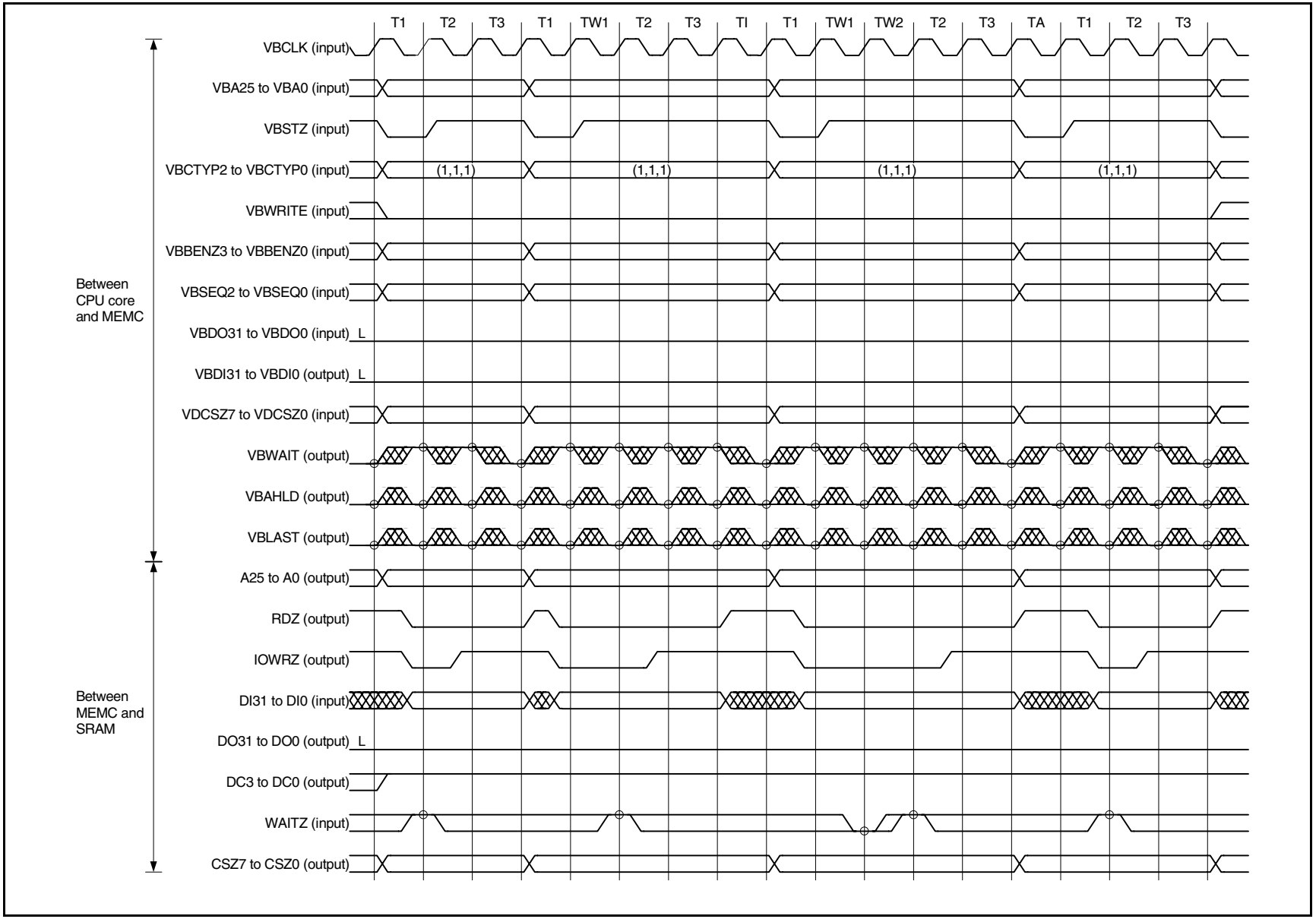
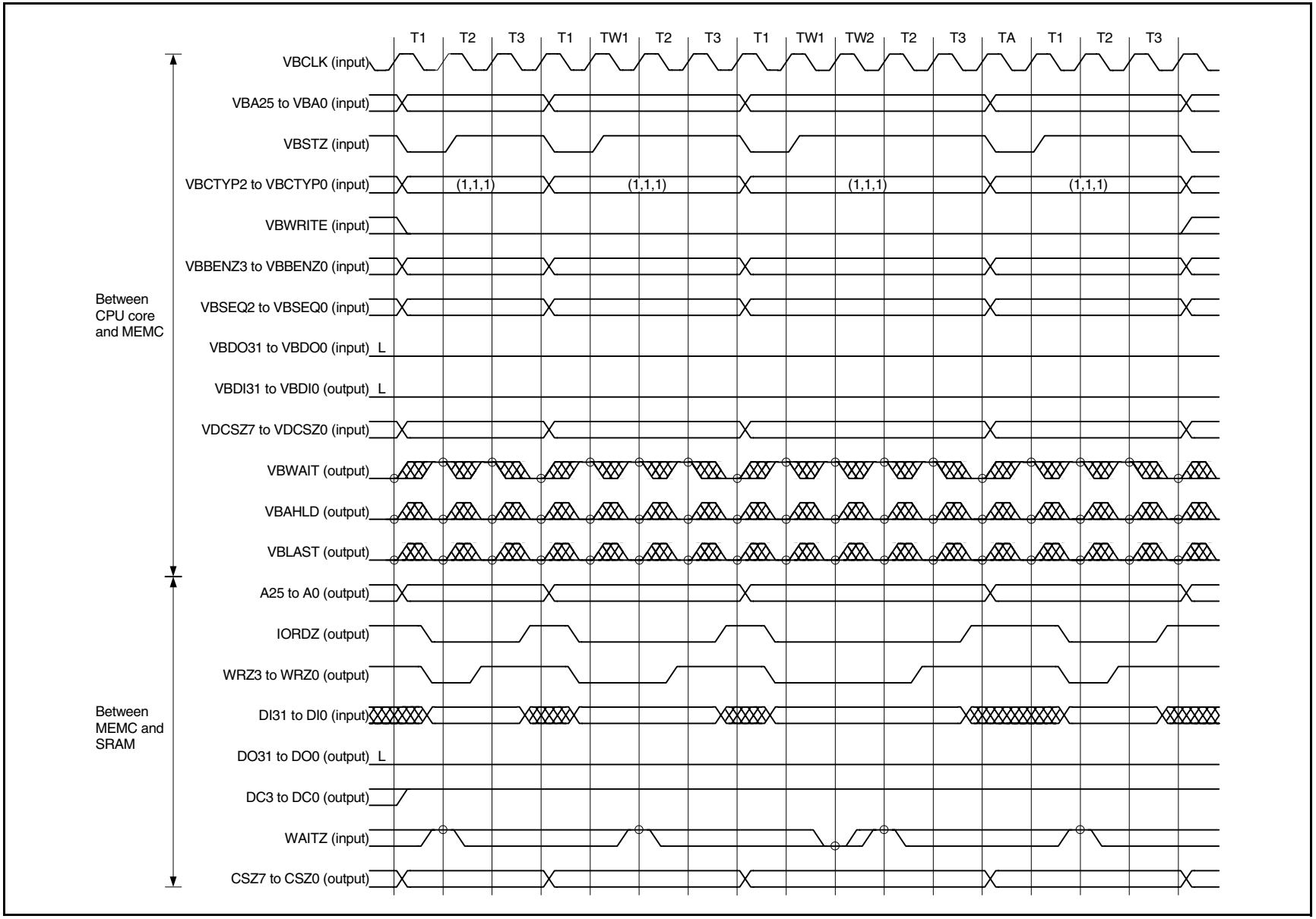


Figure 1-13. SRAM Flyby Cycle Timing (I/O → SRAM)



1.3.6 Page ROM configuration register (PRC)

When a page ROM bus cycle occurs, the NT85E500 judges whether or not it is an on-page access by comparing the address immediately after the page ROM cycle that occurred with the current address.

The address comparison width and the number of wait states during an on-page cycle are set using this register.

This register can be read or written in 16-bit units.

Caution The number of wait states during an off-page cycle is set using the DWC0 and DWC1 registers.

Figure 1-14. Page ROM Configuration Register (PRC) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
PRC	0	PRW2	PRW1	PRW0	0	0	0	0	0	0	0	0	MA6	MA5	MA4	MA3	Address FFFFF49AH	After reset 7000H

Bit position	Bit name	Description
14 to 12	PRW2 to PRW0	Set the number of data wait states during a page ROM on-page read cycle.

PRW2	PRW1	PRW0	Number of data wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Caution The value set in the DWC0 and DWC1 registers is used for the number of wait states during the first page ROM read (off-page read). If this is followed by consecutive on-page address reading, the wait state number set by the PRW2 to PRW0 bits is used. It is therefore necessary to set a wait state number in the DWC0 and DWC1 registers that satisfies the off-page read access time of the connected page ROM and a wait state number in the PRW2 to PRW0 bits that satisfies the on-page read access time.

Figure 1-14. Page ROM Configuration Register (PRC) (2/2)

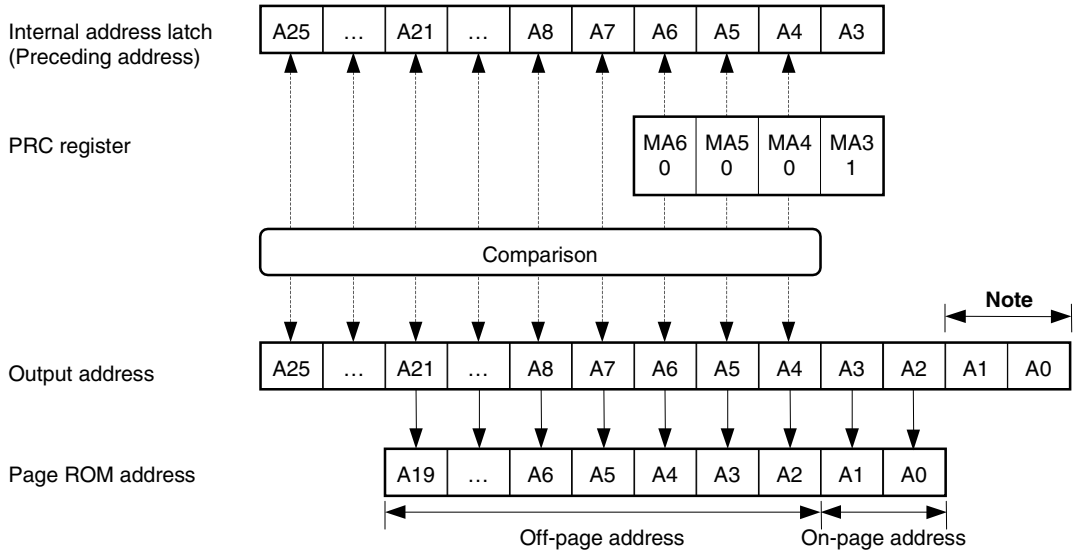
Bit position	Bit name	Description
3 to 0	MA6 to MA3	Set the mask bits for comparing addresses.

MA6	MA5	MA4	MA3	Number of consecutive reads
0	0	0	0	32 bits × 2, 16 bits × 4, 8 bits × 8
0	0	0	1	32 bits × 4, 16 bits × 8, 8 bits × 16
0	0	1	1	32 bits × 8, 16 bits × 16, 8 bits × 32
0	1	1	1	32 bits × 16, 16 bits × 32, 8 bits × 64
1	1	1	1	32 bits × 32, 16 bits × 64, 8 bits × 128

Caution The MA6 to MA3 bits do not set the desired number of continuous accesses; use them to set the number of times consecutive reading can be executed during on-page access of the connected page ROM.

An example of address mask control when four 1-Mword × 8-bit page ROMs are connected is shown below.

Figure 1-15. Example of Control Using Bits MA6 to MA3



Note Not used for a 32-bit data bus.

1.3.7 Page ROM cycle

(1) Connection example

Figure 1-16. Page ROM Connection Example (for 16-Bit Data Bus)

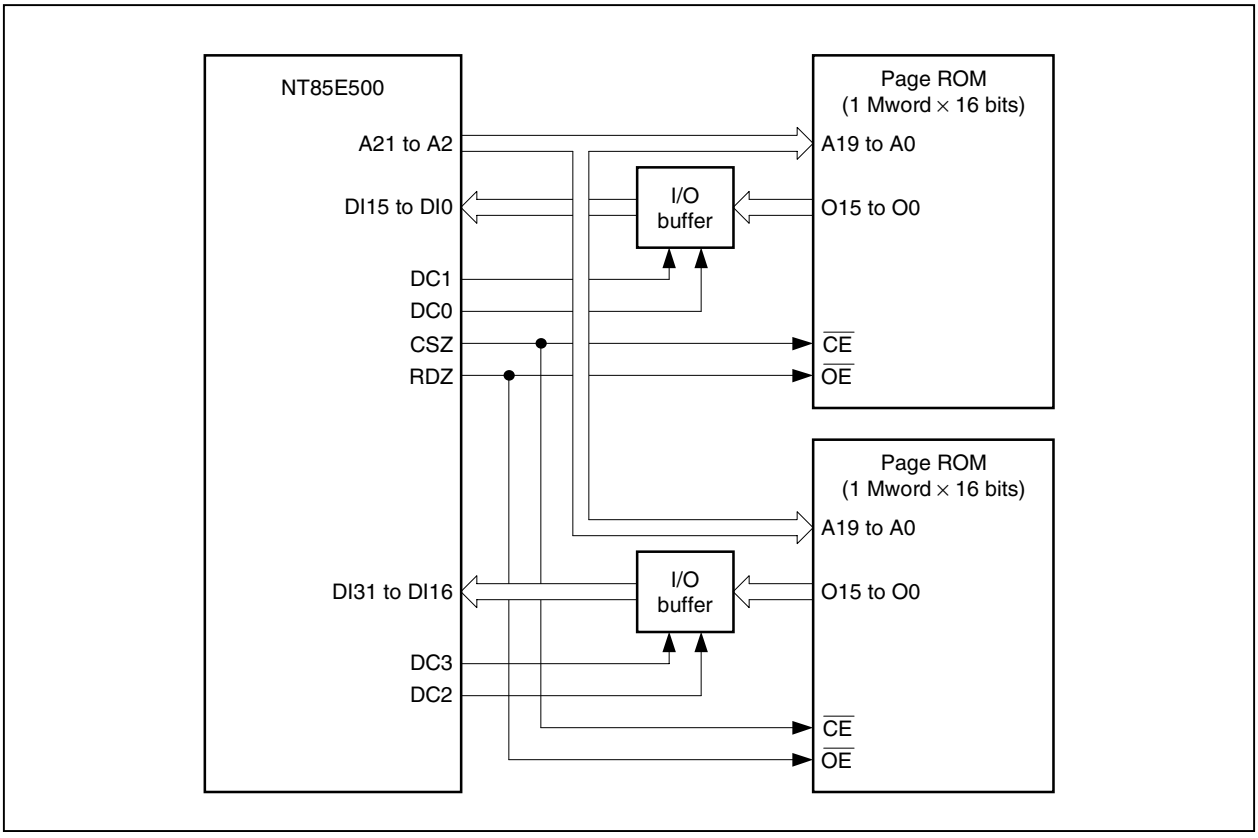
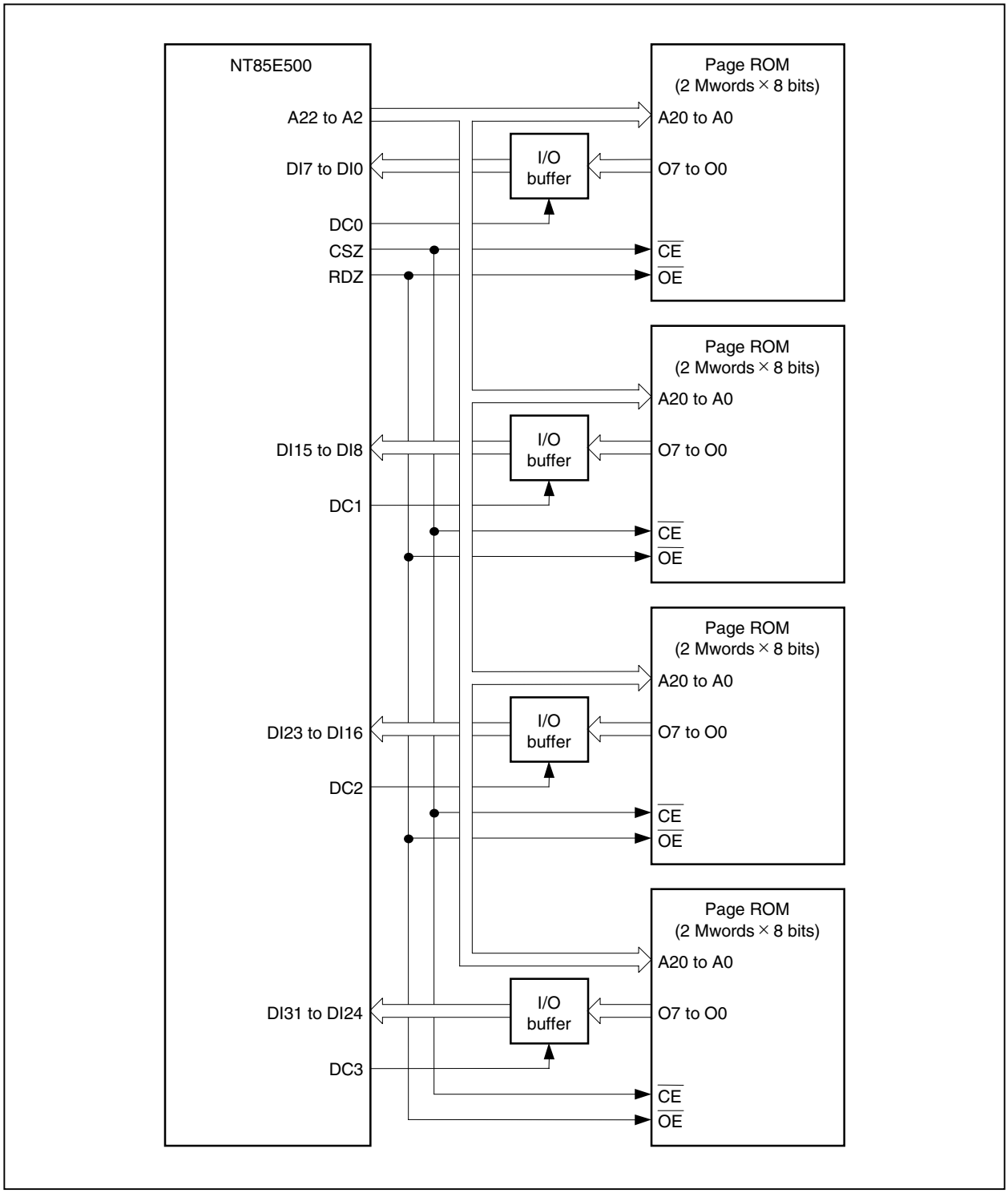


Figure 1-17. Page ROM Connection Example (for 8-Bit Data Bus)



(2) Bus timing

Examples of the bus timing for a page ROM read are shown below. A page ROM bus cycle consists of the following states.

- T1 and T2 states: Basic states for access by the NT85E500.
- T3 state: Basic state that is added during a flyby transfer.
- TA state: Address setting wait state that is inserted according to the ASC register settings. This state is inserted regardless of on-page/off-page.
- TI state: Idle state that is inserted according to the BCC register settings. This state is inserted regardless of on-page/off-page.
- TO1 and TO2 states: Sequential transfer basic states at the time of a page ROM read.
- TW1 state: Wait state that is inserted according to the DWC0 and DWC1 register settings.
- TW2 state: Wait state caused by the WAITZ input.
- TW3 state: Data wait state inserted according to the PRC register settings during a page ROM on-page read cycle.

Remarks 1. Circles indicate sampling timing.

2. XXX: Unknown state (output) or any level (input).

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 1-18. Page ROM Read Timing (1/2)

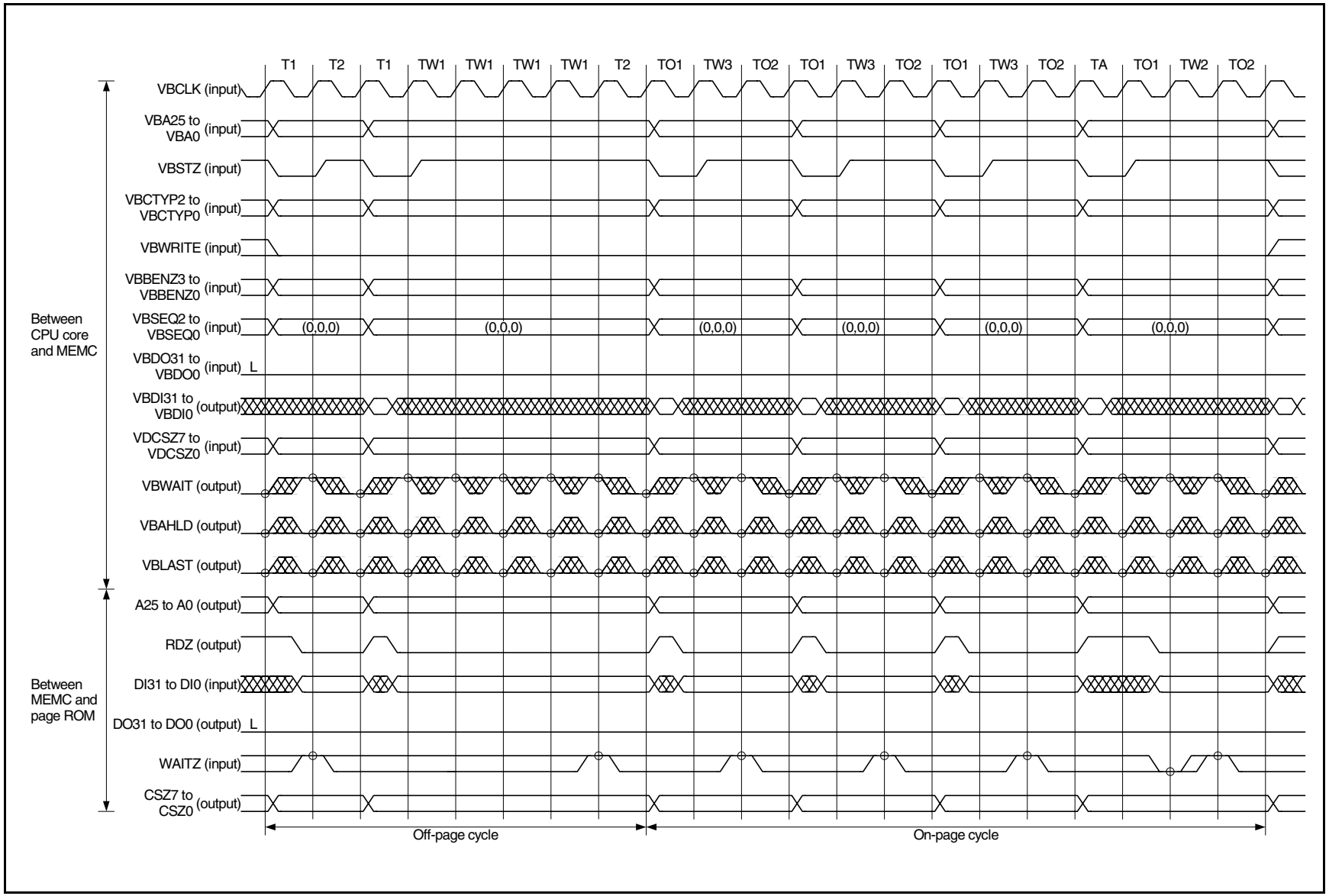
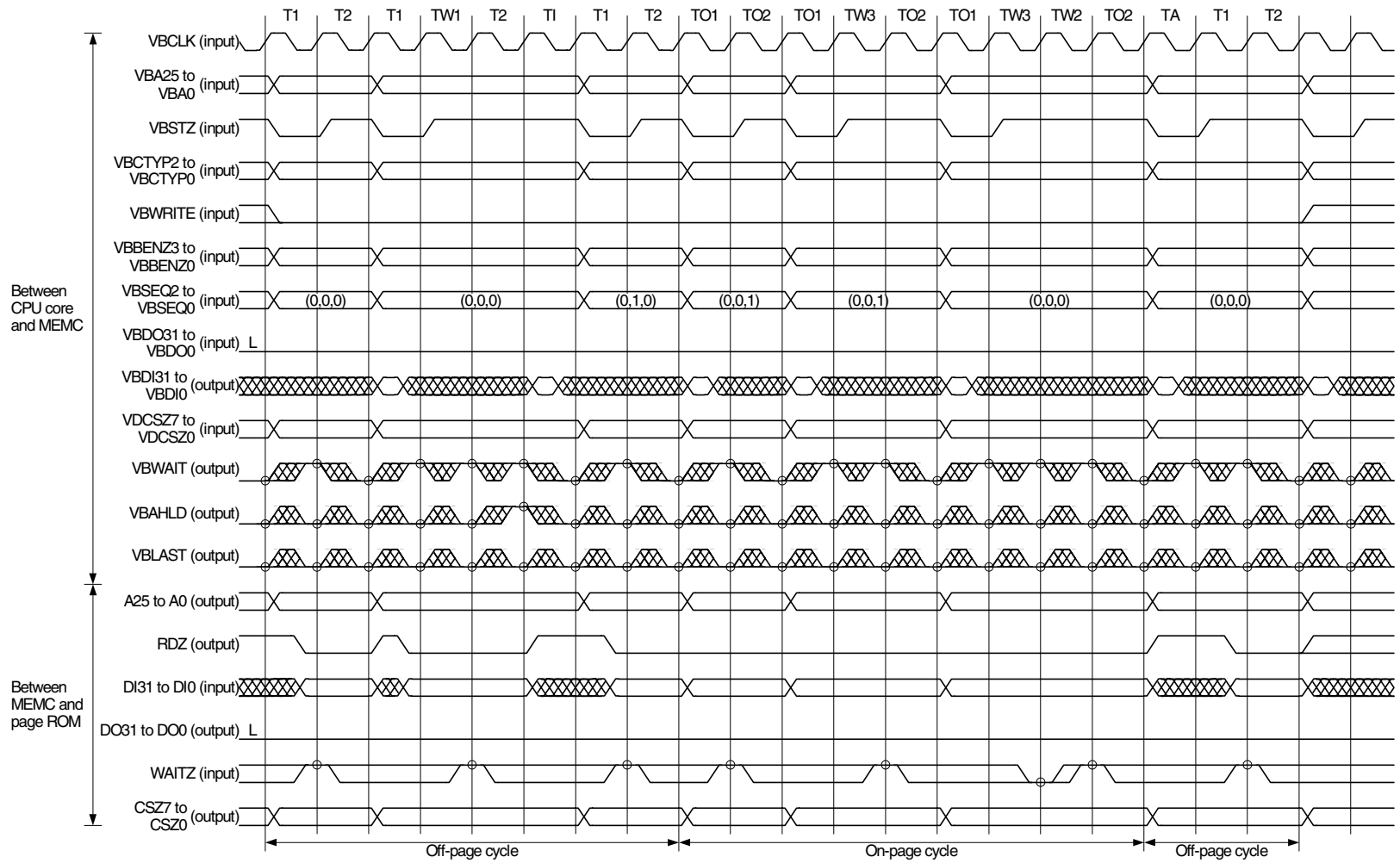
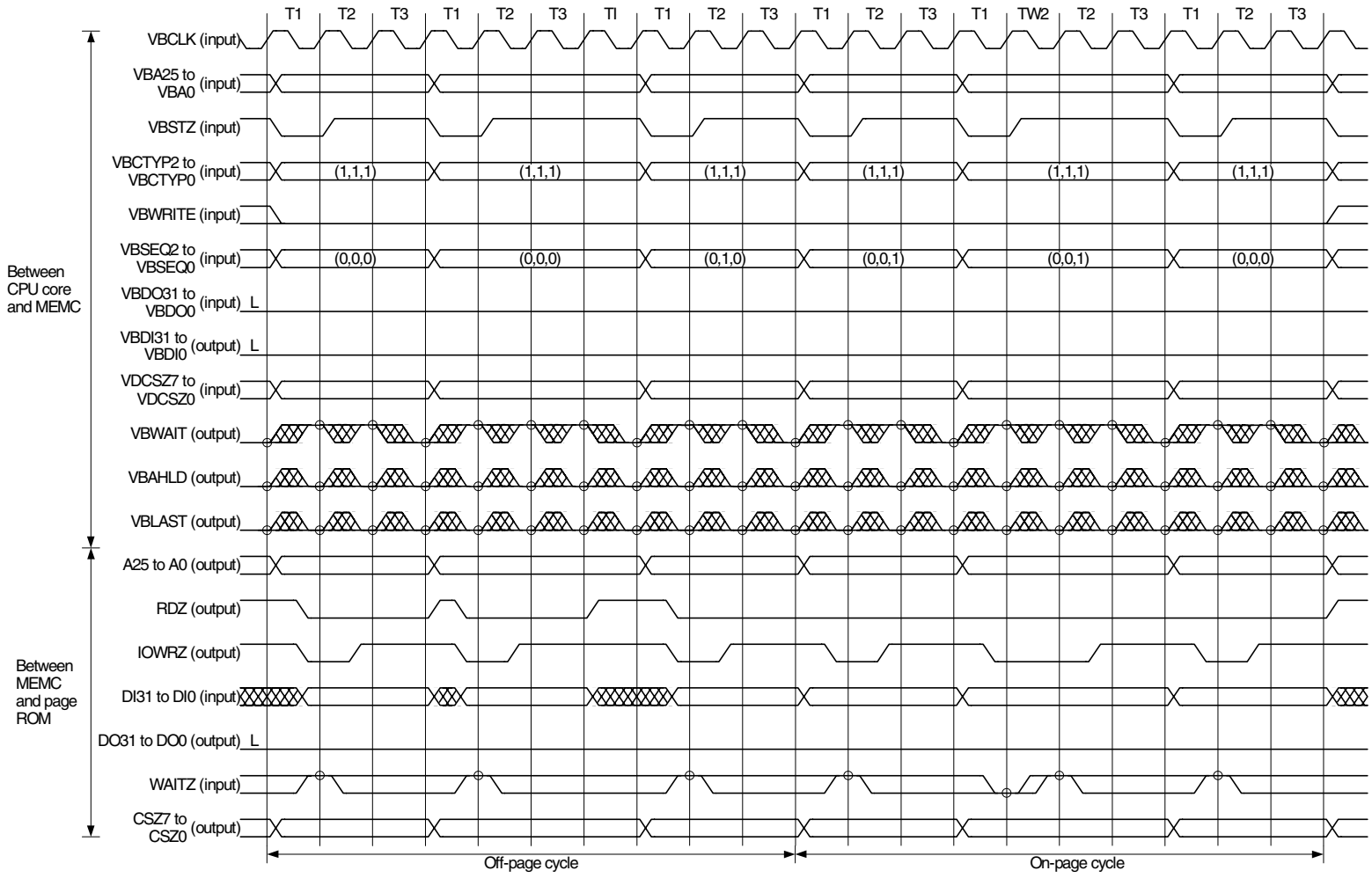


Figure 1-18. Page ROM Read Timing (2/2)



Remark This figure indicates the timing when the RDZ signal is held active (low level) during an on-page cycle (only when the VBSEQ2 to VBSEQ0 signals indicate consecutive transfer).

Figure 1-19. Page ROM Flyby Cycle Timing (Page ROM → I/O)



Remark This figure indicates the timing when the RDZ signal is held active (low level) during an on-page cycle (only when the VBSEQ2 to VBSEQ0 signals indicate consecutive transfer and the number of wait states is set to 0 by the ASC and BCC registers).

★ **(3) Restriction related to page ROM access**

When multiple page ROMs are connected to multiple different CSn areas in the system, the following restriction related to page ROM access applies (n = 0 to 7).

Caution Page ROM has a page access function and includes memory that enables high-speed consecutive access on the page.

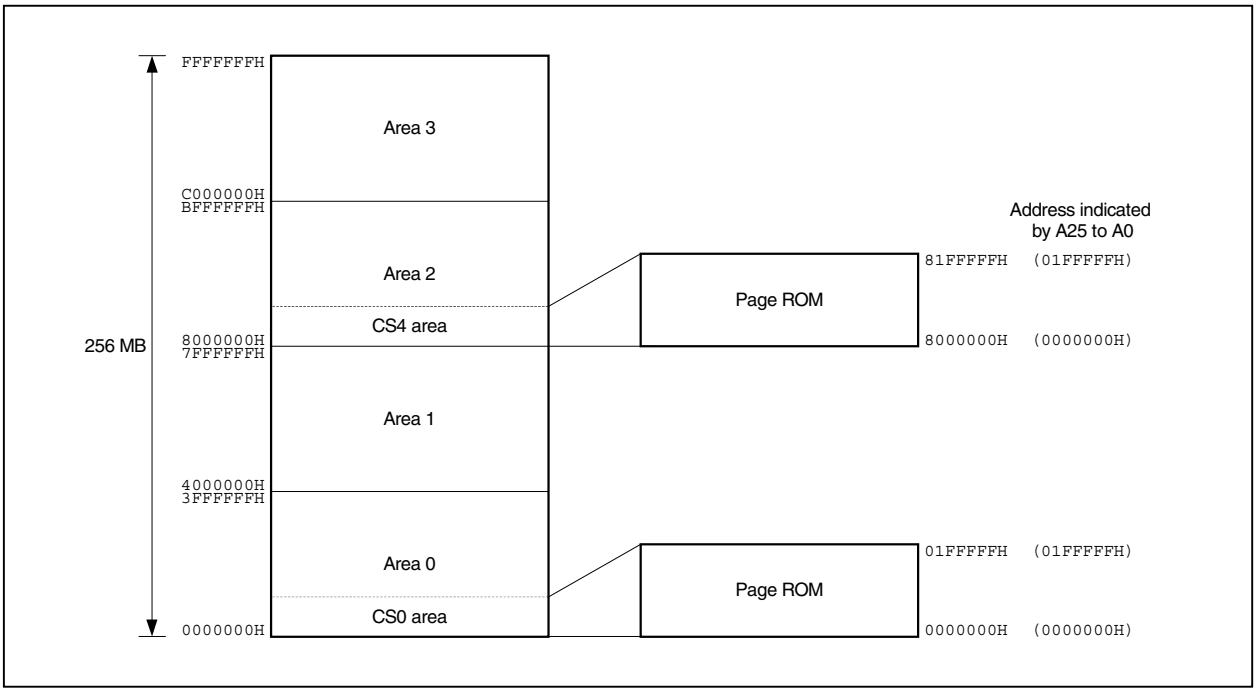
(a) Restriction

If the page ROM of another CSn area is accessed consecutively immediately after a page ROM is accessed, when the address at which the page ROM was accessed earlier and the address at which the page ROM was accessed immediately after are on the same page of the page ROM, an on-page cycle is also generated for the page ROM accessed immediately after because it is mistakenly assumed that the same page ROM is accessed, even though a different CSn area is accessed (n = 0 to 7).

As a result, the data access time for the page ROM accessed immediately after is insufficient, and the read operation cannot be performed correctly.

For example, in the case of the memory map configuration example shown in Figure 1-20, an on-page cycle is generated for 8000002H if 8000002H of the CS4 area is accessed immediately after 0000000H of the CS0 area is accessed.

Figure 1-20. Memory Map Configuration Example (When Restriction Applies)



If any of the following conditions applies, the restriction operation does not occur.

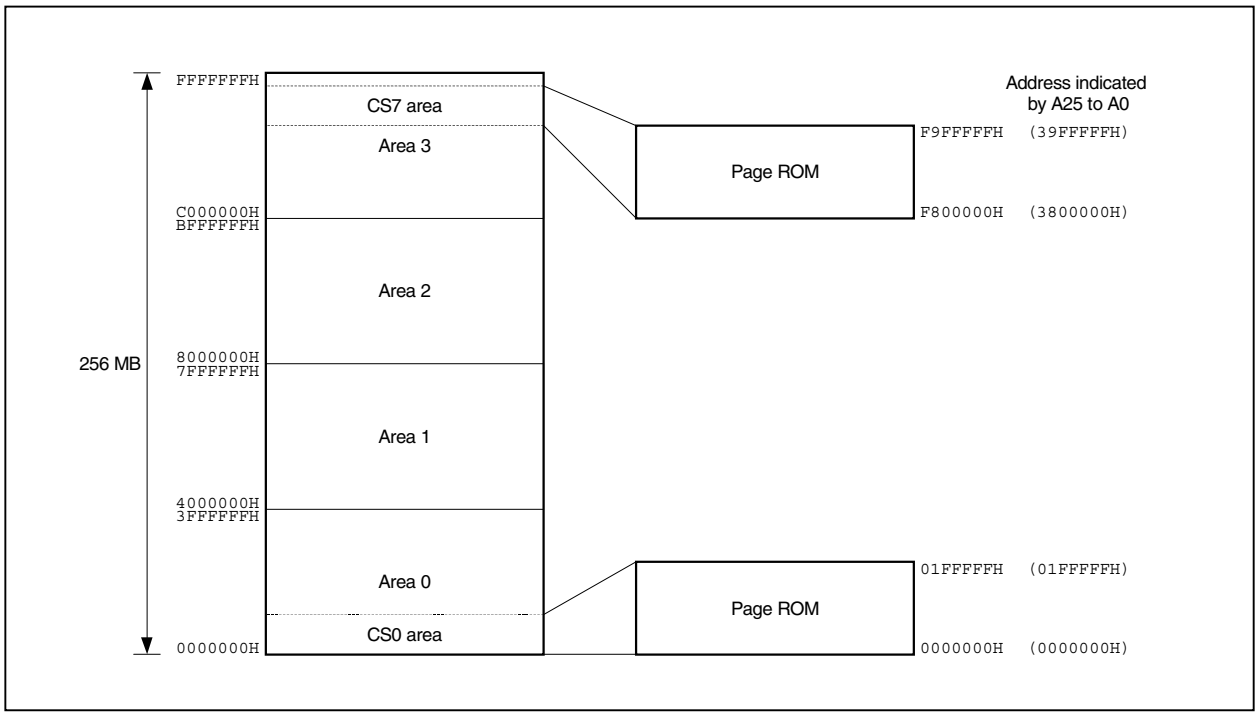
- When ROM with page mode is not used
- When only one ROM with page mode is used
- When ROM with page mode is used only for program area
- When data area is used in 64 MB mode
- When ROM with multiple page modes is used in CS0, CS1, and CS2 areas only
- When ROM with multiple page modes is used in CS5, CS6, and CS7 areas only
- When the address indicated by A25 to A0 does not overlap in ROM with multiple page modes

(b) Countermeasure

When using multiple page ROMs, allocate each page ROM so that the address indicated by A25 to A0 does not overlap.

For example, when allocating two 2 MB page ROMs to different CSn areas, allocate one page ROM to 0000000H to 01FFFFFH, and allocate the other page ROM to F800000H to F9FFFFFH, to configure the memory map shown in Figure 1-21 (n = 0 to 7).

Figure 1-21. Memory Map Configuration Example (When Restriction Does Not Apply)



1.3.8 Bus hold function

When the HLDRQZ signal becomes active, the NT85E500 shifts to the bus hold status. When the transition into the bus hold status is completed, the HLDAKZ signal becomes active. The HLDAKZ signal retains an active level during a bus hold.

During a bus hold, the bus master of the VSB becomes the NT85E500. Design the external memory connection pins on the user logic side so that signals do not conflict during a bus hold. For details of pin statuses during a bus hold, refer to **Table 1-4 Pin Status in Each Operating Mode**.

When the HLDRQZ signal becomes inactive, the NT85E500 shifts to the normal status.

(1) Bus hold procedure

<1> An external bus hold request signal (HLDRQZ) is input for the NT85E500 from an external bus master.
<2> The NT85E500 outputs a VSB mastership request signal (VAREQ) for the NU85EA.
<3> The current bus cycle ends.
<4> An acknowledge signal for the VAREQ signal (VAACK) is input to the NT85E500 from the NU85EA.
<5> The NT85E500 returns an acknowledge signal for the HLDRQZ signal (HLDAKZ) to external memory.

(2) Bus hold release procedure

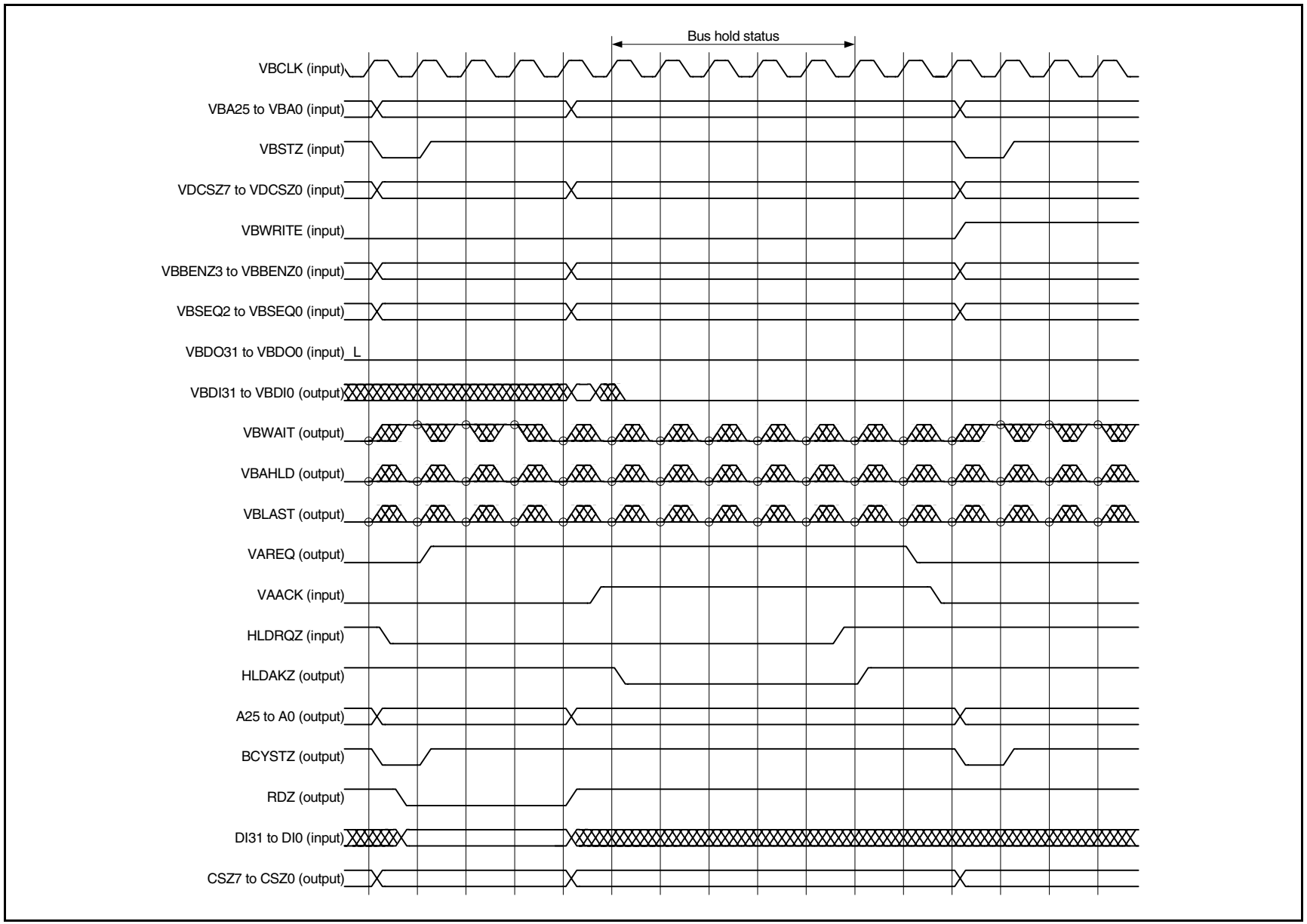
<1> The HLDRQZ signal becomes inactive.
<2> The bus hold request is released externally and the HLDAKZ signal becomes inactive.
<3> After the refresh cycle ends if a refresh request has been generated, or immediately if there is no refresh request, the VAREQ signal to the NU85EA becomes inactive.
<4> The VAACK signal from the NU85EA becomes inactive and the bus hold status ends.
<5> The NU85EA becomes the master and a VSB bus cycle begins.

(3) Bus hold timing

An example of bus hold timing is shown below.

Remarks 1. Circles indicate sampling timing.
2. ⌧: Unknown state (output) or any level (input).
3. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 1-22. Bus Hold Timing



1.3.9 Bus cycle period control register (BCP)

The NT85E500 can double the bus cycle period when accessing SRAM or page ROM. Control of the bus cycle period is performed using the BCP register.

When the BCP bit of the BCP register is set (to 1), a dummy state (TD) is inserted before each state of the bus cycle.

The BCP register can be read or written in 8-bit or 1-bit units.

Caution This register's settings are only valid when accessing SRAM or page ROM (invalid when accessing SDRAM).

Figure 1-23. Bus Cycle Period Control Register (BCP)

	7	6	5	4	3	2	1	0	Address	After reset
BCP	BCP	0	0	0	0	0	0	0	FFFFF48CH	**Note**

Bit position	Bit name	Description
7	BCP	Sets the length of the bus cycle period. 0: Normal 1: Double

Note On high-level input to BCPEN pin: 80H
On low-level input to BCPEN pin: 00H

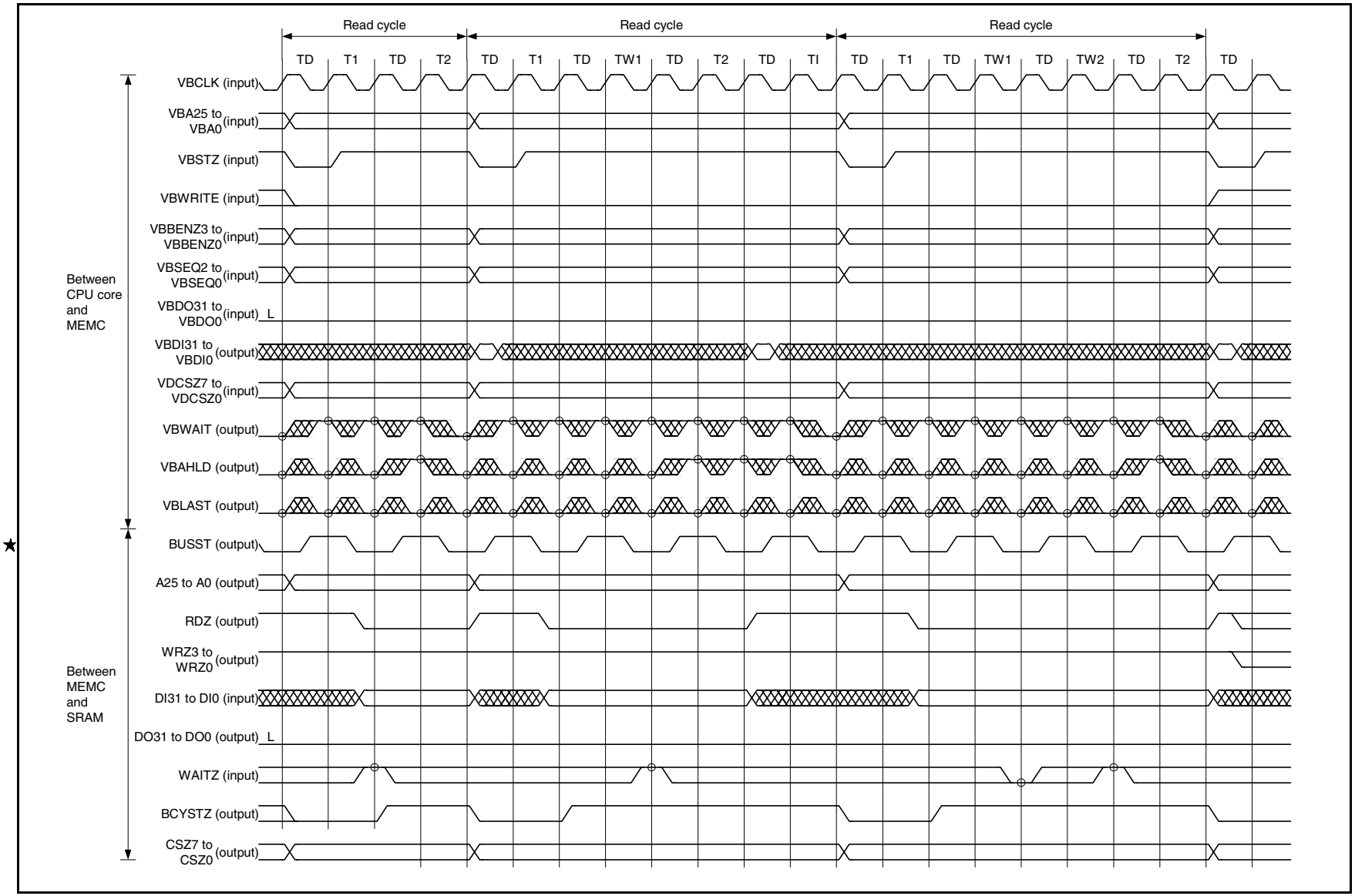
An example of the timing when the bus cycle period is doubled is shown below.

Remarks 1. Circles indicate sampling timing.

2. XXX: Unknown state (output) or any level (input).

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 1-24. SRAM Read Timing (Bus Cycle Period Doubled)



1.3.10 STOP function

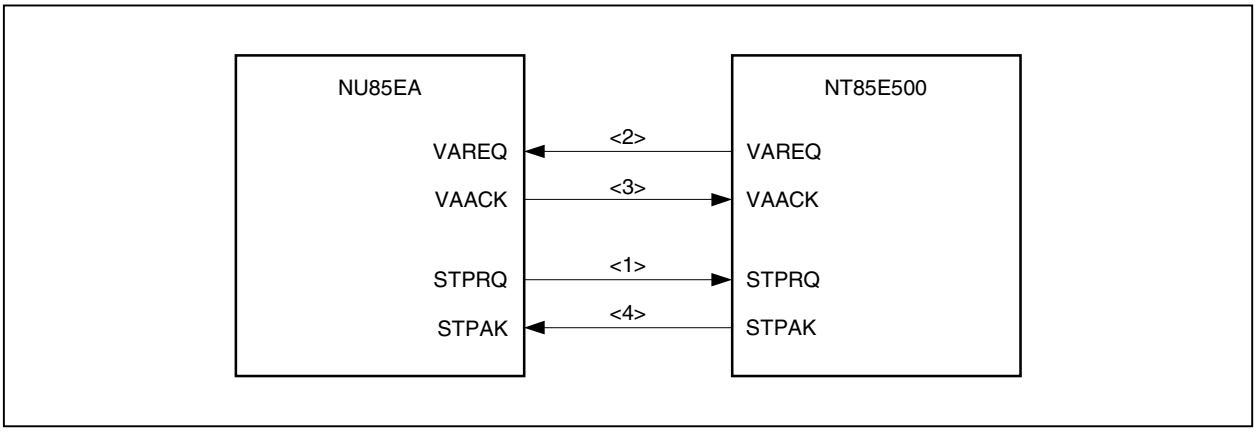
When the NU85EA undergoes a transition to STOP mode, the NT85E500 operates according to the following sequence (see **Figure 1-25**).

<1> When a hardware STOP or software STOP is executed, a STOP mode request signal (STPRQ) is input from the NU85EA to the NT85E500.
<2> The NT85E500 outputs a VSB mastership request signal (VAREQ) for the NU85EA.
<3> An acknowledge signal for the VAREQ signal (VAACK) is input from the NU85EA to the NT85E500.
<4> The NT85E500 returns an acknowledge signal for the STPRQ signal (STPAK) to the NU85EA.

The NT85E500 returns the STPAK signal no less than two clocks after receiving the STPRQ signal.

Moreover, if an NT85E502 is connected to the NT85E500, the STPAK signal becomes active after the SDRAM self-refresh cycle is executed.

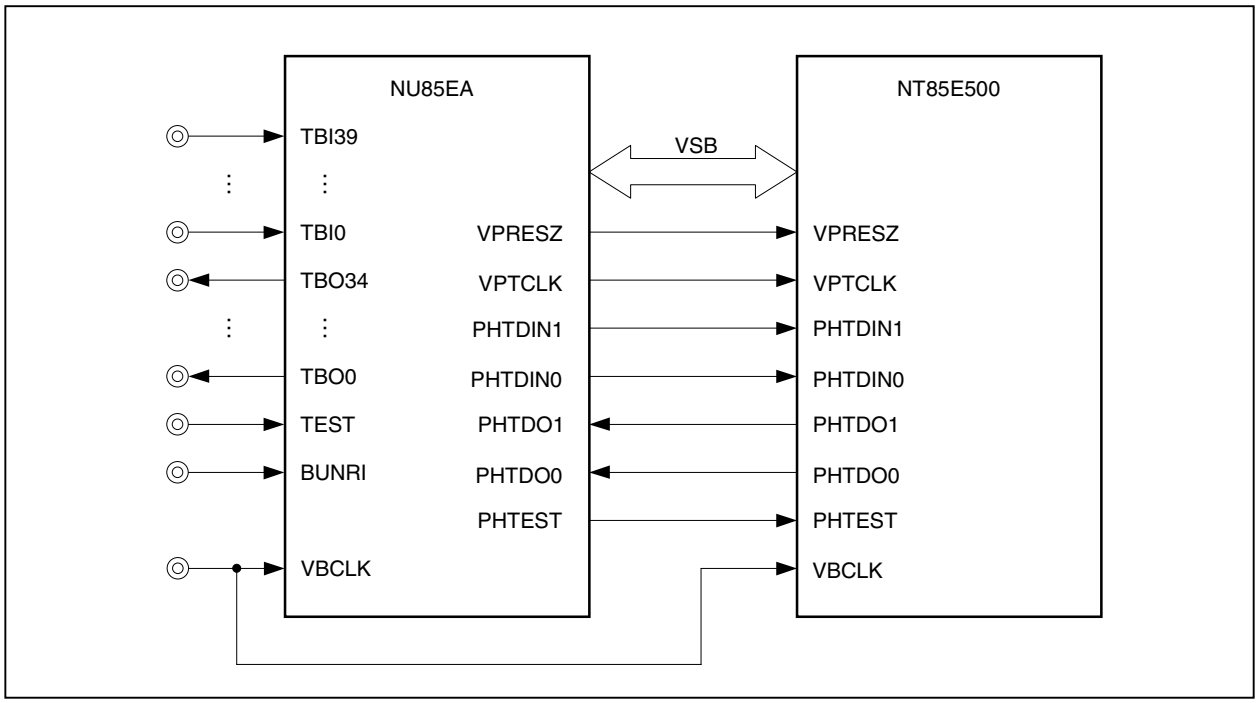
Figure 1-25. NT85E500 Operation at Time of STOP Mode Transition



1.4 Test Function

The NT85E500 can be tested using the NU85EA test mode.
To test the NT85E500, connect it to the NU85EA as follows.

Figure 1-26. Connection of NT85E500 to NU85EA in Test Mode



★ Process each pin in the test mode as follows.

(1) Test mode pins

Connect test mode pins to the NU85EA as shown in Figure 1-26.

(2) Other pins

Make other pins the same as in normal mode (If they are unused, process them according to **1.2.3 Recommended connection of unused pins**). Refer to **1.2.4 Pin status** regarding the pin status.
The DI31 to DI0, HLDRQZ, WAITZ, and SELFREF signals are ignored regardless of the values that are input.

Remark For details about test modes, refer to the **NU85E Hardware User's Manual (A14874E)**.

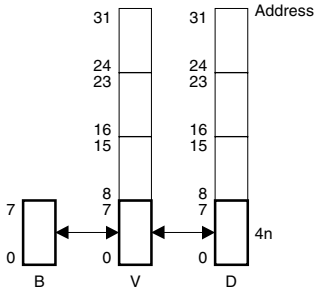
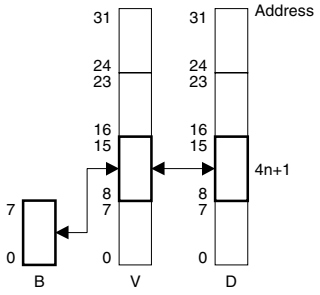
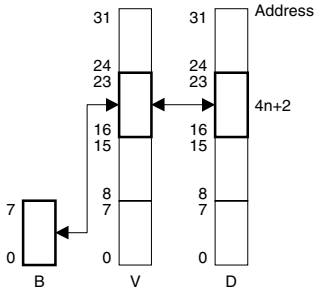
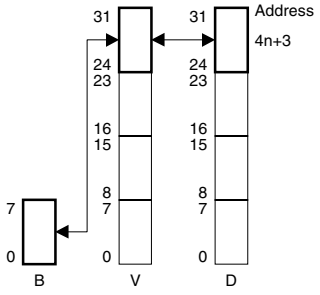
1.5 Data Flow

The flow of data transfer to external memory differs according to the register settings, starting addresses, and data width.

Data flows are shown below for each condition.

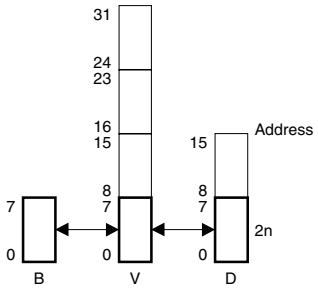
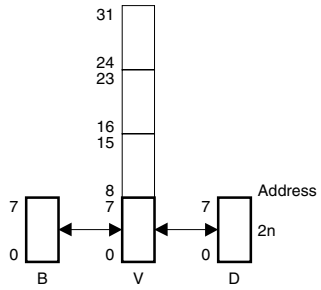
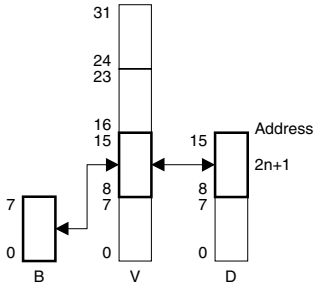
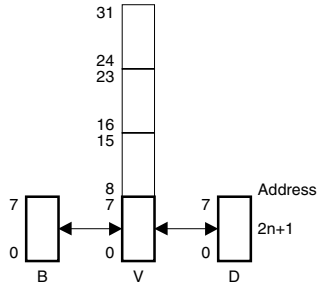
1.5.1 Data flow for byte access (8 bits)

Figure 1-27. Byte Access (Little Endian) (1/2)

Address To Be Accessed	Data Transfer Flow
	External Data Bus: 32 Bits
4n	
4n + 1	
4n + 2	
4n + 3	

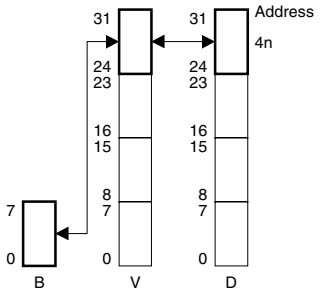
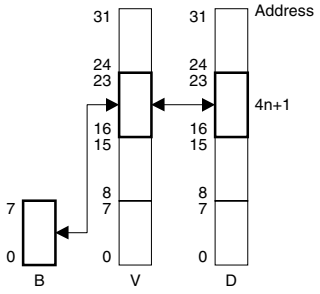
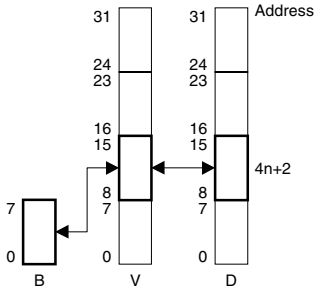
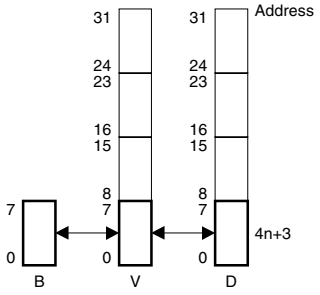
Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-27. Byte Access (Little Endian) (2/2)

Address To Be Accessed	Data Transfer Flow	
	External Data Bus: 16 Bits	External Data Bus: 8 Bits
2n		
2n + 1		

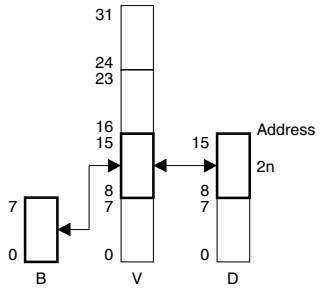
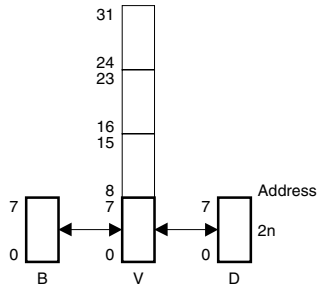
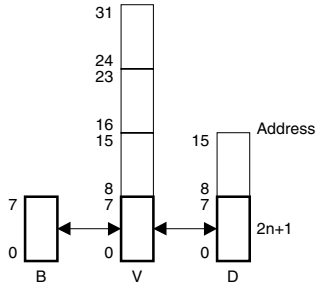
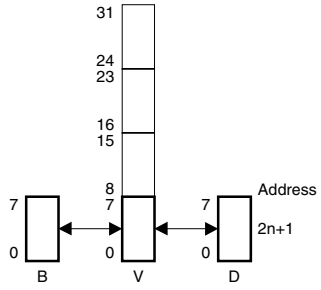
Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-28. Byte Access (Big Endian) (1/2)

Address To Be Accessed	Data Transfer Flow
	External Data Bus: 32 Bits
4n	
4n + 1	
4n + 2	
4n + 3	

Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-28. Byte Access (Big Endian) (2/2)

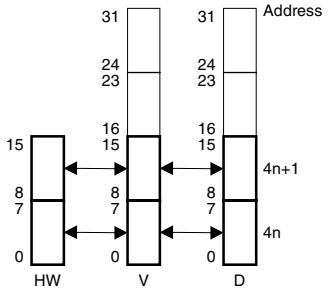
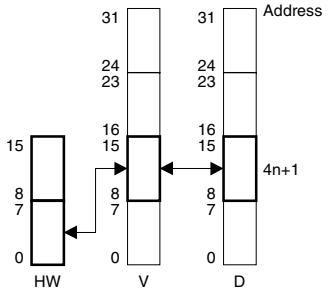
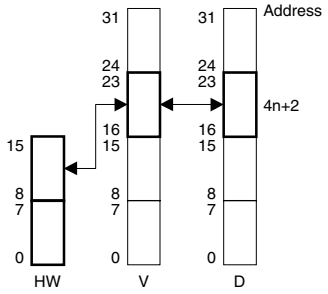
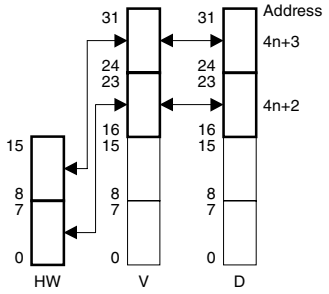
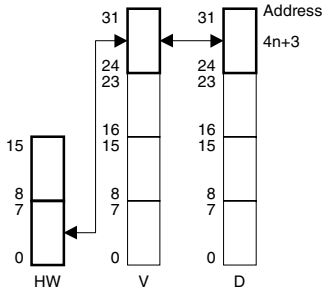
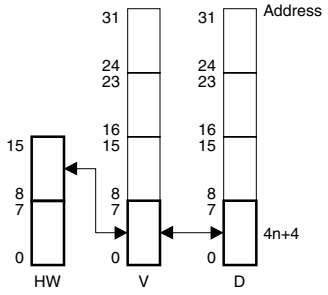
Address To Be Accessed	Data Transfer Flow	
	External Data Bus: 16 Bits	External Data Bus: 8 Bits
2n		
2n + 1		

Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

1.5.2 Data flow for halfword access (16 bits)

Figure 1-29. Halfword Access (Little Endian) (1/2)

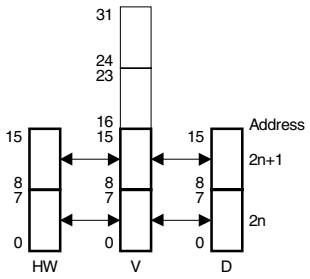
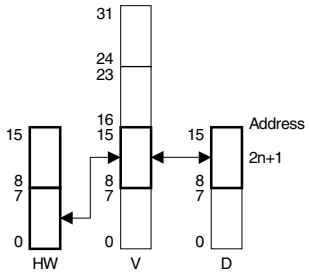
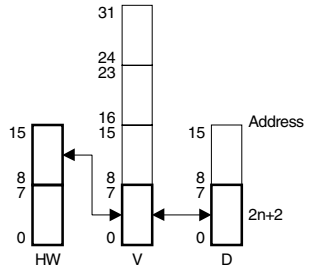
(a) External data bus: 32 bits

Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
4n		—
4n + 1		
4n + 2		—
4n + 3		

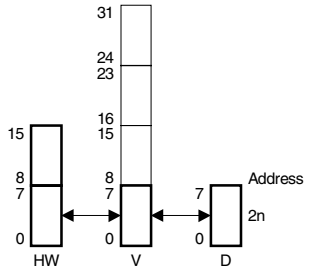
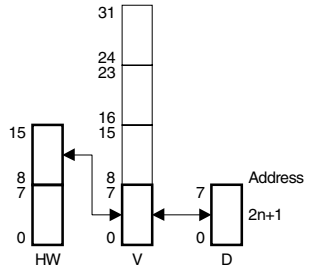
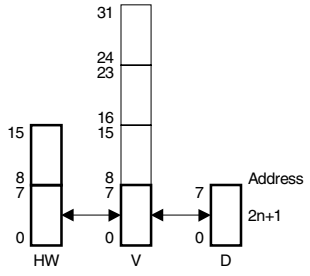
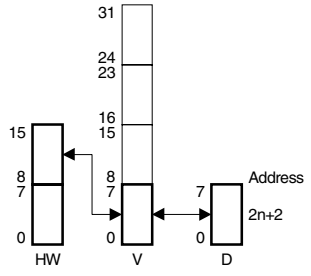
Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-29. Halfword Access (Little Endian) (2/2)

(b) External data bus: 16 bits

Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		—
2n + 1		

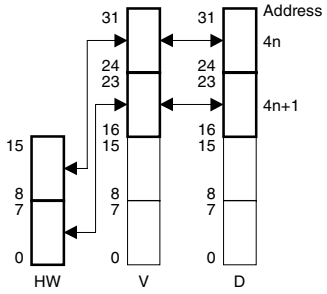
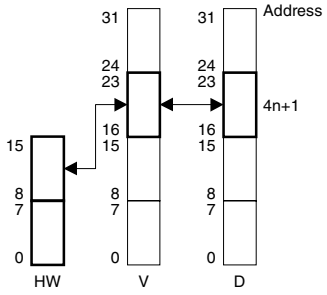
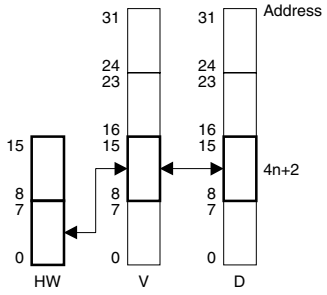
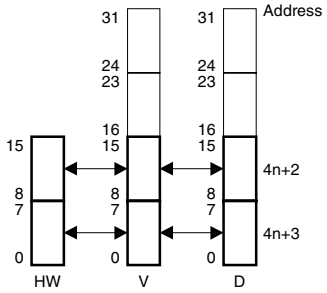
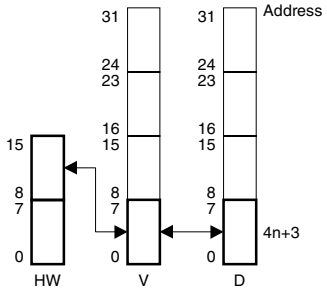
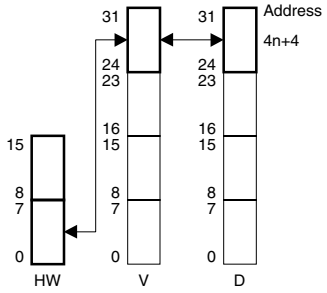
(c) External data bus: 8 bits

Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		
2n + 1		

Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-30. Halfword Access (Big Endian) (1/2)

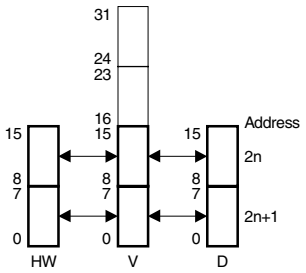
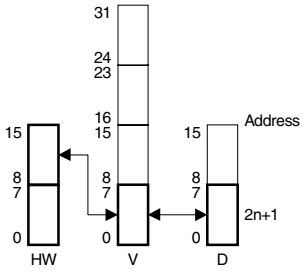
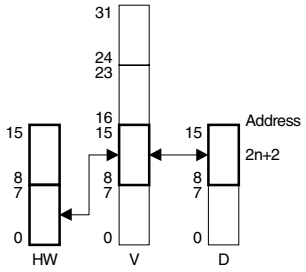
(a) External data bus: 32 bits

Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
4n		—
4n + 1		
4n + 2		—
4n + 3		

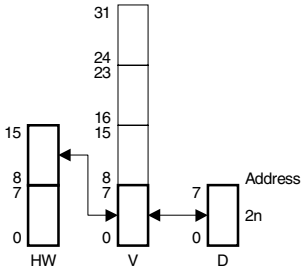
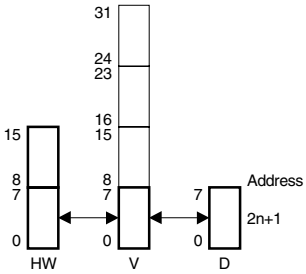
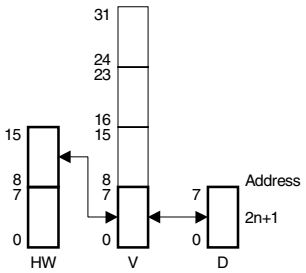
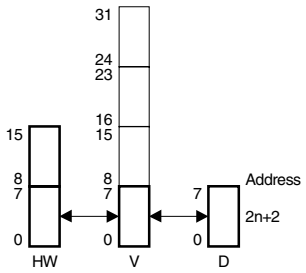
Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-30. Halfword Access (Big Endian) (2/2)

(b) External data bus: 16 bits

Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		—
2n + 1		

(c) External data bus: 8 bits

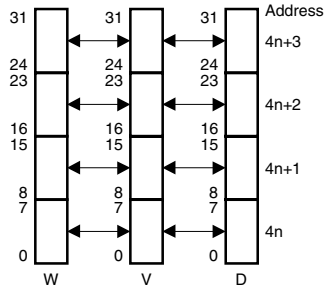
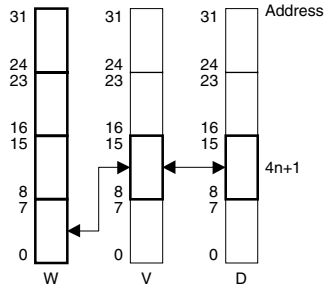
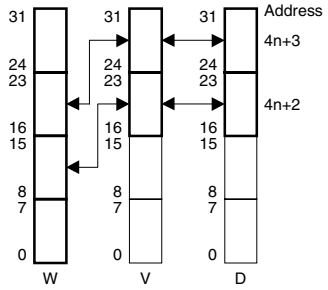
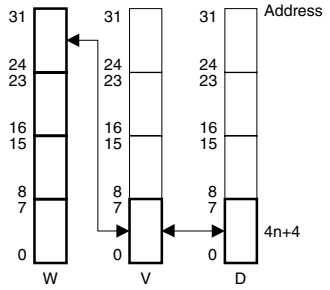
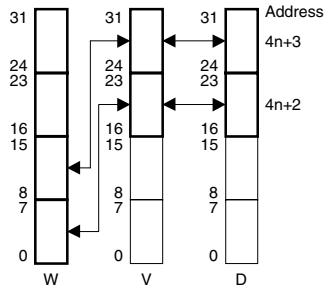
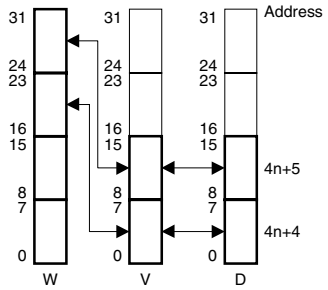
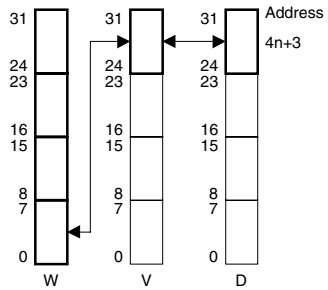
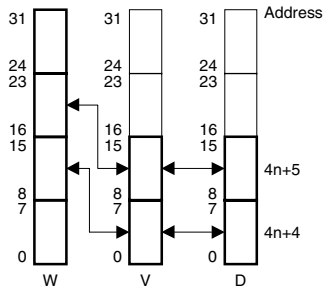
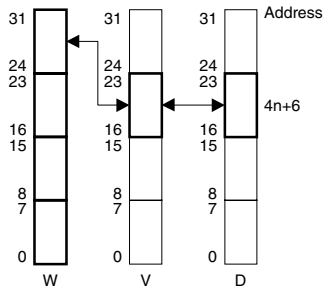
Address To Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		
2n + 1		

Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

1.5.3 Data flow for word access (32 bits)

Figure 1-31. Word Access (Little Endian) (1/3)

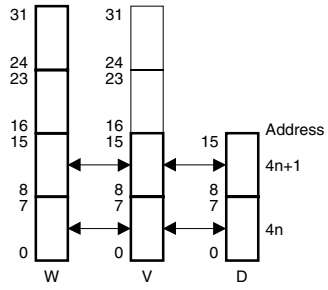
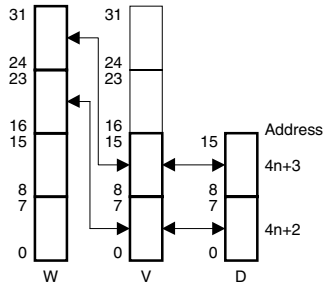
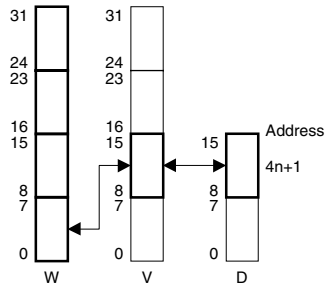
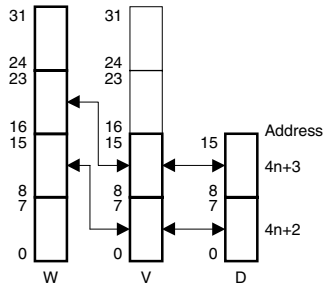
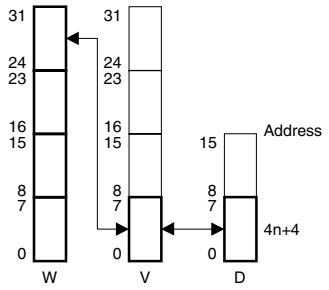
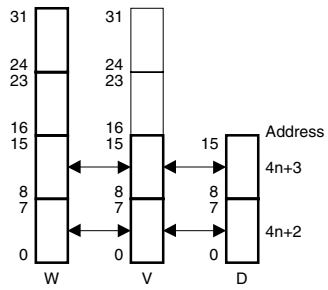
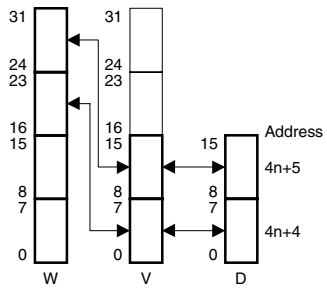
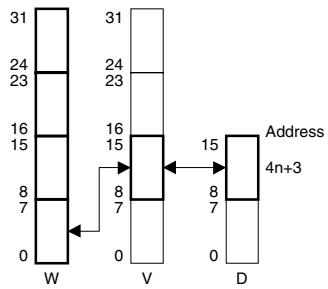
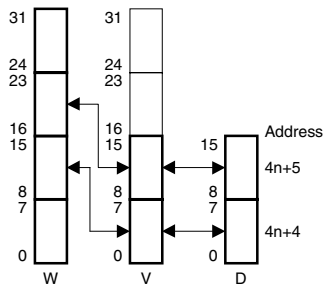
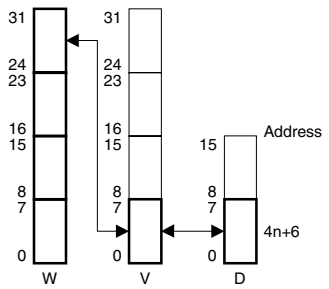
(a) External data bus: 32 bits

Address To Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n		—	—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-31. Word Access (Little Endian) (2/3)

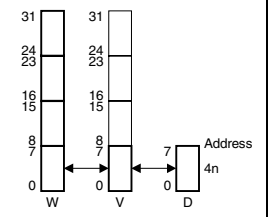
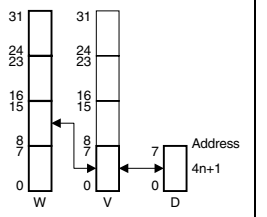
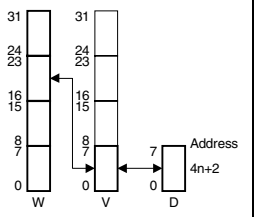
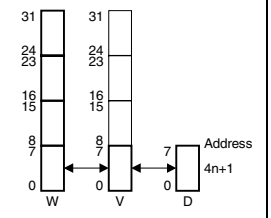
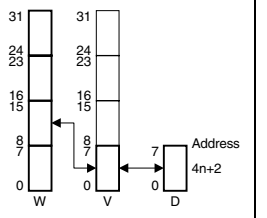
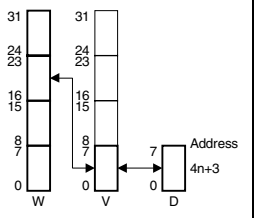
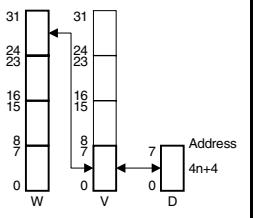
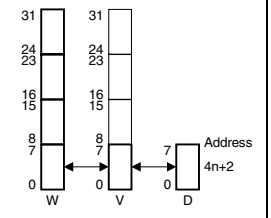
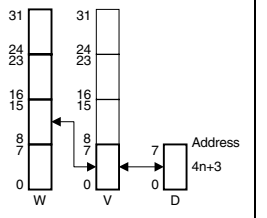
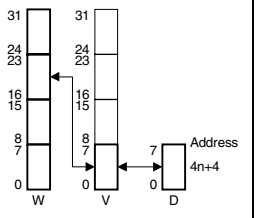
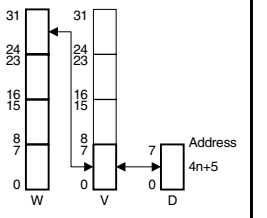
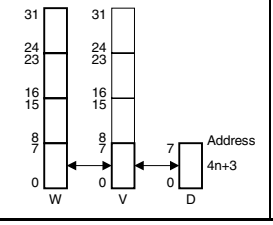
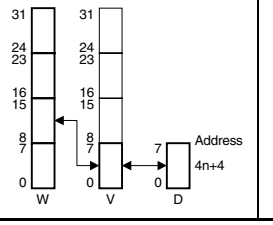
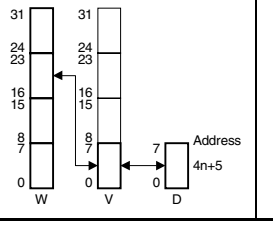
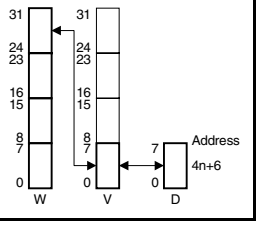
(b) External data bus: 16 bits

Address To Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n			—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-31. Word Access (Little Endian) (3/3)

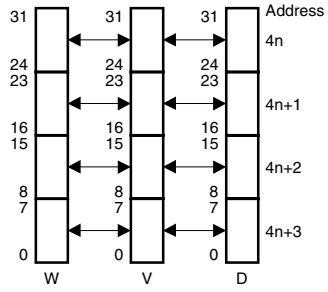
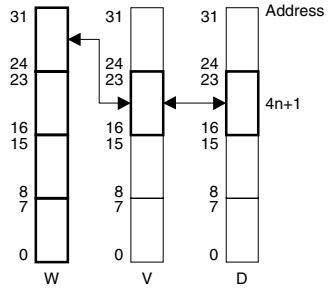
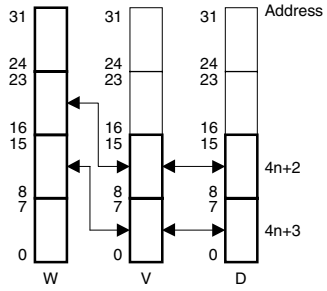
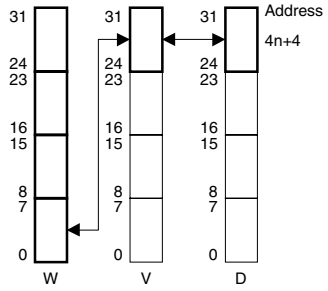
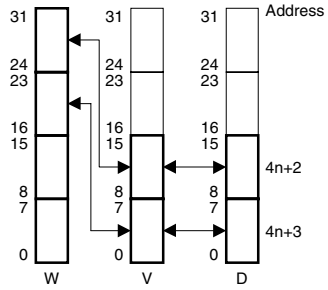
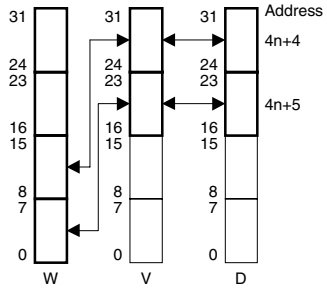
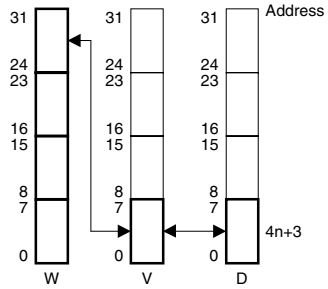
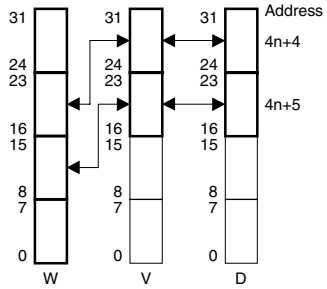
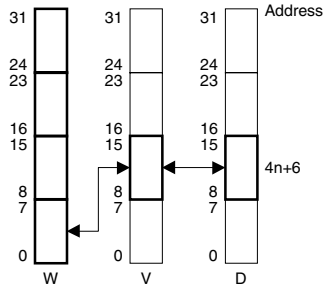
(c) External data bus: 8 bits

Address To Be Accessed	Data Transfer Flow			
	First Time	Second Time	Third Time	Fourth Time
4n				
4n + 1				
4n + 2				
4n + 3				

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-32. Word Access (Big Endian) (1/3)

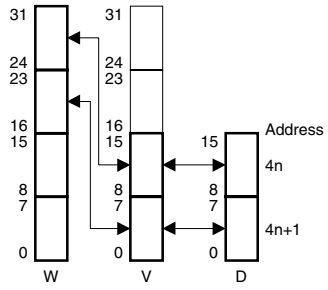
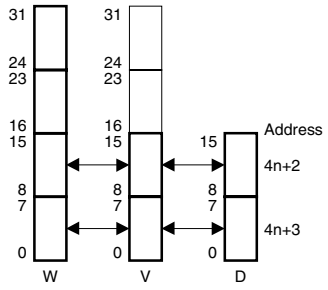
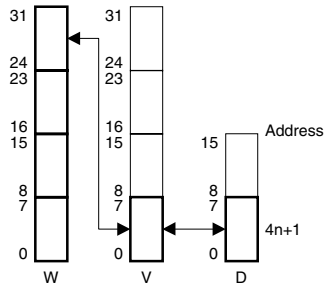
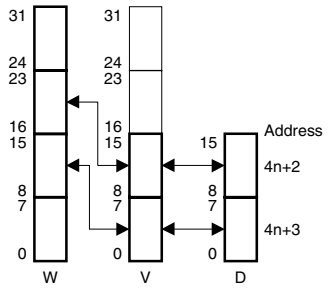
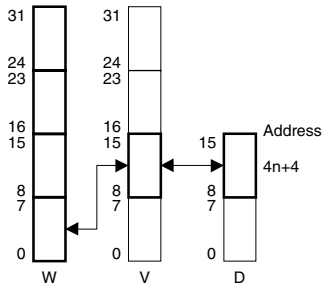
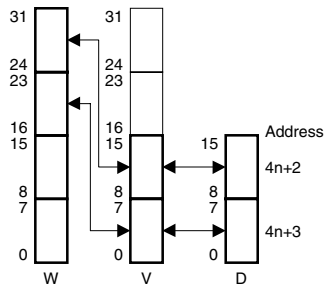
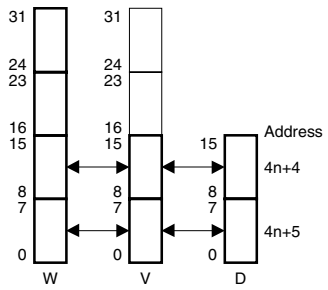
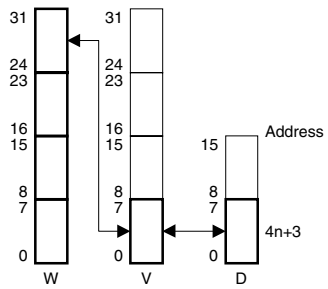
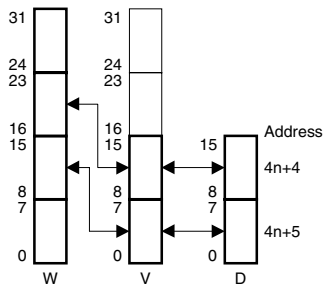
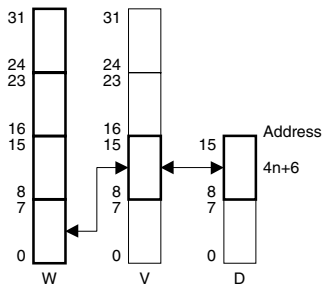
(a) External data bus: 32 bits

Address To Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n		—	—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-32. Word Access (Big Endian) (2/3)

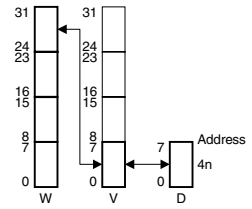
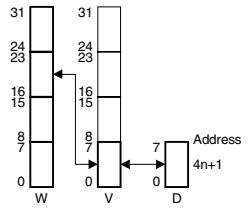
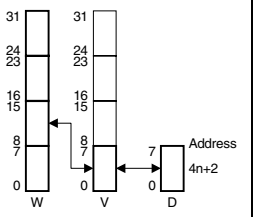
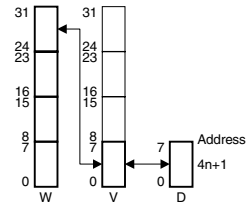
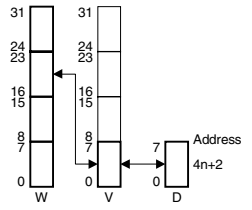
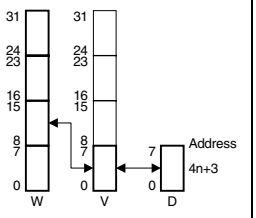
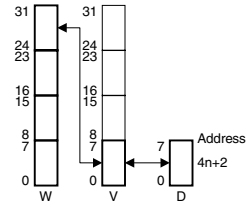
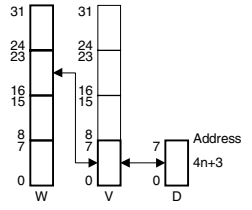
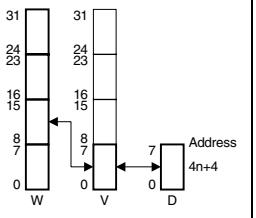
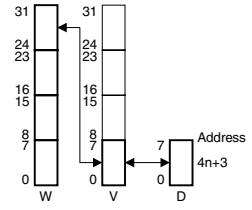
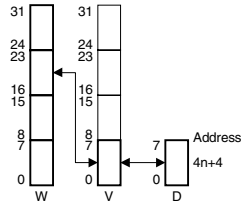
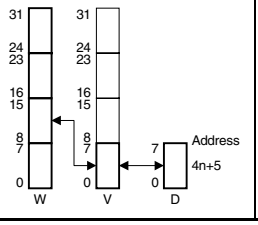
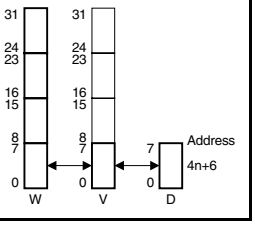
(b) External data bus: 16 bits

Address To Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n			—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-32. Word Access (Big Endian) (3/3)

(c) External data bus: 8 bits

Address To Be Accessed	Data Transfer Flow			
	First Time	Second Time	Third Time	Fourth Time
4n				
4n + 1				
4n + 2				
4n + 3				

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

CHAPTER 2 NT85E502

2.1 Outline

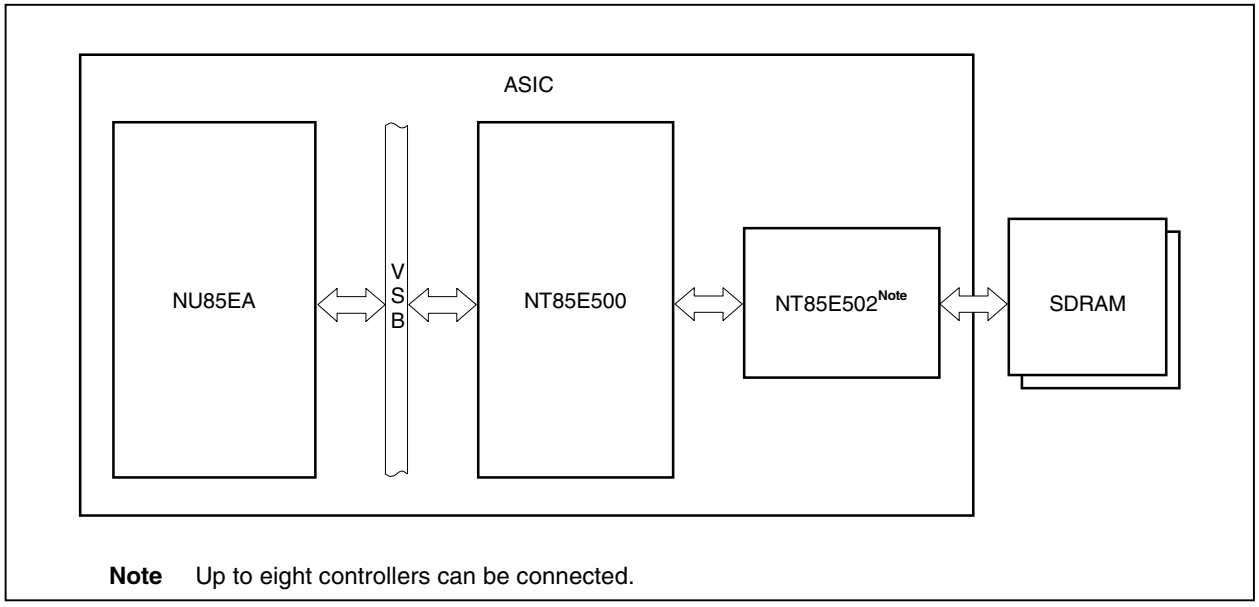
The NT85E502 is a macro for controlling synchronous DRAM (SDRAM).

An external SDRAM bus cycle can be started by connecting the NT85E502 to the NU85EA via the NT85E500 and the VSB.

The NT85E502 is used connected to the NT85E500.

Up to eight NT85E502 controllers can be connected.

Figure 2-1. NT85E500 and NT85E502 Connection Example



Note Up to eight controllers can be connected.

Remark The NT85E502 only supports 12 row addresses and 10 column addresses. Therefore, only SDRAMs of 128 Mb or less can be connected.

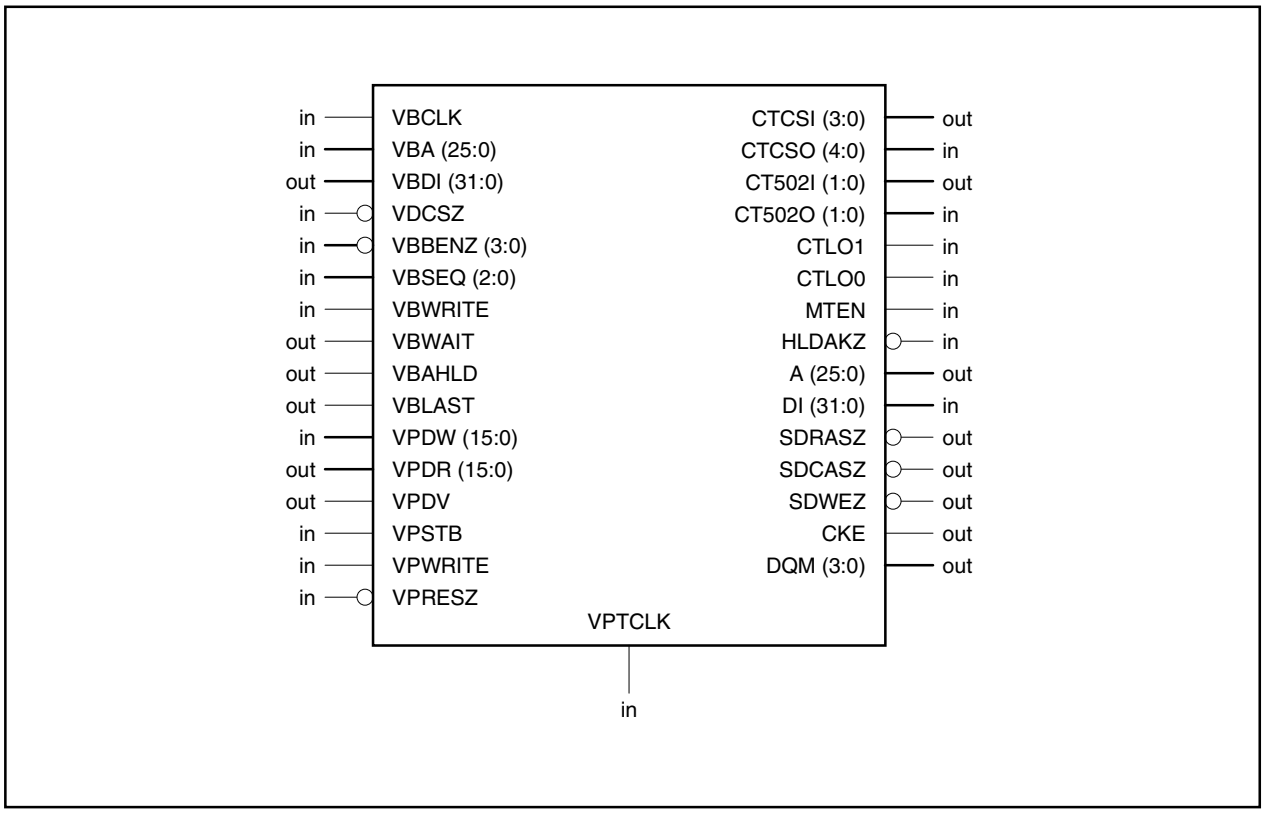
The maximum CS area in 256 MB mode is the 64 MB area of CS1, CS3, CS4, and CS6. If assigning SDRAMs to all of this 64 MB area, it is necessary that this area supports 512 Mb (64 MB) with a 128 Mb (4 Mwords × 8 bits × 4 banks) × 4 configuration, and 32-bit bus access.

2.1.1 Features

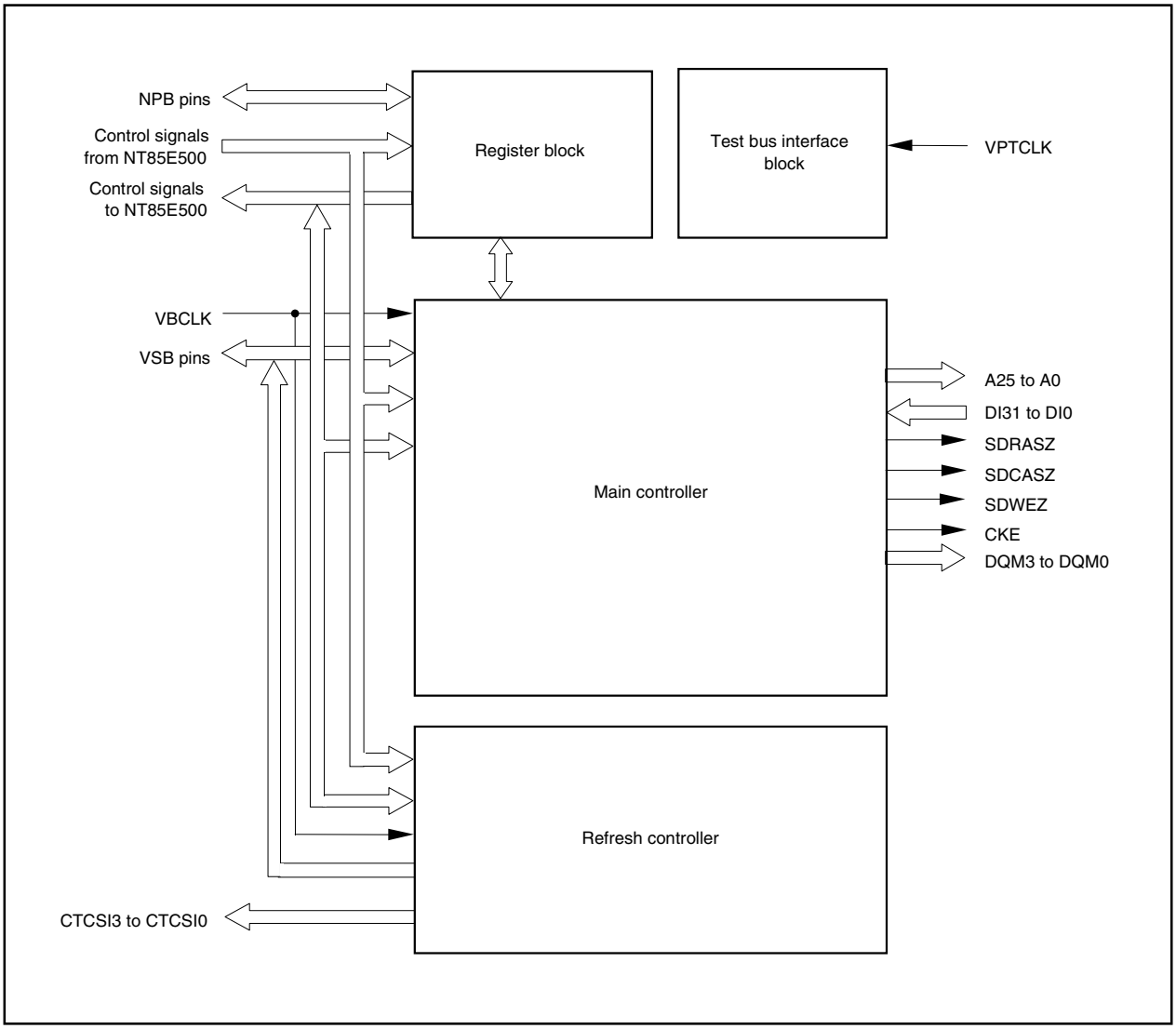
- Only a single access can be started.
- A command for continuous access indicated by the VBSEQ2 to VBSEQ0 pins can be issued continuously after a one-clock interval, for example in the following cases.
  - When the external data bus is 8 bits and 16-/32-bit data is being read/written
  - When the external data bus is 16 bits and 32-bit data is being read/written
  - When the instruction cache/data cache is being refilled
- CAS latency = 2 and 3 are supported.
- An address multiplex function is available.
- The column address width can be changed by means of an SCRn register setting.
- Up to 3 wait states can be inserted by means of an SCRn register setting.
- A register write operation can be executed for each write access to the SCRn register.
- A CBR (CAS before RAS) refresh command can be issued.

Remark n = 7 to 0

2.1.2 Symbol diagram



2.1.3 Block diagram

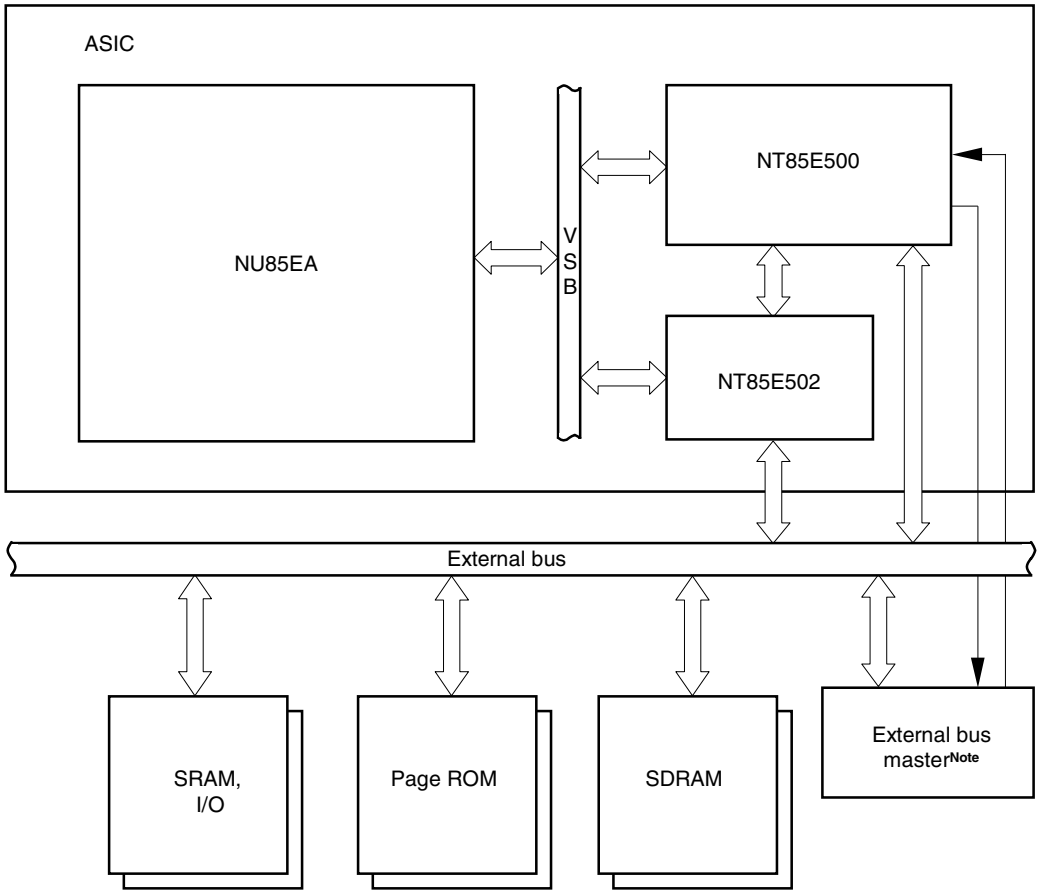


2.1.4 Configuration example

The NT85E502 starts bus cycles for external SDRAM.

The following figure shows an application example using the NT85E502.

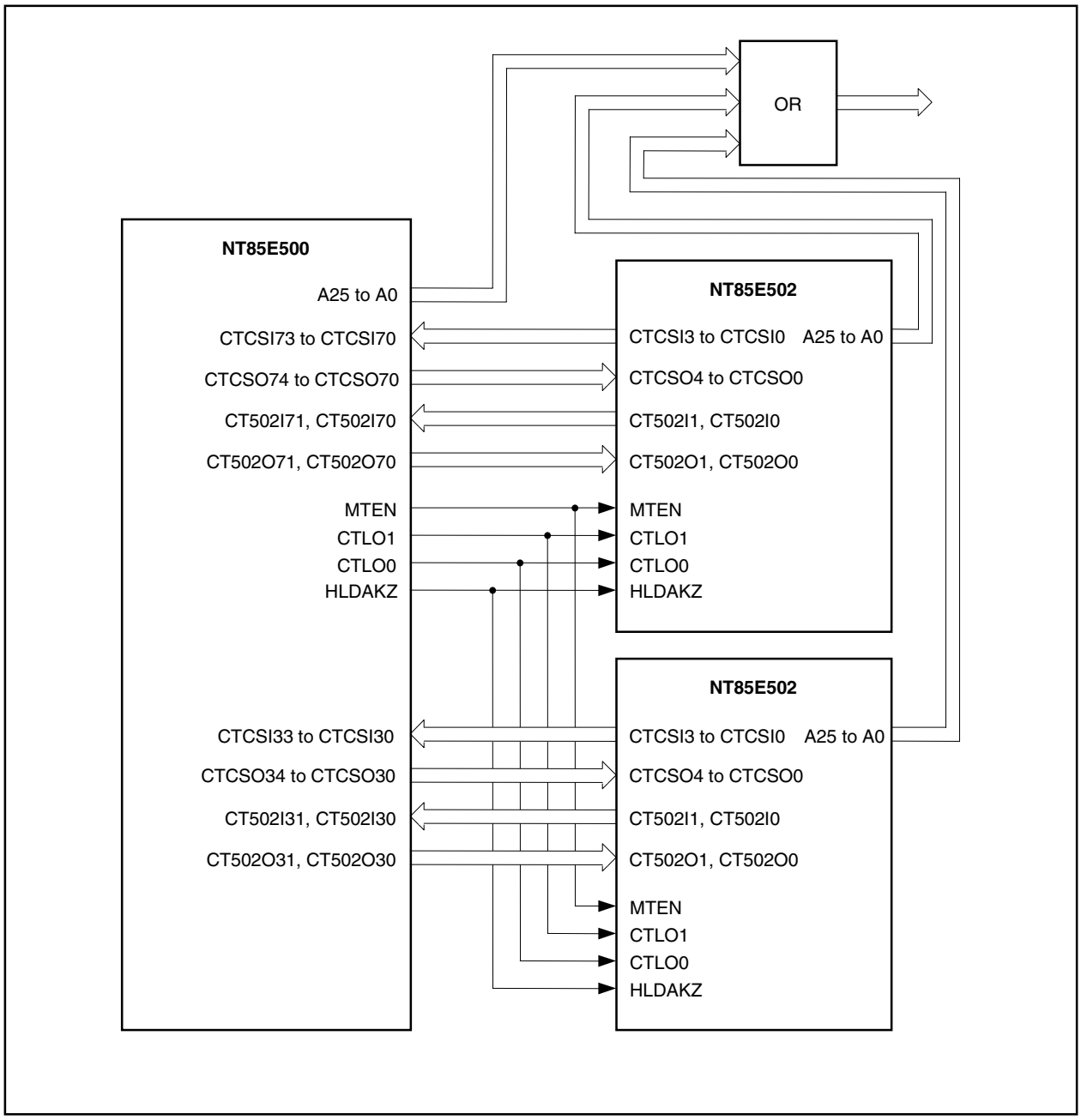
Figure 2-2. Application Example



Note The NT85E500 has an external bus master arbitration function, which is controlled by the HLDRQZ and HLDAKZ signals.

The following figure shows an example of the connections between the NT85E500 and NT85E502 controllers. In this example, the NT85E502 controllers are connected to the CS7 and CS3 areas.

Figure 2-3. Connection Example



2.1.5 Functional differences between NT85E502 and NU85E502

Item		NT85E502	NU85E502
Target CPU core		NU85EA, NU85ET	NB85E, NB85ET
VSB data bus (n = 31 to 0)		VBDIn	VBDn
NPB data bus (n = 15 to 0)		VPDWn (input), VPDRn (output)	VPDn (I/O)
NPB data output bus control pin		VPDV	(None)
I/O timing	Data bus (n = 31 to 0)	VBDIn	VBDn
	Transfer response signal	VBWAIT, VBLAST, VBAHLD	
Pin status after reset, during idle	VBDI31 to VBDI0, VBWAIT, VBAHLD, VBLAST, VPD15 to VPD0	Low-level output	High impedance

2.2 Pin Functions

2.2.1 List of pin functions

Pin Name		I/O	Function
NU85EA connection pins	VBCLK	Input	Internal system clock input
	VBA25 to VBA0	Input	Address input (for VSB)
	VBDI31 to VBDI0	Output	Data output (for VSB)
	VDCSZ	Input	Chip select input (for VSB)
	VBBENZ3 to VBBENZ0	Input	Byte enable input (for VSB)
	VBSEQ2 to VBSEQ0	Input	Sequential status input (for VSB)
	VBWRITE	Input	Read/write status input (for VSB)
	VBWAIT	Output	Wait response output (for VSB)
	VBAHLD	Output	Address hold response output (for VSB)
	VBLAST	Output	Last response output (for VSB)
	VPDW15 to VPDW0	Input	Data input (for NPB)
	VPDR15 to VPDR0	Output	Data output (for NPB)
	VPDV	Output	Data output (VPDR15 to VPDR0) control output (for NPB)
	VPSTB	Input	Data strobe input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPRESZ	Input	Reset input
NT85E500 connection pins	CTCSI3 to CTCSI0	Output	Control output to NT85E500
	CTCSO4 to CTCSO0	Input	Control input from NT85E500
	CT502I1, CT502I0	Output	Control output to NT85E500
	CT502O1, CT502O0	Input	Control input from NT85E500
	CTLO1, CTLO0	Input	Control input from NT85E500
	MTEN	Input	Test mode enable input from NT85E500
	HLDAKZ	Input	Bus hold status input from NT85E500
External memory connection pins	A25 to A0	Output	External memory address output
	DI31 to DI0	Input	External memory data input
	SDRASZ	Output	SDRAM row address strobe output
	SDCASZ	Output	SDRAM column address strobe output
	SDWEZ	Output	SDRAM data write enable output
	CKE	Output	Clock enable output
	DQM3 to DQM0	Output	Data mask output
Test mode pin	VPTCLK	Input	Test clock input

2.2.2 Explanation of pin functions

(1) NU85EA connection pins

(a) VBCLK (input)

This is the external clock input pin for the internal system clock. A 50% duty stable clock is input from an external clock controller.

(b) VBA25 to VBA0 (input)

These pins constitute an address input bus for the VSB and are connected to the VMA25 to VMA0 pins of the NU85EA.

(c) VBDI31 to VBDI0 (output)

These pins constitute a data output bus for the VSB and are connected to the VBDI31 to VBDI0 pins of the NU85EA.

(d) VDCSZ (input)

This is the low-level active chip select input pin and is connected to the VDCSZn pin of the NU85EA (n = 7 to 0). For further details, refer to the **NU85E Hardware User's Manual (A14874E).**

(e) VBBENZ3 to VBBENZ0 (input)

These are low-level active input pins that indicate the valid byte data out of the four data bus (VBDI31 to VBDI0) parts and are connected to the VMBENZ3 to VMBENZ0 pins of the NU85EA.

Table 2-1. VBBENZ3 to VBBENZ0 Signals

Active (Low-Level Input) Signal	Valid Byte Data
VBBENZ3	VBDI31 to VBDI24
VBBENZ2	VBDI23 to VBDI16
VBBENZ1	VBDI15 to VBDI8
VBBENZ0	VBDI7 to VBDI0

(f) VBSEQ2 to VBSEQ0 (input)

These are pins that input the sequential status indicating the transfer size during burst transfer and are connected to the VMSEQ2 to VMSEQ0 pins of the NU85EA.

These pins indicate "burst transfer length" at the start of burst transfer, "continuous" during burst transfer, and "single transfer" at the end of burst transfer.

Table 2-2. VBSEQ2 to VBSEQ0 Signals

VBSEQ2	VBSEQ1	VBSEQ0	Sequential Status
0	0	0	Single transfer
0	0	1	Continuous (indicates that the next transfer address is related to the current transfer address)[Note]
0	1	0	Continuous 4 times (burst transfer length: 4)
0	1	1	Continuous 8 times (burst transfer length: 8)
1	0	0	Continuous 16 times (burst transfer length: 16)
1	0	1	Continuous 32 times (burst transfer length: 32)
1	1	0	Continuous 64 times (burst transfer length: 64)
1	1	1	Continuous 128 times (burst transfer length: 128)

Note This is output during continuous 2 times, or continuous 4, 8, 16, 32, 64, or 128 times transfer.

Remark 0: Low-level input 1: High-level input

(g) VBWRITE (input)

This is an input pin that indicates the data transfer direction (read/write status) and is connected to the VMWRITE pin of the NU85EA.

It inputs a high level during write access.

(h) VBWAIT (output)

This is the wait response pin and is connected to the VMWAIT pin of the NU85EA.

This signal is output to the bus master to request additional bus cycles because the data output preparations have not completed.

When this signal becomes high level, the bus cycle changes to the wait status.

(i) VBAHLD (output)

This is the address hold response pin and is connected to the VMAHLD pin of the NU85EA.

This signal is output to the bus master to request additional bus cycles when the data output preparations have completed.

When this signal and the VBWAIT signal become high level, the bus cycle goes into the address hold status.

Since, in the address hold status, addresses do not change even during the data read and write cycles, there is no need to latch addresses and the circuit can thus be kept simple.

When the number of idle states is set to 1 or more (BCn1 and BCn0 bits of BCC register = 01B or more), the NT85E502 activates the VBAHLD signal during idle state at the end of a read cycle of an SDRAM.

(j) VBLAST (output)

This is the last response pin and is connected to the VMLAST pin of the NU85EA. This pin is used when the bus decoder requires a decode cycle.

In the case of a system where several slave devices are connected externally and a bus decoder has been added to select slaves, decoding for bus slave selection is normally performed during non-sequential transfer.

Thus even when attempts to change a slave device are made during sequential transfer such as burst transfer, the decode cycle for slave selection cannot be issued.
In such a case, the slave device outputs a last response notifying the fact that the slave selection signal has changed to the bus master. When there is a last response from the slave device, the bus master makes the next bus cycle non-sequential transfer to enable decode cycle issuance.
The NT85E502 cannot activate the VBLAST signal.

(k) VPDW15 to VPDW0 (input)

These pins constitute a data input bus for NPB and are connected to the VPDO15 to VPDO0 pins of the NU85EA.

(l) VPDR15 to VPDR0 (output)

These pins constitute a data output bus for NPB and are connected to the VPDI15 to VPDI0 pins of the NU85EA.

(m) VPDV (output)

This is the data output (VPDR15 to VPDR0) control signal output pin. It outputs a high level during read. To configure a bidirectional data bus, connect this pin to the 3-state buffer enable pin connected to the data bus for data output control.
This pin is not used when connecting with the NU85EA, therefore leave this pin open.

(n) VPSTB (input)

This is the data strobe output pin for NPB.

(o) VPWRITE (input)

This is the write access strobe input pin for the VPDW15 to VPDW0 signals.
It inputs a high level during write.

(p) VPRESZ (input)

This is the input pin for a system reset output from the NU85EA.

(2) NT85E500 connection pins

(a) CTCSI3 to CTCSI0 (output)

These are pins for controlling output to the NT85E500.

(b) CTCSO4 to CTCSO0 (input)

These are pins for controlling input from the NT85E500.

(c) CT502I1 and CT502I0 (output)

These are pins for controlling output to the NT85E500.

(d) CT502O1 and CT502O0 (input)

These are pins for controlling input from the NT85E500.

(e) CTLO1 and CTLO0 (input)

These are pins for controlling input from the NT85E500.

(f) MTEN (input)

This is the pin to which the test mode enable is input from the NT85E500.

(g) HLDAKZ (input)

This is the pin to which the bus hold status is input from the NT85E500.

This is used only when the external bus master accesses SDRAM during a bus hold. Input a high level when not being used.

Cautions 1. When accessing the SDRAM using the external bus master during a bus hold, be sure to perform access after issuing the precharge command.

2. Do not rewrite SDRAM configuration register n (SCRn) (n = 7 to 0) using the external bus master during a bus hold.

Remark After releasing a bus hold, when the NT85E502 regains bus mastership and accesses SDRAM, access starts from all bank precharge.

(3) External memory connection pins

(a) A25 to A0 (output)

These pins constitute the external SDRAM address bus.

When the VDCSZ signal is inactive, all of the pins A25 to A0 output a low-level signal.

(b) DI31 to DI0 (input)

These pins constitute the external SDRAM data bus.

(c) SDRASZ (output)

This is the row address strobe output pin for external SDRAM.

(d) SDCASZ (output)

This is the column address strobe output pin for external SDRAM.

(e) SDWEZ (output)

This is the data write enable output pin for external SDRAM.

(f) CKE (output)

This is the clock enable output pin for external SDRAM.

This pin outputs an inactive (low level) during a self-refresh cycle.

(g) DQM3 to DQM0 (output)

These are the data mask output pins for external SDRAM.

During a write cycle, they output the same values as the VMBENZ3 to VMBENZ0 signals of the NU85EA when a write command is performed. During a read cycle, the DQM3 to DQM0 pins all output a low level after a read command is performed.

(4) Test mode pin

(a) VPTCLK (input)

This is a test clock input pin.

2.2.3 Recommended connection of unused pins

Pin Name		I/O	Recommended Connection Method
★ NU85EA connection pin	VPDV	Output	Leave open.
External memory connection pins	A25 to A0, SDRASZ, SDCASZ, SDWEZ, CKE, DQM3 to DQM0	Output	Leave open.
	DI31 to DI0	Input	Input low level.

2.2.4 Pin status

The following table shows the status in each operating mode of the pins that have output functions.

Table 2-3. Pin Status in Each Operating Mode

Pin Name		Pin Status				
		Reset	STOP Mode	HALT Mode	Bus Hold	Test Mode
NU85EA connection pins	VBDI31 to VBDI0	L	L	Operating	L	Operating
	VBWAIT	L	L	Operating	L	Operating
	VBAHLD	L	L	Operating	L	Operating
	VBLAST	L	L	Operating	L	Operating
	VPDR15 to VPDR0	L	L	Operating	L	Operating
	VPDV	L	L	Operating	L	Operating
NT85E500 connection pins	CTCSI3 to CTCSI0	L	Retained	Operating	L	Operating
	CT502I1, CT502I0	L	Retained	Operating	L	Operating
External memory connection pins	A25 to A0	Undefined	Retained	Operating	L	Operating
	SDRASZ	H	H	Operating	H	Operating
	SDCASZ	H	H	Operating	H	Operating
	SDWEZ	H	H	Operating	H	Operating
	CKE	H	L	Operating	H	Operating
	DQM3 to DQM0	H	H	Operating	H	Operating

Remark L: Low-level output
H: High-level output
Retained: Retains the previous status

2.3 Bus Cycle Function

In the bus cycle function of the NT85E502, the operation settings are made using the following control registers, which are assigned to the peripheral I/O area of the NU85EA.

Address	Register Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FFFFF4A0H	SDRAM configuration register 0	SCR0	R/W			√	0000H
FFFFF4A2H	SDRAM refresh control register 0	RFS0	R/W			√	0000H
FFFFF4A4H	SDRAM configuration register 1	SCR1	R/W			√	0000H
FFFFF4A6H	SDRAM refresh control register 1	RFS1	R/W			√	0000H
FFFFF4A8H	SDRAM configuration register 2	SCR2	R/W			√	0000H
FFFFF4AAH	SDRAM refresh control register 2	RFS2	R/W			√	0000H
FFFFF4ACH	SDRAM configuration register 3	SCR3	R/W			√	0000H
FFFFF4AEH	SDRAM refresh control register 3	RFS3	R/W			√	0000H
FFFFF4B0H	SDRAM configuration register 4	SCR4	R/W			√	0000H
FFFFF4B2H	SDRAM refresh control register 4	RFS4	R/W			√	0000H
FFFFF4B4H	SDRAM configuration register 5	SCR5	R/W			√	0000H
FFFFF4B6H	SDRAM refresh control register 5	RFS5	R/W			√	0000H
FFFFF4B8H	SDRAM configuration register 6	SCR6	R/W			√	0000H
FFFFF4BAH	SDRAM refresh control register 6	RFS6	R/W			√	0000H
FFFFF4BCH	SDRAM configuration register 7	SCR7	R/W			√	0000H
FFFFF4BEH	SDRAM refresh control register 7	RFS7	R/W			√	0000H

2.3.1 SDRAM configuration register n (SCRn)

This register sets the number of waits and the column address width.

When more than one NT85E502 is incorporated in the system, settings can be made for each CSn area (n = 7 to 0).

If this register is written to, the NT85E502 will start a register write operation.

This register can be read or written in 16-bit units.

Cautions 1. An SDRAM read/write cycle will not be generated prior to the execution of a register write operation.
Access SDRAM after waiting 20 clocks following execution of a program that writes to the SCRn register. When setting the SCRn register again after accessing SDRAM, first clear (to 0) the MEn bit of the BCT0 and BCT1 registers in the NT85E500 and then set (1) again (n = 7 to 0).

2. Do not execute continuous write instructions to the SCRn register. Be sure to insert and execute another instruction between write instructions to the SCRn register (n = 7 to 0).

3. When using two or more NT85E502s, do not access the SDRAM area until all the SCRn register settings are completed (n = 7 to 0).

★ **4. Set SDRAM refresh control register n (RFSn) before setting the SCRn register (n = 7 to 0).**

Remarks 1. n of the register name corresponds to the CSn area number.

2. The address decoder is in the NT85E500. For the addresses of each CSn area, refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 2-4. SDRAM Configuration Register n (SCRn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
SCRn	0	LTM2	LTM1	LTM0	0	0	0	0	BCW1	BCW0	SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	FFFFF4A0H + 4n	0000H

Bit position	Bit name	Description
14 to 12	LTM2 to LTM0	Set the CAS latency value of a read operation.

LTM2	LTM1	LTM0	CAS latency
0	0	Don't care	Setting prohibited
0	1	0	2
0	1	1	3
1	Don't care	Don't care	Setting prohibited

Remark n = 7 to 0

Figure 2-4. SDRAM Configuration Register n (SCRn) (2/2)

<table>
<tr><th>Bit position</th><th>Bit name</th><th>Description</th></tr>
<tr><td>7, 6</td><td>BCW1,
BCW0</td><td>Set the number of wait states between the bank active command and the read/write command, or between the precharge command and the bank active command.
<table>
<tr><th>BCW1</th><th>BCW0</th><th>Number of wait states</th></tr>
<tr><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>3</td></tr>
</table></td></tr>
<tr><td>5, 4</td><td>SSO1,
SSO0</td><td>Set the address shift width during On-page judgment.
When the data bus size has been set to either 16 bits or 32 bits, the system does not use the lower addresses (A0 or A1 and A0).
<table>
<tr><th>SSO1</th><th>SSO0</th><th>Address shift width</th></tr>
<tr><td>0</td><td>0</td><td>0 bits (8-bit data bus)</td></tr>
<tr><td>0</td><td>1</td><td>1 bit (16-bit data bus)</td></tr>
<tr><td>1</td><td>0</td><td>2 bits (32-bit data bus)</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>3, 2</td><td>RAW1,
RAW0</td><td>Set the row address width.
<table>
<tr><th>RAW1</th><th>RAW0</th><th>Row address width</th></tr>
<tr><td>0</td><td>0</td><td>11 bits</td></tr>
<tr><td>0</td><td>1</td><td>12 bits</td></tr>
<tr><td>1</td><td>Don’t care</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>1, 0</td><td>SAW1,
SAW0</td><td>Set the column address width.
<table>
<tr><th>SAW1</th><th>SAW0</th><th>Column address width</th></tr>
<tr><td>0</td><td>0</td><td>8 bits</td></tr>
<tr><td>0</td><td>1</td><td>9 bits</td></tr>
<tr><td>1</td><td>0</td><td>10 bits</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
</table>

Table 2-4. Row Address Output

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SAW1 and SAW0 bits = 10	a25 to a18	a17	a16	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10
SAW1 and SAW0 bits = 01	a25 to a18	a17	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9
SAW1 and SAW0 bits = 00	a25 to a18	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9	a8

Table 2-5. Column Address Output

(a) All bank precharge commands

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	a25 to a18	a17	a16	a15	a14	a13	a12	a11	1	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 01	a25 to a18	a17	a16	a15	a14	a13	a12	1	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 10	a25 to a18	a17	a16	a15	a14	a13	1	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

(b) Register write command

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	0	0	0	0	0	0	0	0	0	0	0	0	LTM 2	LTM 1	LTM 0	0	0	0	0
SSO1 and SSO0 bits = 01	0	0	0	0	0	0	0	0	0	0	0	LTM 2	LTM 1	LTM 0	0	0	0	0	0
SSO1 and SSO0 bits = 10	0	0	0	0	0	0	0	0	0	0	LTM 2	LTM 1	LTM 0	0	0	0	0	0	0

(c) Read/write command

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	a25 to a18	a17	a16	a15	a14	a13	a12	a11	0	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 01	a25 to a18	a17	a16	a15	a14	a13	a12	0	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 10	a25 to a18	a17	a16	a15	a14	a13	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

(1) Address outputs and SDRAM connection

The settings of SDRAM configuration register n (SCRn), physical addresses, address outputs from the NT85E502, and connection of the NT85E502 and SDRAM for each data bus width (8 bits, 16 bits, and 32 bits) are described below.

(a) 8-bit data bus

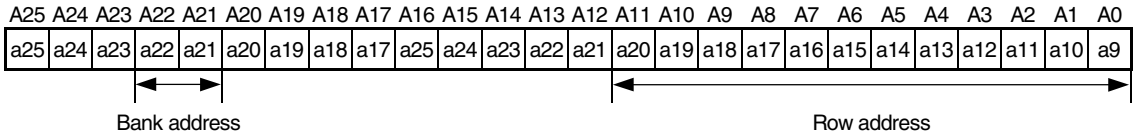
A connection example of 64 Mb SDRAM (2 Mwords × 8 bits × 4 banks) when using an 8-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 00: Data bus width = 8 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 01: Column address width = 9 bits

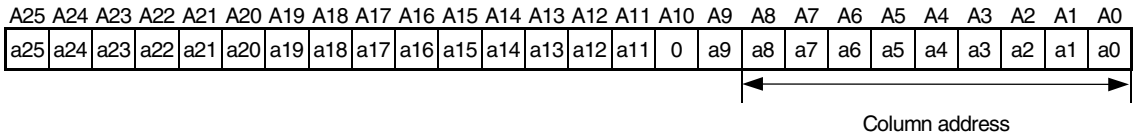
- Physical addresses
  A22, A21: Bank address
  A20 to A9: Row address
  A8 to A0: Column address

- Addresses output from the NT85E502
  A22, A21: Bank address
  A11 to A0: Row address (12 bits), column address (9 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



- Connection of the NT85E502 and SDRAM
  A22, A21 (NT85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A11 to A0 (NT85E502) → A11 to A0 (SDRAM)

(b) 16-bit data bus

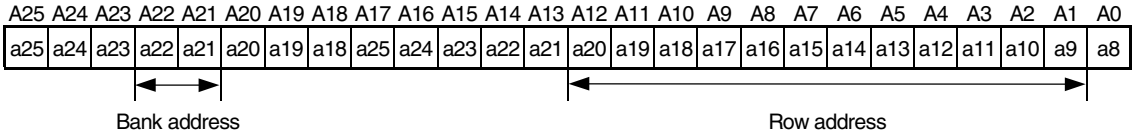
A connection example of 64 Mb SDRAM (1 Mword × 16 bits × 4 banks) when using a 16-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 01: Data bus width = 16 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 00: Column address width = 8 bits

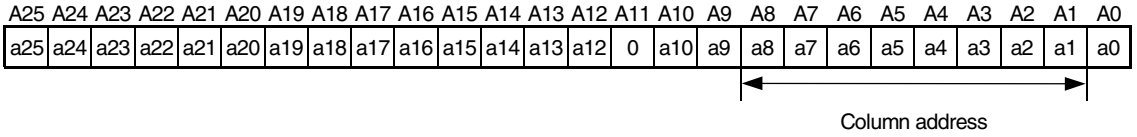
- Physical addresses
  A22, A21: Bank address
  A20 to A9: Row address
  A8 to A1: Column address

- Addresses output from the NT85E502
  A22, A21: Bank address
  A12 to A1: Row address (12 bits), column address (8 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



- Connection of the NT85E502 and SDRAM
  A22, A21 (NT85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A12 to A1 (NT85E502) → A11 to A0 (SDRAM)

(c) 32-bit data bus

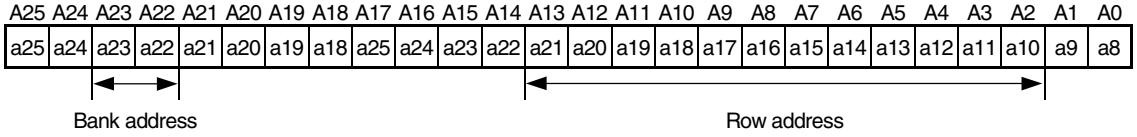
A connection example of 128 Mb SDRAM (64 Mb SDRAM (1 Mword × 16 bits × 4 banks) × 2) when using a 32-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 10: Data bus width = 32 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 00: Column address width = 8 bits

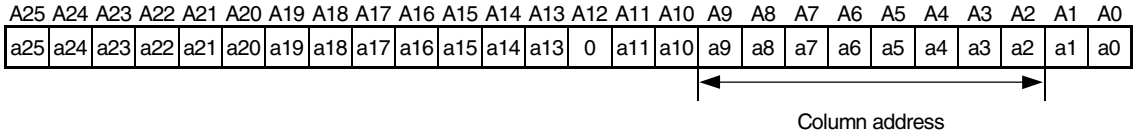
- Physical addresses
  A23, A22: Bank address
  A21 to A10: Row address
  A9 to A2: Column address

- Addresses output from the NT85E502
  A23, A22: Bank address
  A13 to A2: Row address (12 bits), column address (8 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



- Connection of the NT85E502 and SDRAM
  A23, A22 (NT85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A13 to A2 (NT85E502) → A11 to A0 (SDRAM)

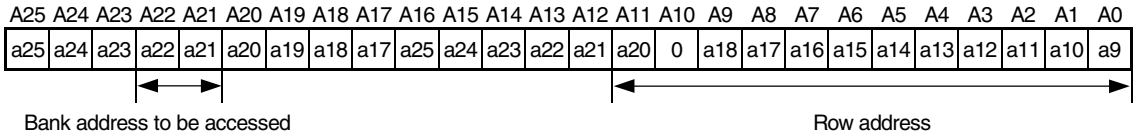
(2) Bank address output

The NT85E502 precharges the bank to be accessed at the row address output immediately after a page change as a bank precharge command. In addition, after a bank change, the NT85E502 precharges the bank accessed last at the column address output. Therefore, since a bank precharge is performed either at the row address output or the column address output, always connect the pins (A22 and A21) of the NT85E502 that output bank addresses to the bank address pins (A13 and A12) of the SDRAM when connection is performed according to the description in **2.3.1 (1) (a) 8-bit data bus.**

Examples of address output upon bank precharge command at a page change and a bank change when connection is performed according to the description in **2.3.1 (1) (a) 8-bit data bus** are described below.

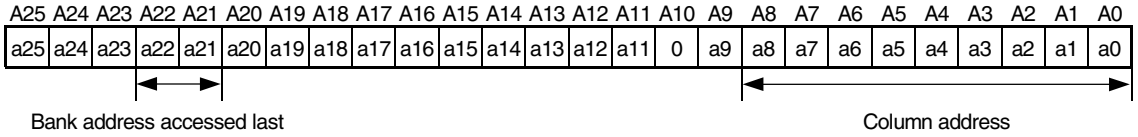
(a) At a page change (8-bit data bus)

Since the bank to be accessed is precharged, the physical addresses (A25 to A9) to be accessed are output from the A25 to A0 pins of the NT85E502.



(b) At a bank change (8-bit data bus)

Since the bank accessed last is precharged, the physical addresses (A25 to A9) accessed last are output from the A25 to A9 pins of the NT85E502.

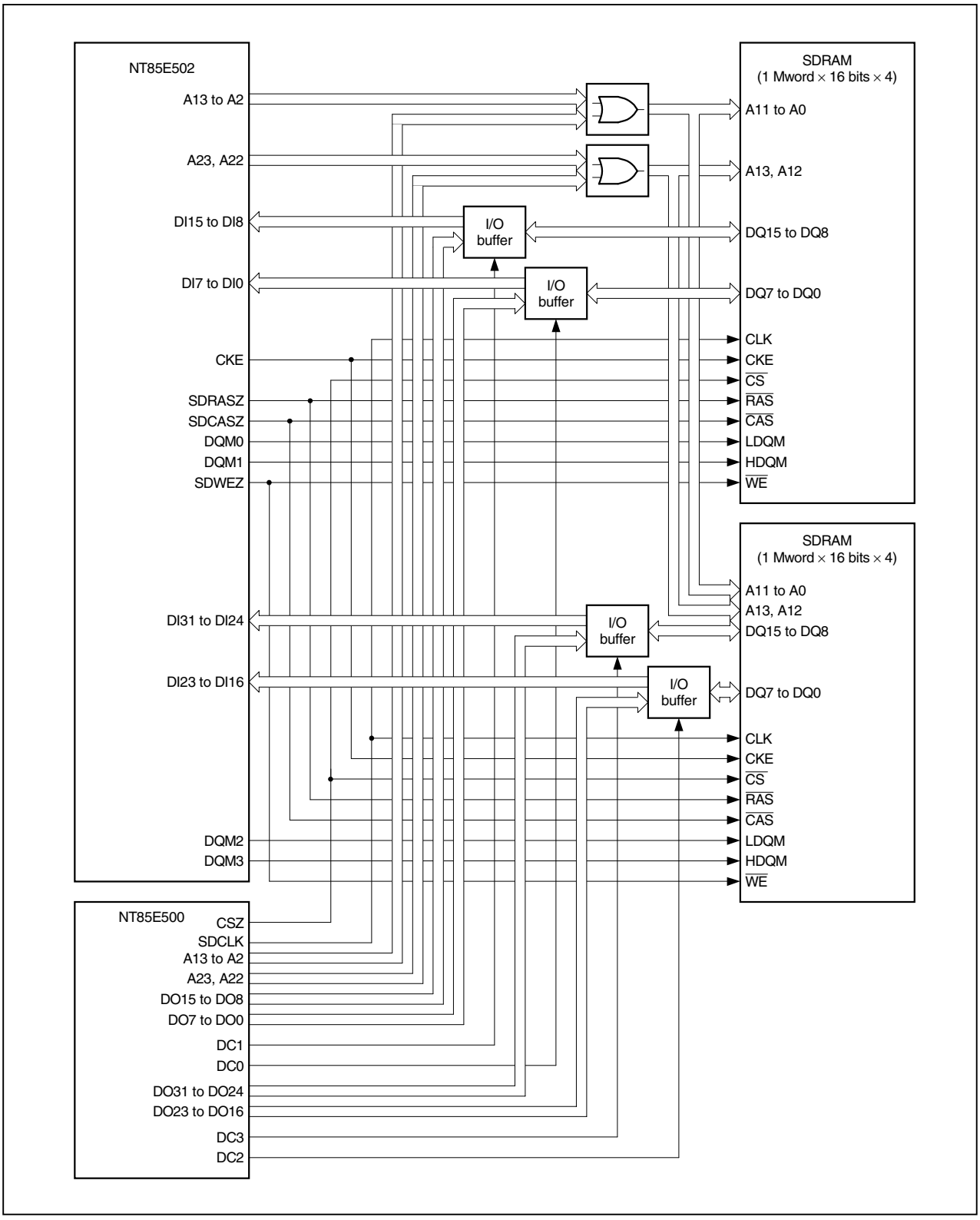


The bit that specifies the precharge mode (A10: 8-bit data bus, A11: 16-bit data bus, A12: 32-bit data bus) outputs a high level upon an all bank precharge command, and a low level during other precharges.

2.3.2 SDRAM cycle

(1) Connection example

Figure 2-5. 64 Mb SDRAM Connection Example



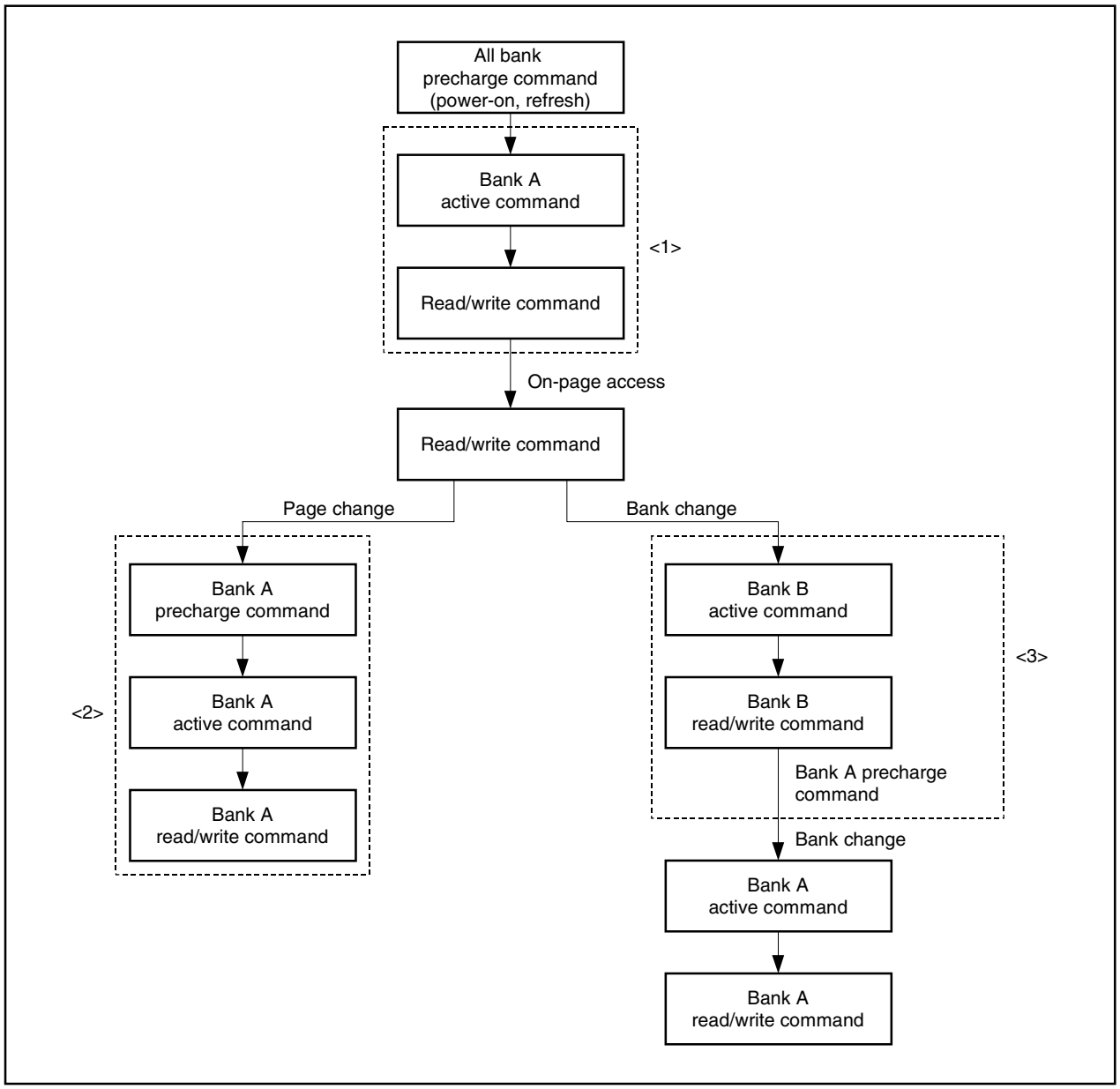
(2) Bus timing

During power-on or refresh, an all bank precharge command is always issued to the SDRAM. Therefore, when the SDRAM is accessed after this, the active command and read/write command are issued in order (<1> in **Figure 2-6**).

When a page change occurs, the precharge command, active command, and read/write command are issued in order (<2> in **Figure 2-6**).

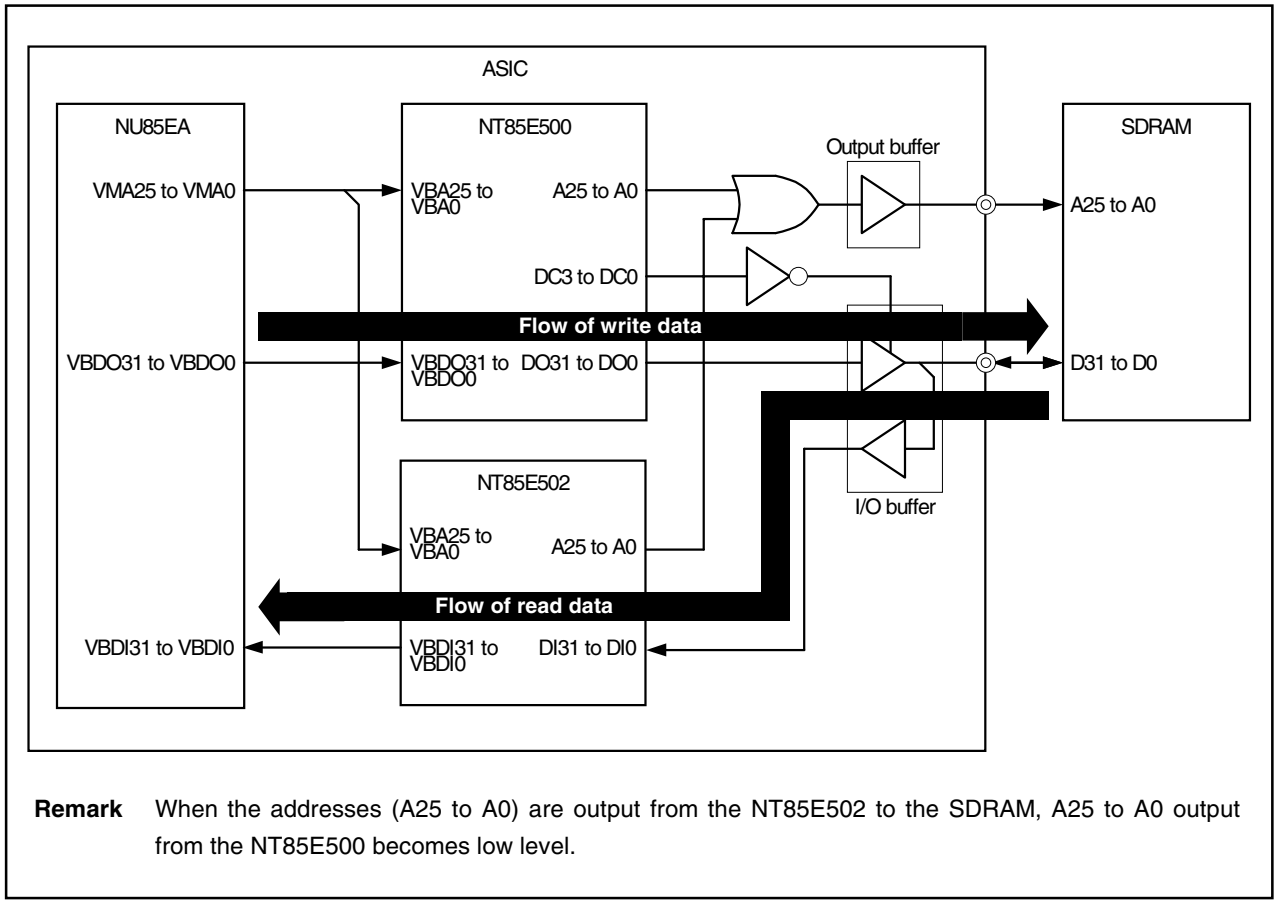
When a bank change occurs, the active command and read/write command for the bank to be accessed next are issued in order. Immediately after the read/write command, the precharge command for the bank that was accessed immediately before the currently accessed bank is issued (<3> in **Figure 2-6**).

Figure 2-6. State Transition of SDRAM Access



The write data to the SDRAM is output from the NT85E500, and the read data from the SDRAM is input to the NT85E502.

Figure 2-7. Read/Write Data Flow for SDRAM



Remark When the addresses (A25 to A0) are output from the NT85E502 to the SDRAM, A25 to A0 output from the NT85E500 becomes low level.

Examples of the bus timing for an SDRAM read or write are shown below. An SDRAM bus cycle consists of the following states.

- ALLPRE state: All bank precharge command state.
- REFW state: Refresh wait state.
- REGW state: Register write command state.
- TACT state: Bank active command state.
- TBCW state: Wait state that is inserted when BCW is set to 2 or 3.
- TI state Idle state that is inserted according to the setting of the BCC register (inserted only during a read operation).
- TLATE state: Latency-amount wait state.
- TPREC state: Bank precharge command state.
- TREAD state: Read command state.
- TREF state: Refresh command state.
- TRPW state: Wait state between the read/write cycles following a register write operation.
- TW state: Wait state.
- TW0 state: Wait state indicating the status of waiting prior to the start of a register write operation.
- TWE state: State indicating the end of the write cycle.
- TWPRE state: State indicating precharge. Precharges the bank accessed last only when the bank changes.
- TWR state: Write command state.

Remarks 1. Circles indicate sampling timing.

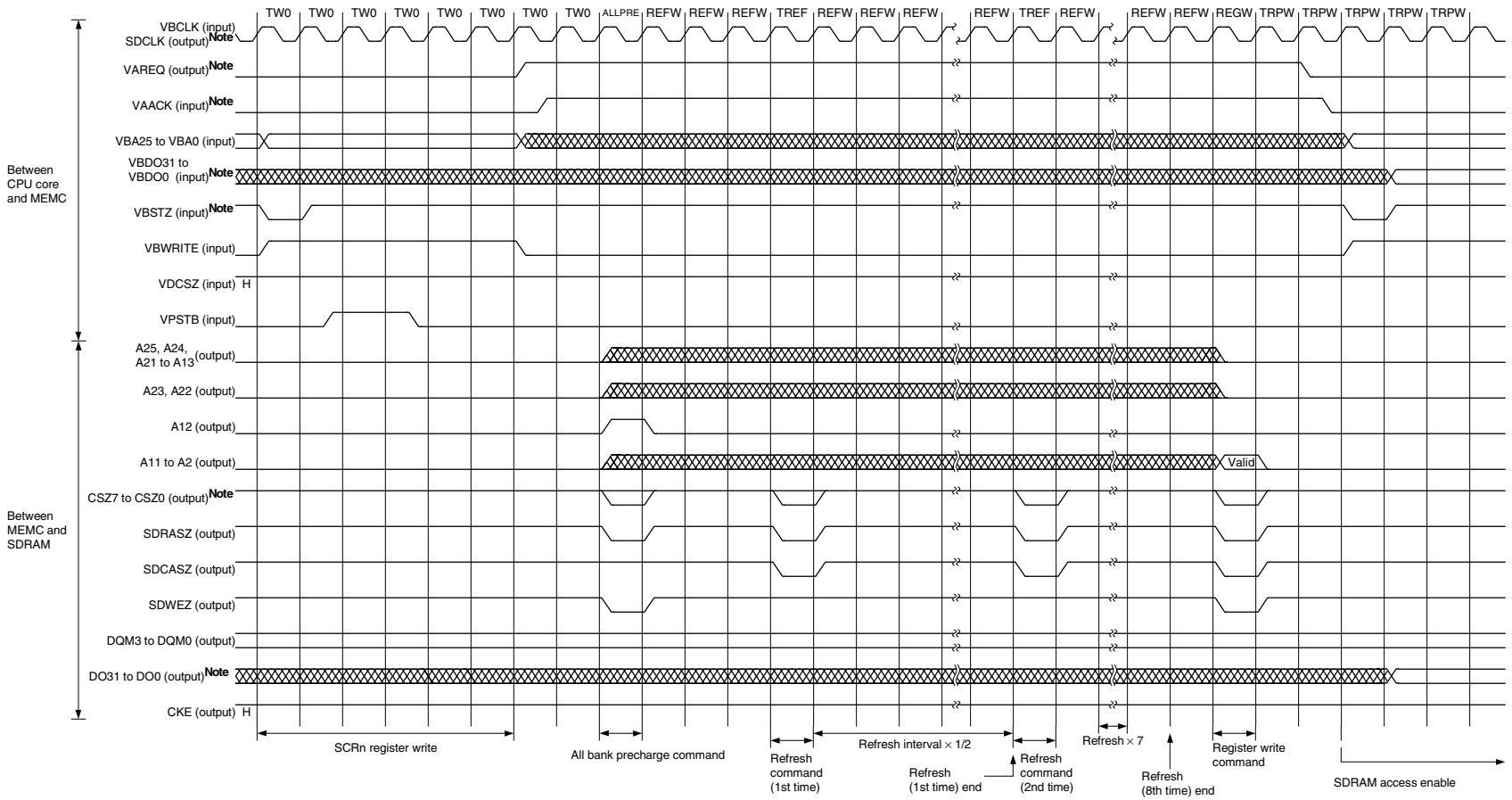
2. ⨯⨯⨯: Unknown state (output) or any level (input).

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

4. BCW: Wait state set by the BCW1 and BCW0 bits of the SCRn register (n = 7 to 0)

5. The address/bank address output upon a bank precharge command is the address/bank address accessed last.

Figure 2-8. SDRAM Register Write Operation Timing

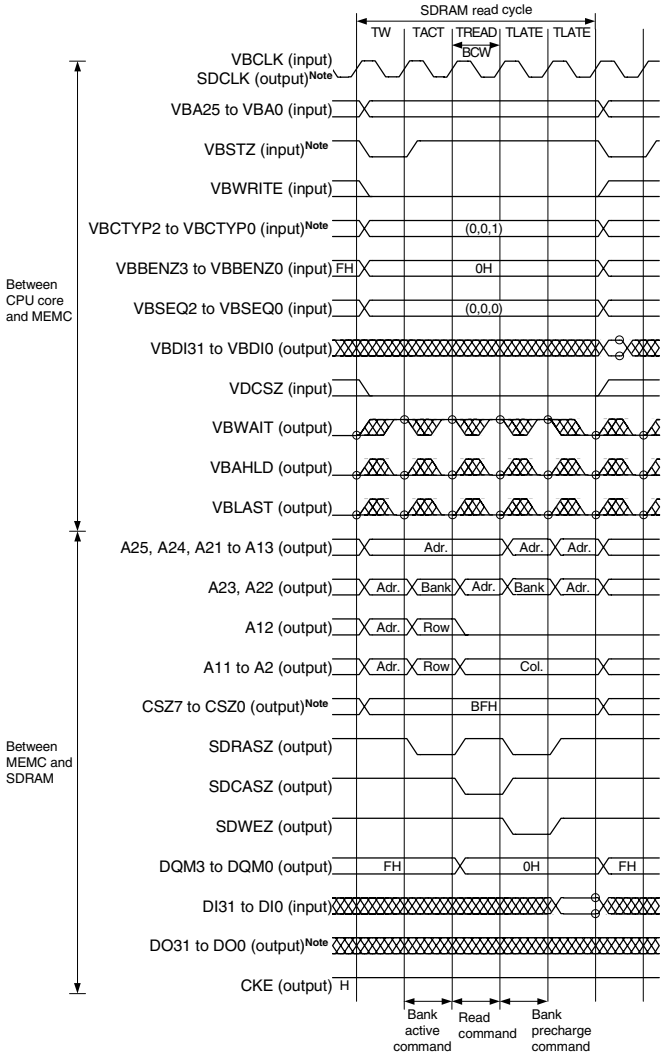


Note NT85E500 signal

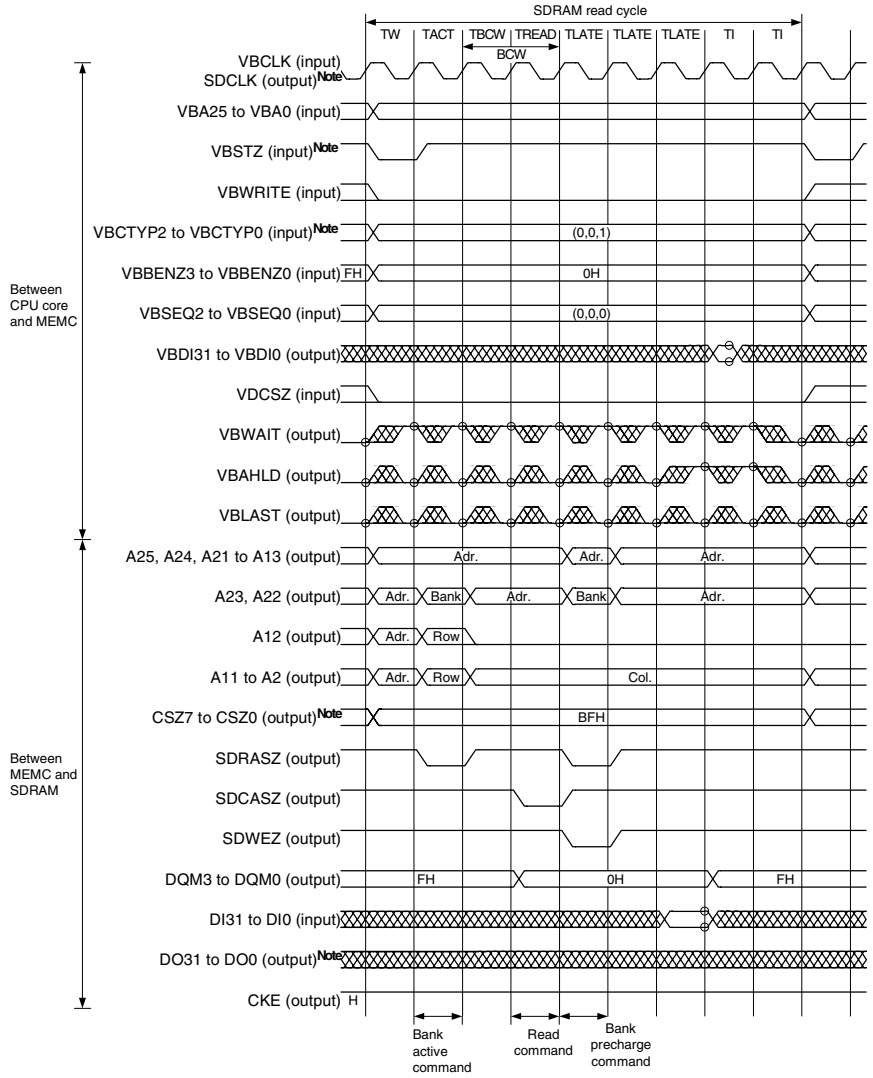
Remark Refresh interval × 1/2: Half period of the refresh interval set by the RFSn register (n = 7 to 0)

Figure 2-9. SDRAM Single Read Cycle (32-Bit Data Bus, Word Access) (1/2)

(a) Off-page, bank change, CAS latency = 2, BCW = 1



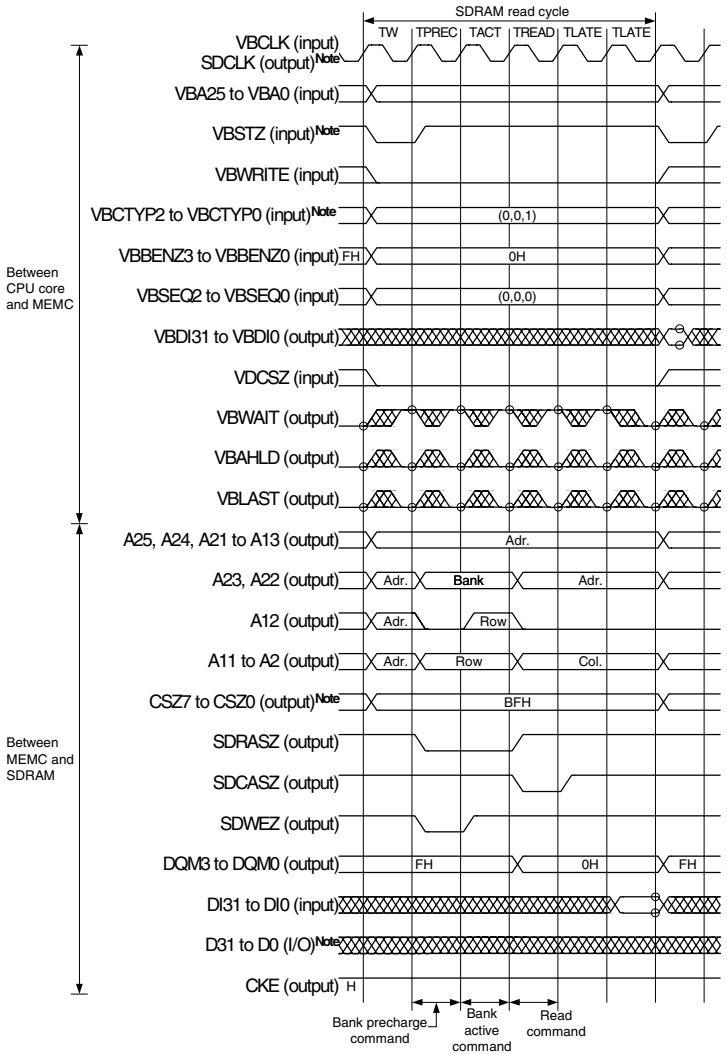
(b) Off-page, bank change, CAS latency = 3, BCW = 2, idle state = 2



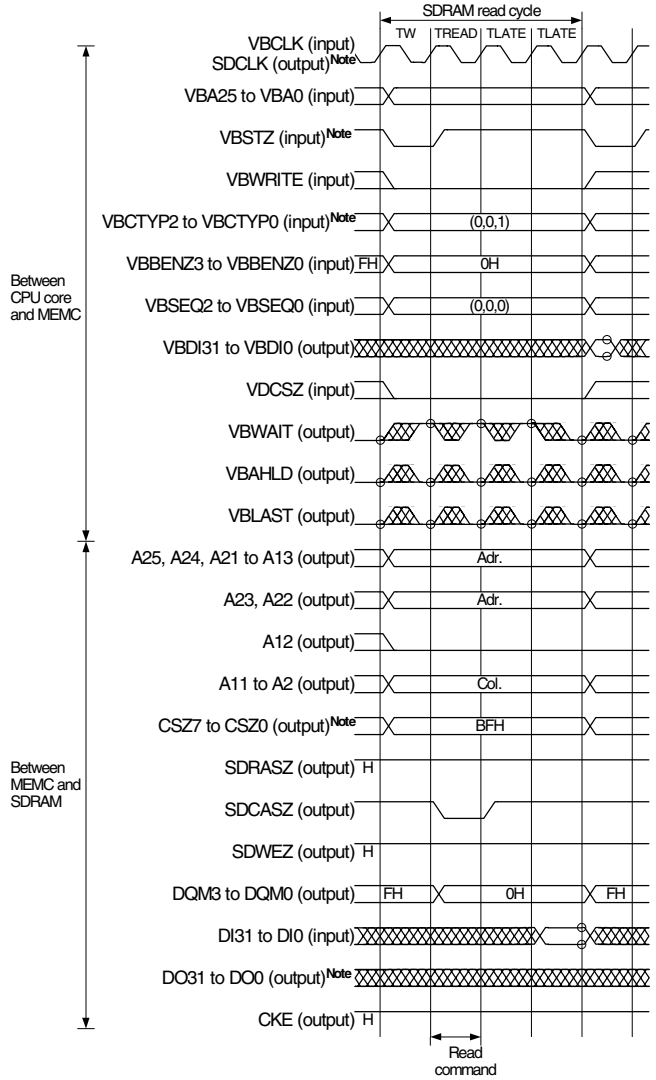
Note NT85E500 signal

Figure 2-9. SDRAM Single Read Cycle (32-Bit Data Bus, Word Access) (2/2)

(c) Off-page, page change



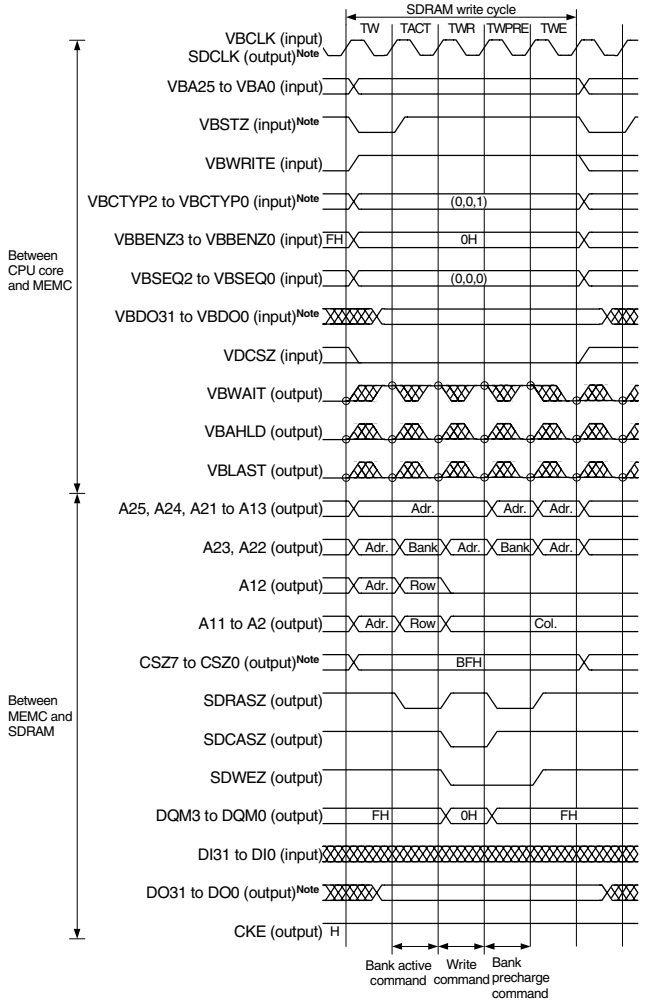
(d) On-page, CAS latency = 2



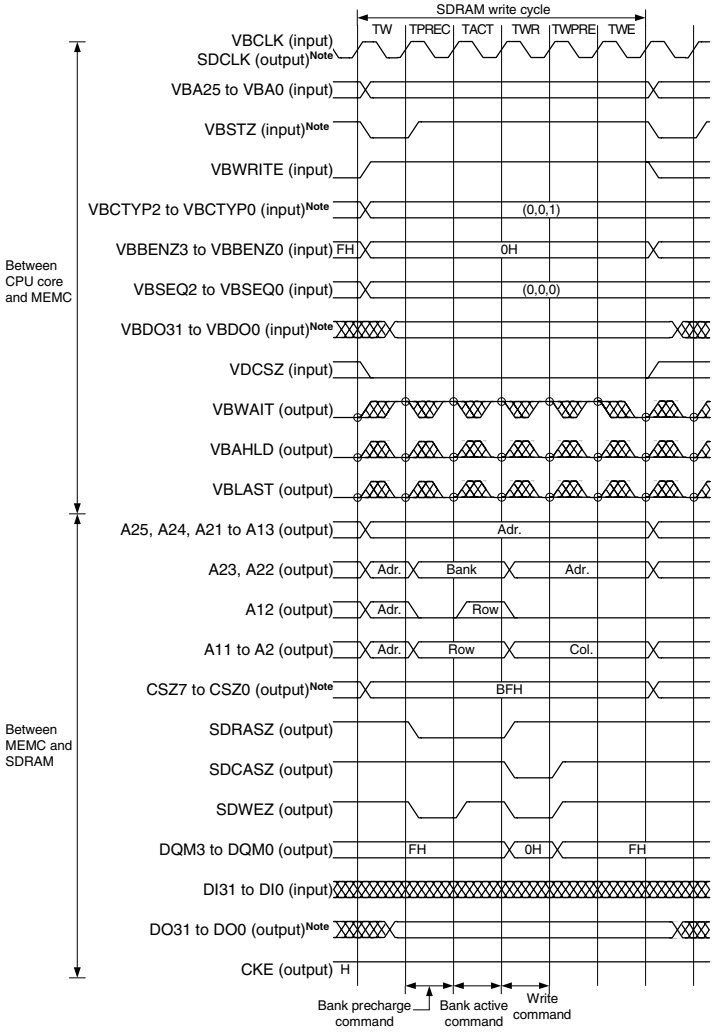
Note NT85E500 signal

Figure 2-10. SDRAM Single Write Cycle (32-Bit Data Bus, Word Access) (1/2)

(a) Off-page, bank change



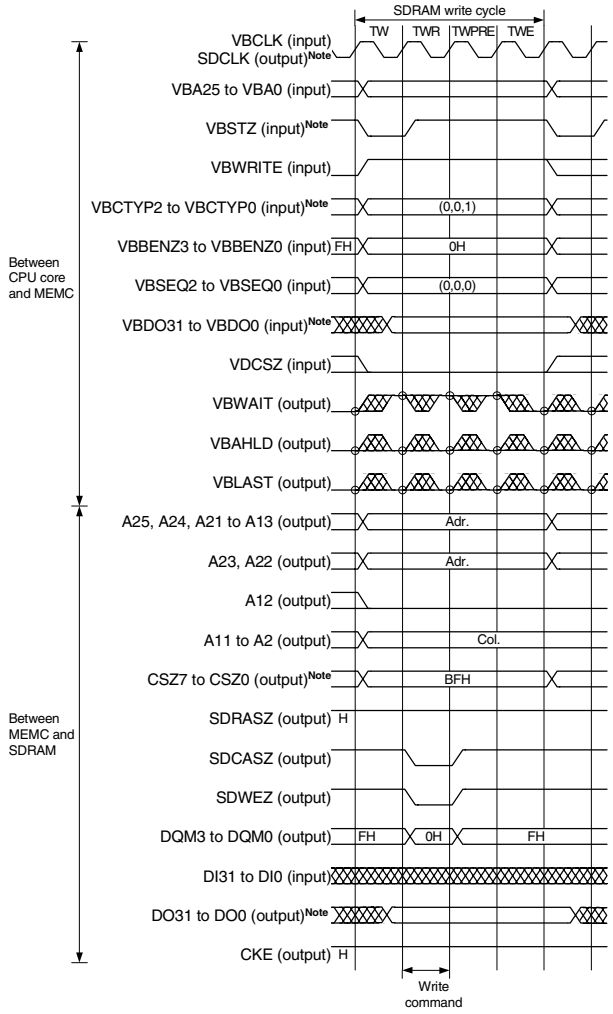
(b) Off-page, page change



Note NT85E500 signal

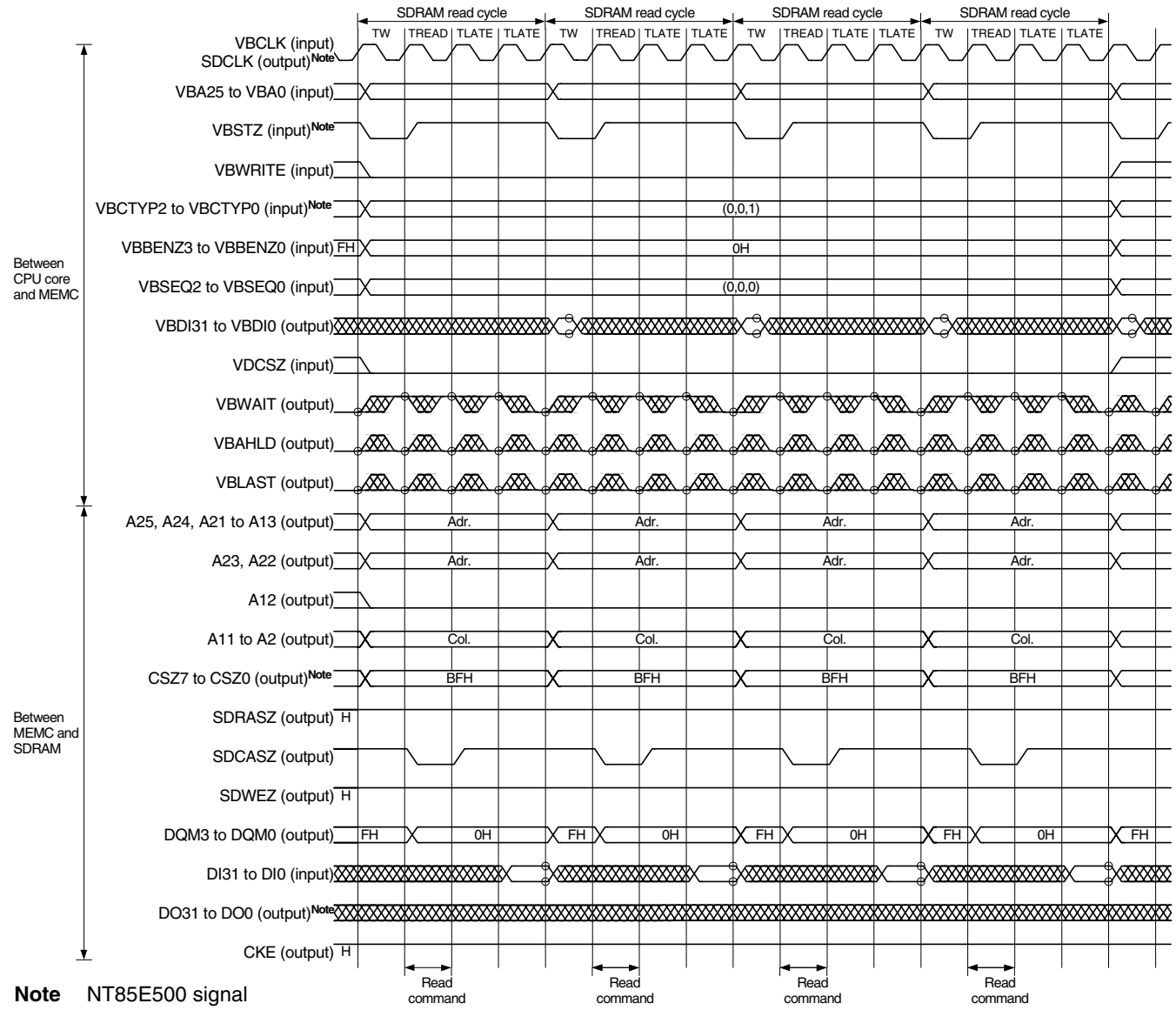
Figure 2-10. SDRAM Single Write Cycle (32-Bit Data Bus, Word Access) (2/2)

(c) On-page



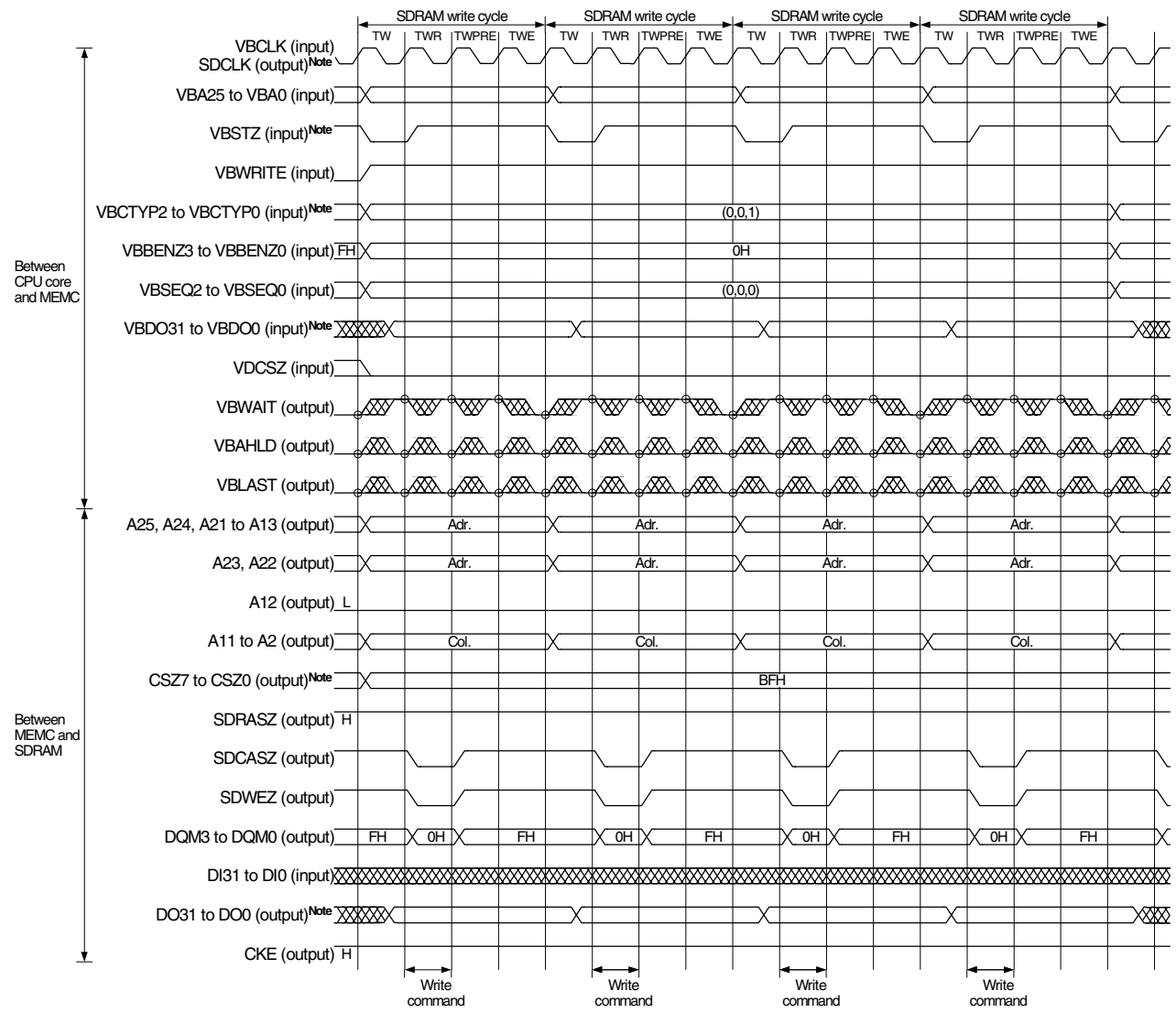
Note NT85E500 signal

Figure 2-11. SDRAM Continuous Read Cycle (32-Bit Data Bus, Word Access, On-Page)



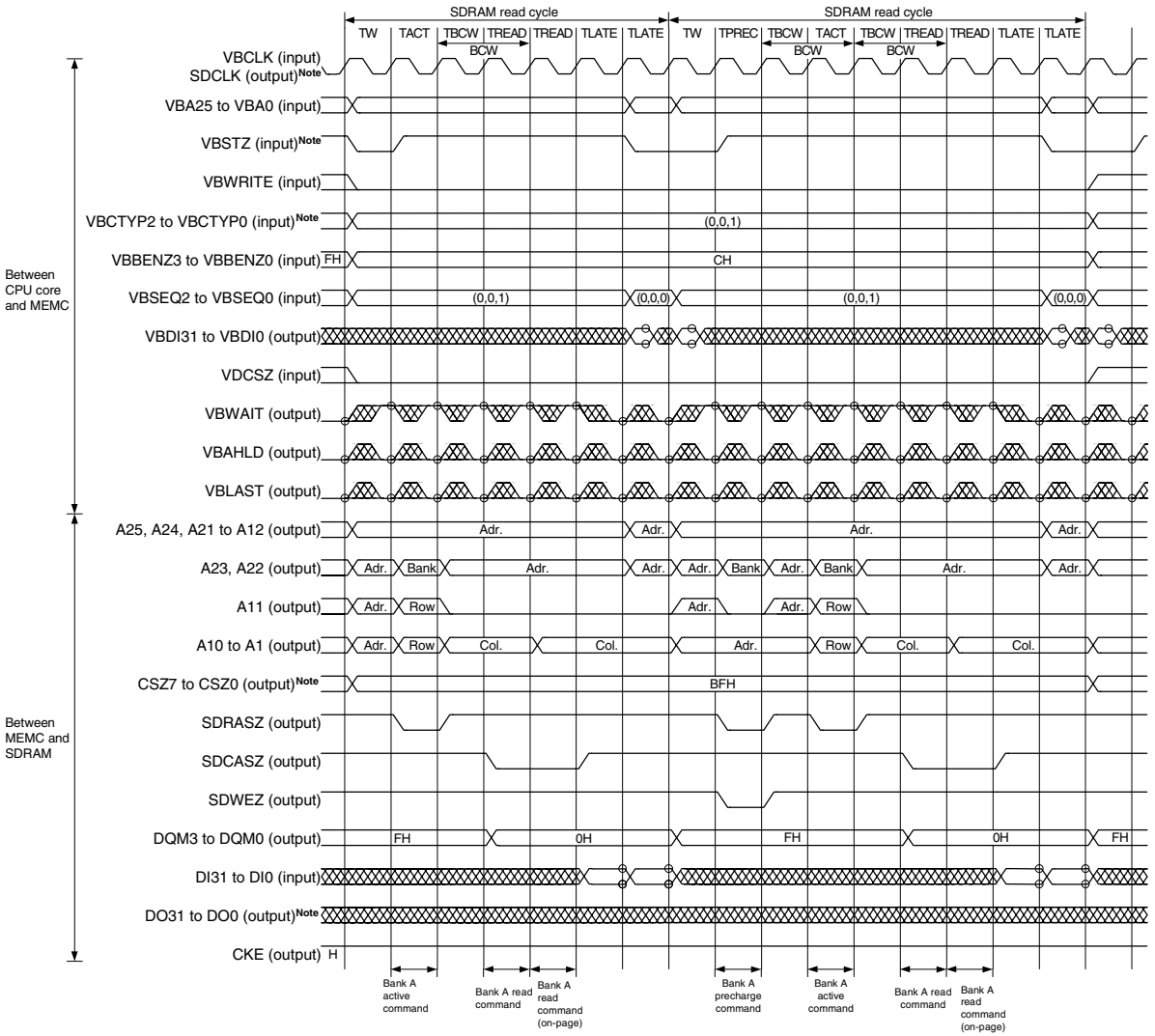
Note NT85E500 signal

Figure 2-12. SDRAM Continuous Write Cycle (32-Bit Data Bus, Word Access, On-Page)



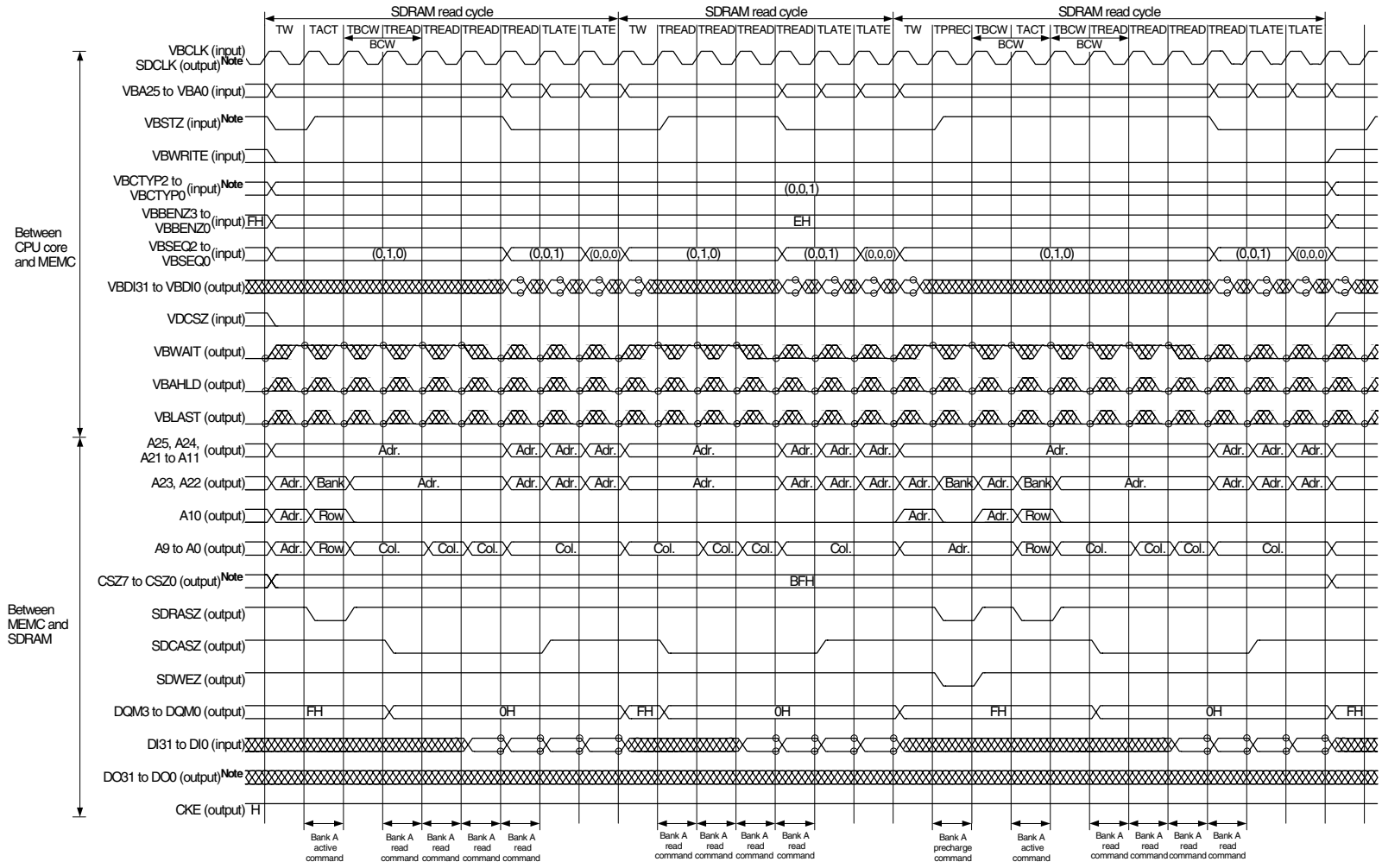
Note NT85E500 signal

Figure 2-13. SDRAM Sequential Read Cycle (16-Bit Data Bus, Word Access, Page Change, CAS Latency = 2, BCW = 2)



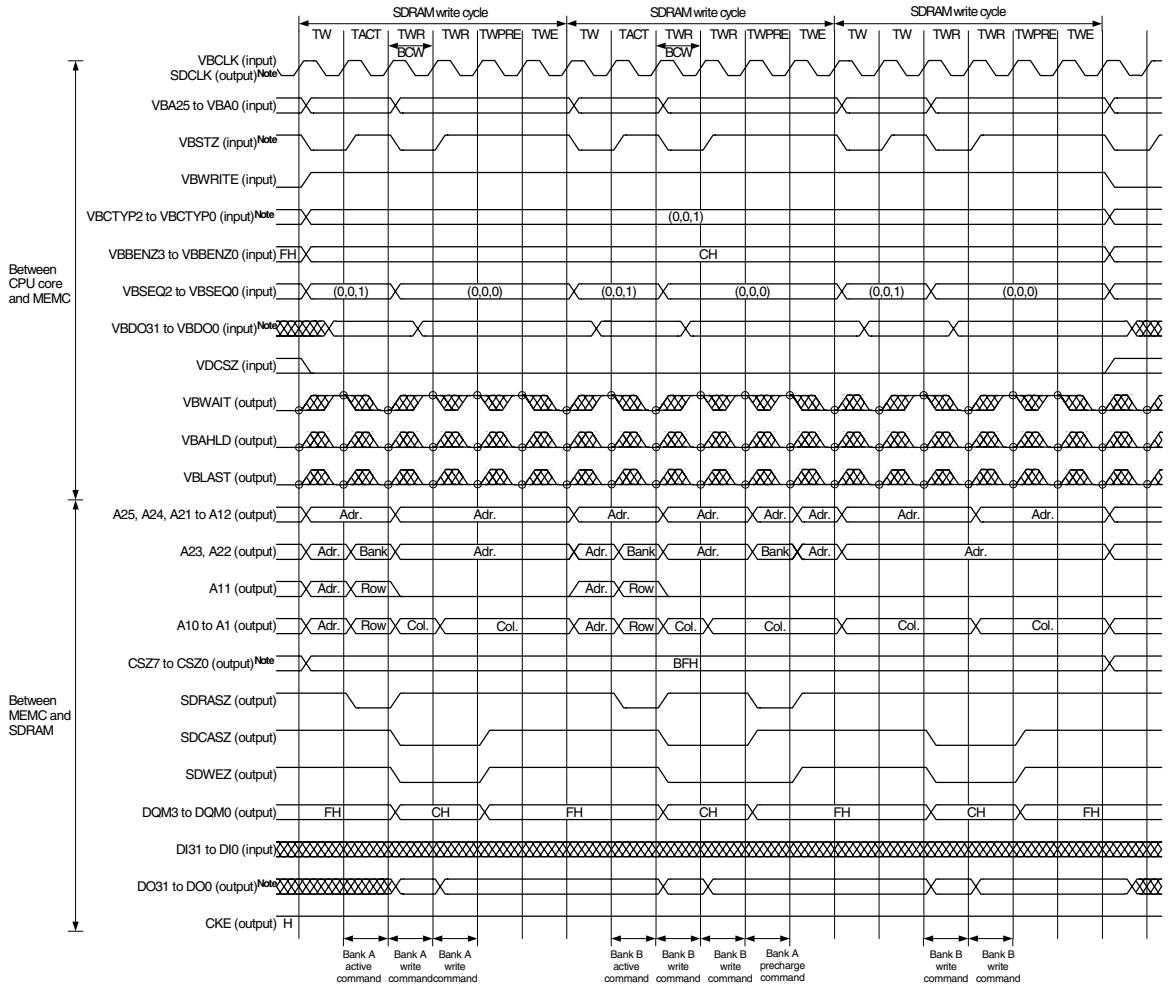
Note NT85E500 signal

Figure 2-14. SDRAM Sequential Read Cycle (8-Bit Data Bus, Word Access, Page Change, CAS Latency = 2, BCW = 2)



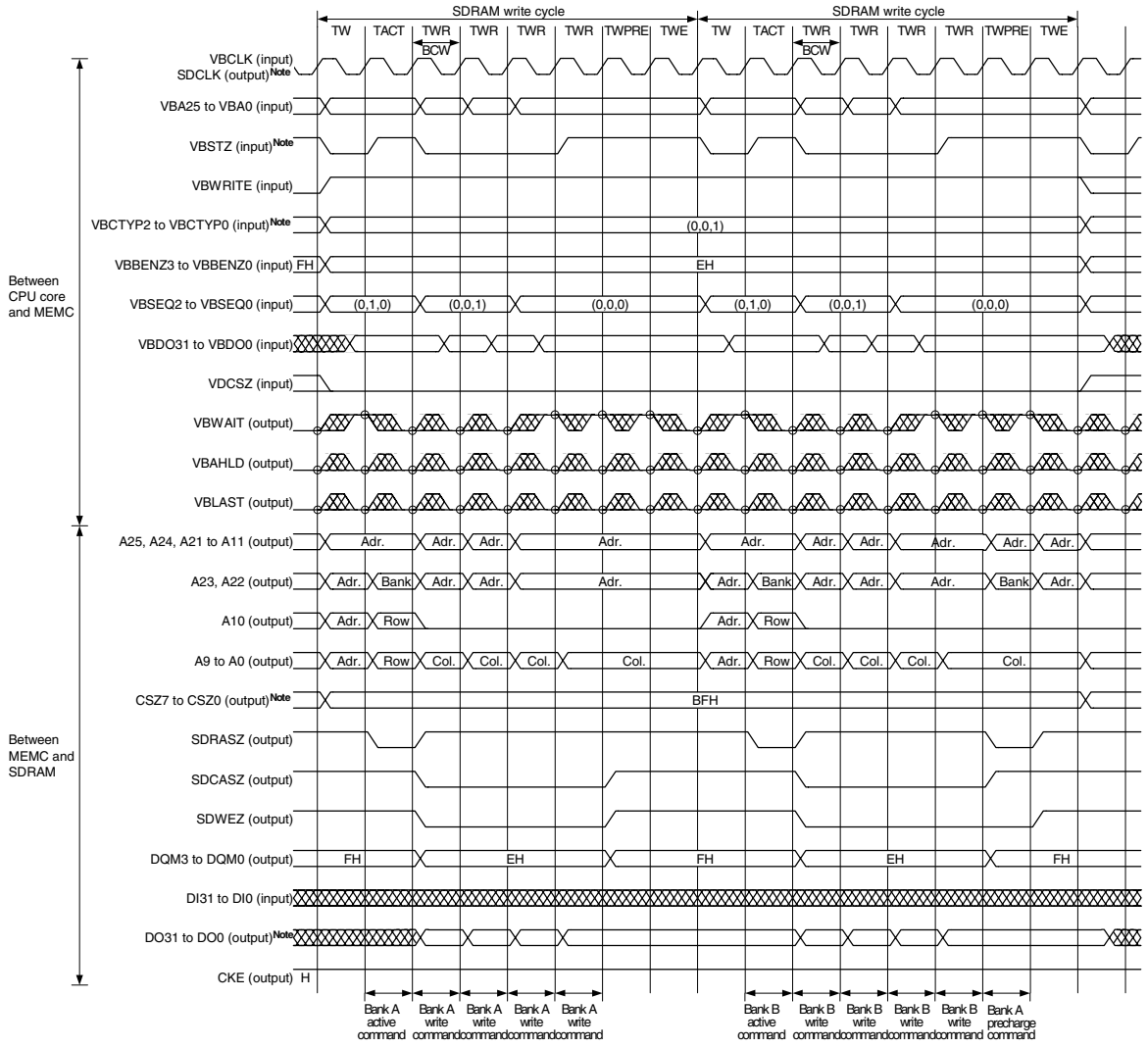
Note NT85E500 signal

Figure 2-15. SDRAM Sequential Write Cycle (16-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)



Note NT85E500 signal

Figure 2-16. SDRAM Sequential Write Cycle (8-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)



Note NT85E500 signal

2.3.3 SDRAM refresh control register n (RFSn)

It is possible to generate an SDRAM CBR refresh cycle and a self-refresh cycle in the NT85E502. Refresh enable and the refresh interval are set by this register.

When more than one NT85E502 is incorporated in the system, settings can be made for each CSn area (n = 7 to 0).

This register can be read or written in 16-bit units.

Remarks 1. n of the register name corresponds to the CSn area number.

2. The address decoder is in the NT85E500. For the addresses of each CSn area, refer to the **NU85E Hardware User's Manual (A14874E)**.

Figure 2-17. SDRAM Refresh Control Register n (RFSn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
RFSn	REN	0	0	0	0	0	RCC1	RCC0	0	0	RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	FFFFF4A2H + 4n	0000H

Bit position	Bit name	Description
15	REN	Sets refresh enable.

REN	Refresh setting
0	Refresh disabled
1	Refresh enabled

Bit position	Bit name	Description
9, 8	RCC1, RCC0	Set the source clock factor for the refresh interval counter.

RCC1	RCC0	Count source clock factor (Cfac)
0	0	32
0	1	128
1	0	256
1	1	Setting prohibited

Remark Refresh count clock (Trcy) = Cfac/ϕ

ϕ: Internal system clock (VBCLK)

Remark n = 7 to 0

Figure 2-17. SDRAM Refresh Control Register n (RFSn) (2/2)

Bit position	Bit name	Description
5 to 0	RIN5 to RIN0	Set the refresh interval factor.

RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	Interval factor (Ifac)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

Caution To change the settings of the RFSn register, follow the procedure below (n = 7 to 0).

<1> Clear (0) the REN bit.

<2> Set the new values to the RCC1, RCC0 and RIN5 to RIN0 bits and set (1) the REN bit. In addition, when changing the refresh interval, set a value that allows a refresh to be performed in time during the interval change.

Table 2-6. Examples of SDRAM Refresh Intervals

Refresh Interval Prescribed Value (μs)	Refresh Count Clock (Trcy)	Interval Factor (Ifac)[Note]			
		When ϕ = 20 MHz	When ϕ = 33 MHz	When ϕ = 50 MHz	When ϕ = 66 MHz
15.6	32/ϕ	9 (14.4)	16 (15.5)	24 (15.4)	32 (15.5)
	128/ϕ	2 (12.8)	4 (15.5)	6 (15.4)	8 (15.5)
	256/ϕ	1 (12.8)	2 (15.5)	3 (15.4)	4 (15.5)

Note Values in parentheses indicate the calculated refresh interval values (μs).
Refresh interval (μs) = Trcy $\times$ Ifac

Remark ϕ : Internal system clock (VBCLK)

2.3.4 CBR refresh function

The NT85E502 activates a CBR refresh cycle for every refresh interval set to the RFSn register (n = 7 to 0).

(1) CBR refresh flow

<1> When a refresh request is generated from the settings of the RFSn register, a CBR refresh request is sent to the NT85E500 from the NT85E502.
<2> The NT85E500 outputs the VSB mastership request signal (VAREQ) to the NU85EA.
<3> An acknowledge signal (VAACK) for the VAREQ signal is returned from the NU85EA to the NT85E500.
<4> When the VAACK signal is received, the NT85E500 activates the REFRQZ signal from the rising edge of the VBCLK signal, and starts a CBR refresh.

(2) CBR refresh timing

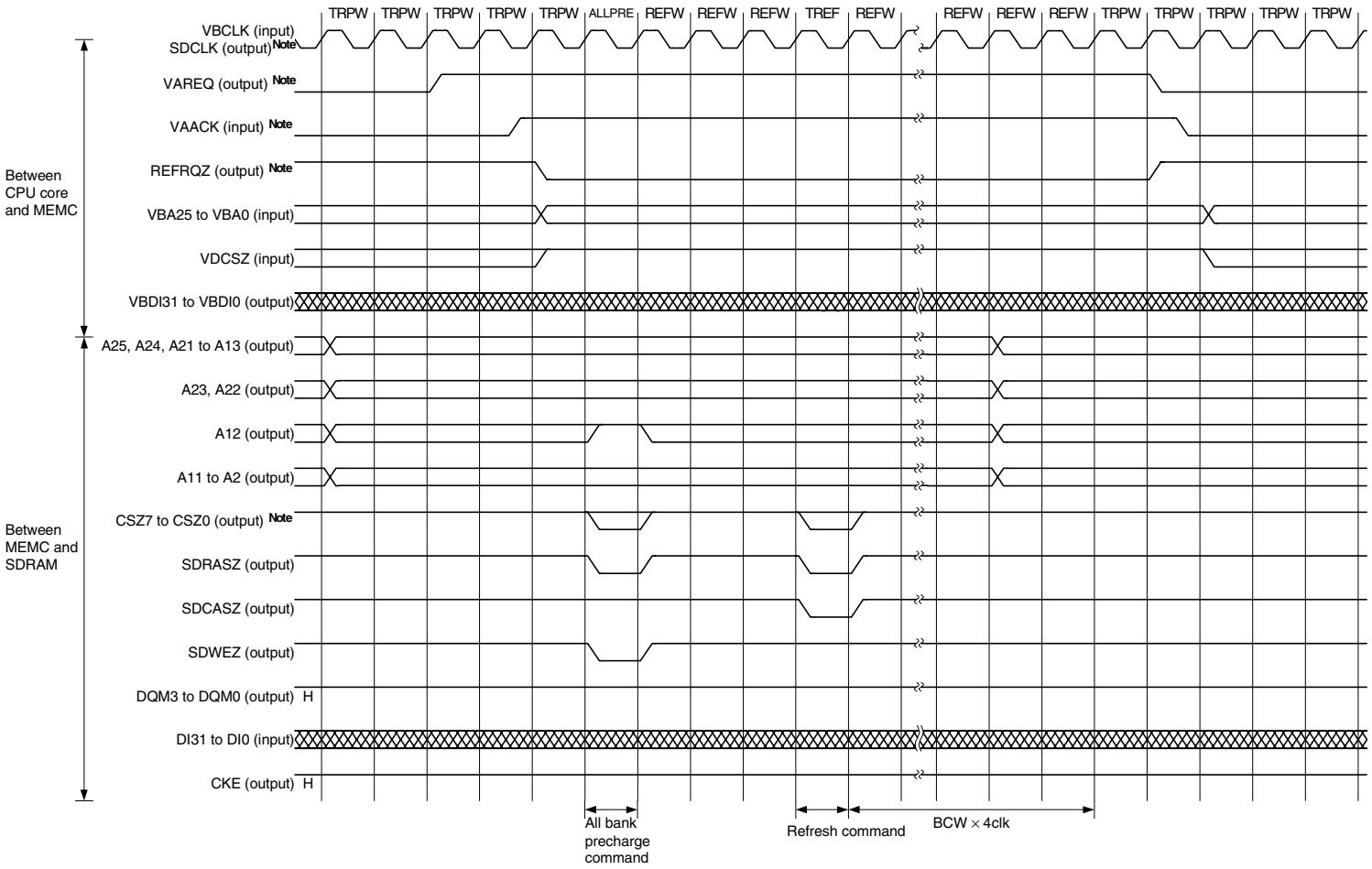
An example of CBR refresh timing is shown below.

Remarks 1. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

2. ⨯⨯⨯ : Unknown state (output) or any level (input).

3. BCW × 4clk: The number of wait states set by the BCW1 and BCW0 bits of the SCRn register × a 4-clock wait are inserted (n = 7 to 0).

Figure 2-18. SDRAM CBR Refresh Timing



Note NT85E500 signal

2.3.5 Self-refresh function

If either the NU85EA undergoes a transition to STOP mode, or the SELFREF signal of the NT85E500 becomes active, the NT85E500 becomes the VSB bus master and the external SDRAM self-refresh cycle is started.

(1) Self-refresh flow

<1> Either a STOP mode request signal (STPRQ) is input to the NT85E500 from the NU85EA, or a self-refresh request signal (SELFREF) is input to the NT85E500 from outside the NT85E500.
<2> The NT85E500 outputs a VSB mastership request signal (VAREQ) to the NU85EA.
<3> The NU85EA returns an acknowledge signal for the VAREQ signal (VAACK) to the NT85E500.
<4> After receiving the VAACK signal, the NT85E500 activates the REFRQZ signal from the rising edge of the next VBCLK signal, and starts a self-refresh.
<5> Transition into the self-refresh status in the entire SDRAM is completed.
<6> The NT85E500 returns an acknowledge signal for the STPRQ signal (STPAK) to the NU85EA.
<7> The STPRQ signal becomes inactive.
<8> Suspension of self-refresh begins.
<9> Suspension of self-refresh in the entire SDRAM is completed.
<10> The VAREQ signal becomes inactive.
<11> Normal status resumes.

(2) Self-refresh timing

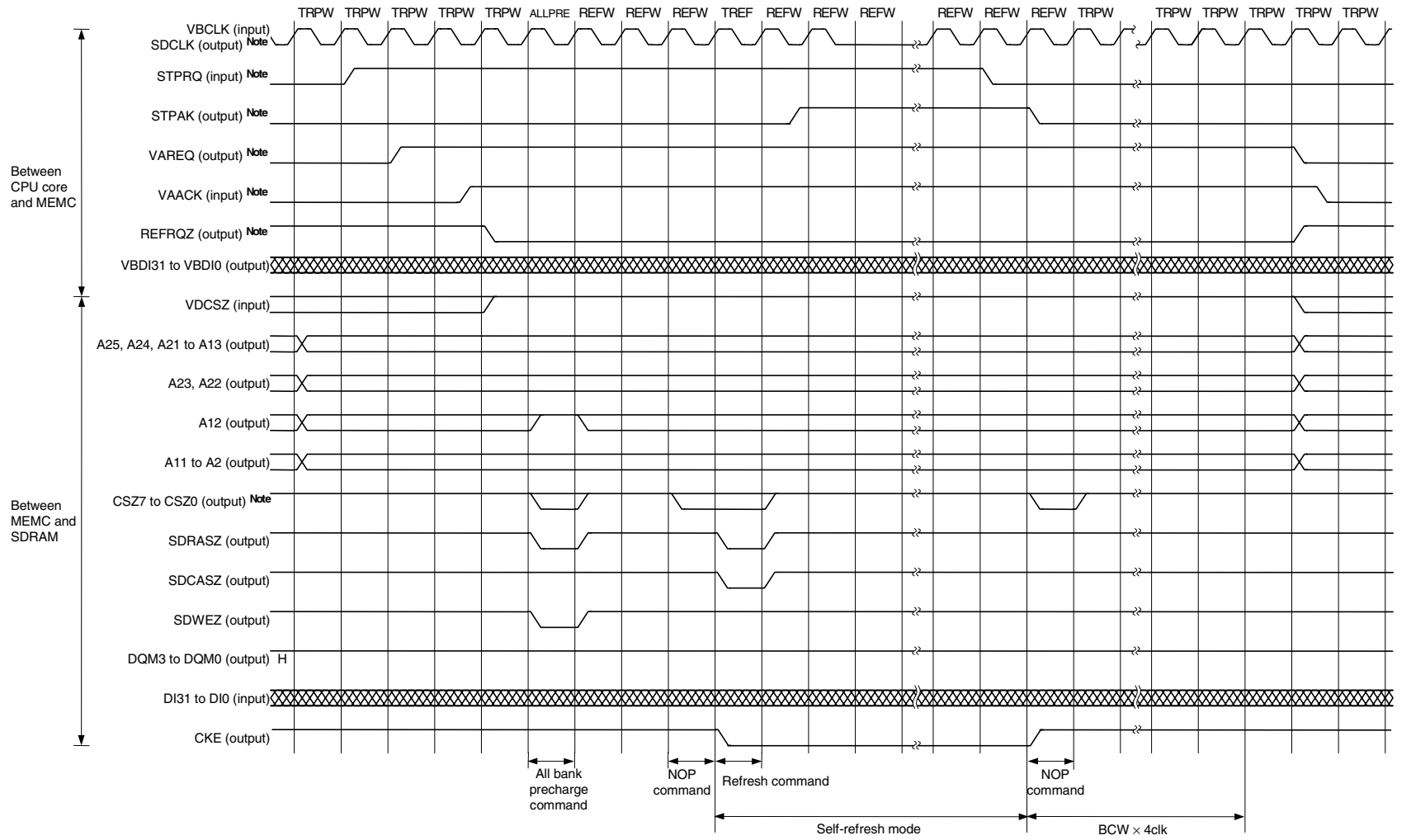
An example of self-refresh timing is shown below.

Remarks 1. For details of VSB signals (VBxxx, VDxxx), refer to the **NU85E Hardware User's Manual (A14874E)**.

2. XXX: Unknown state (output) or any level (input).

3. BCW × 4clk: The number of wait states set by the BCW1 and BCW0 bits of the SCRn register × a 4-clock wait are inserted (n = 7 to 0).

Figure 2-19. SDRAM Self-Refresh Timing



Note NT85E500 signal

2.3.6 Notes on refresh function

The SDRAM refresh is not always performed in the interval set by the RFSn register.

If a refresh request is generated in the case below, the bus cycle ends and the refresh request is held pending until the NT85E500 secures bus mastership.

(1) When the NU85EA operates as the bus master and the VSB bus cycle is generated

The following cases:

- While memory instruction fetch and data access (including NPB access) are being performed from the NU85EA via the VSB.
- During DMA transfer using the VSB (held pending until the current DMA transfer ends in the case of single transfer, single-step transfer, and block transfer. In line transfer, held pending until the one line (four transfers) ends (see **Figure 2-20**)).
- During instruction cache and data cache refill (held pending until one-line refill (four words) ends when a miss-hit has been generated and one-line refill is performed from memory to the VSB. In the case of an instruction auto-fill, held pending until the one-line (four words) refill ends (since the VMLOCK signal of the NU85EA becomes inactive, bus can be released every one line, so the refresh request can be acknowledged)).

(2) In a bus hold state set by an external bus master

If a bus hold request and a refresh request conflict, the bus hold request takes precedence. When a refresh request is generated during a bus hold, the REFRQZ signal of the NT85E500 becomes active and refresh request generation notification can be sent to the external bus master. To shift to the refresh cycle, cancel the bus hold request using this signal. If no external devices can be the bus master and the HLDRQZ pin is fixed to high-level input, the bus hold request is not generated. So, in that case, it is not necessary to consider conflict with a bus hold.

Figure 2-20. Refresh Timing During DMA Line Transfer

Notes 1. NU85EA signal

2. NT85E500 signal

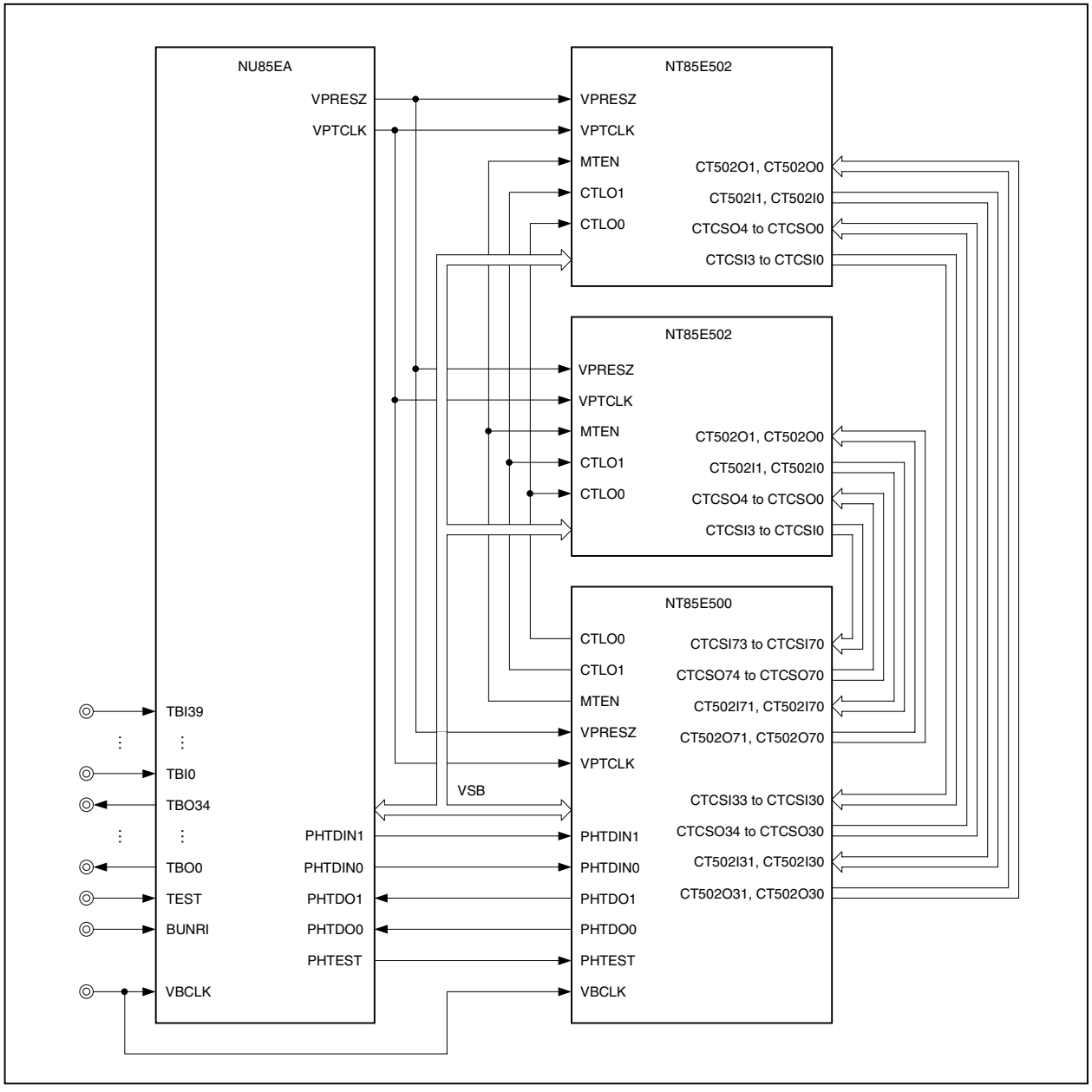
3. ORed signals of the NT85E500 and NT85E502.

2.4 Test Function

The NT85E502 can be tested using the NU85EA test mode.

To test the NT85E502, connect it to the NU85EA as follows (the NT85E502 is connected to the CS7 and CS3 areas).

Figure 2-21. Connection of NT85E502 to NU85EA in Test Mode



Remark For details about test modes, refer to the **NU85E Hardware User's Manual (A14874E)**.

2.4.1 Pin processing when in test mode

(1) External memory connection pins

These operate the same in test mode as in normal mode. Refer to **2.2.4 Pin status** regarding the pin status. Input pins (DI31 to DI0) are ignored regardless of the values that are input.

(2) Test mode pins

Connect test mode pins to the NU85EA as shown in Figure 2-21.

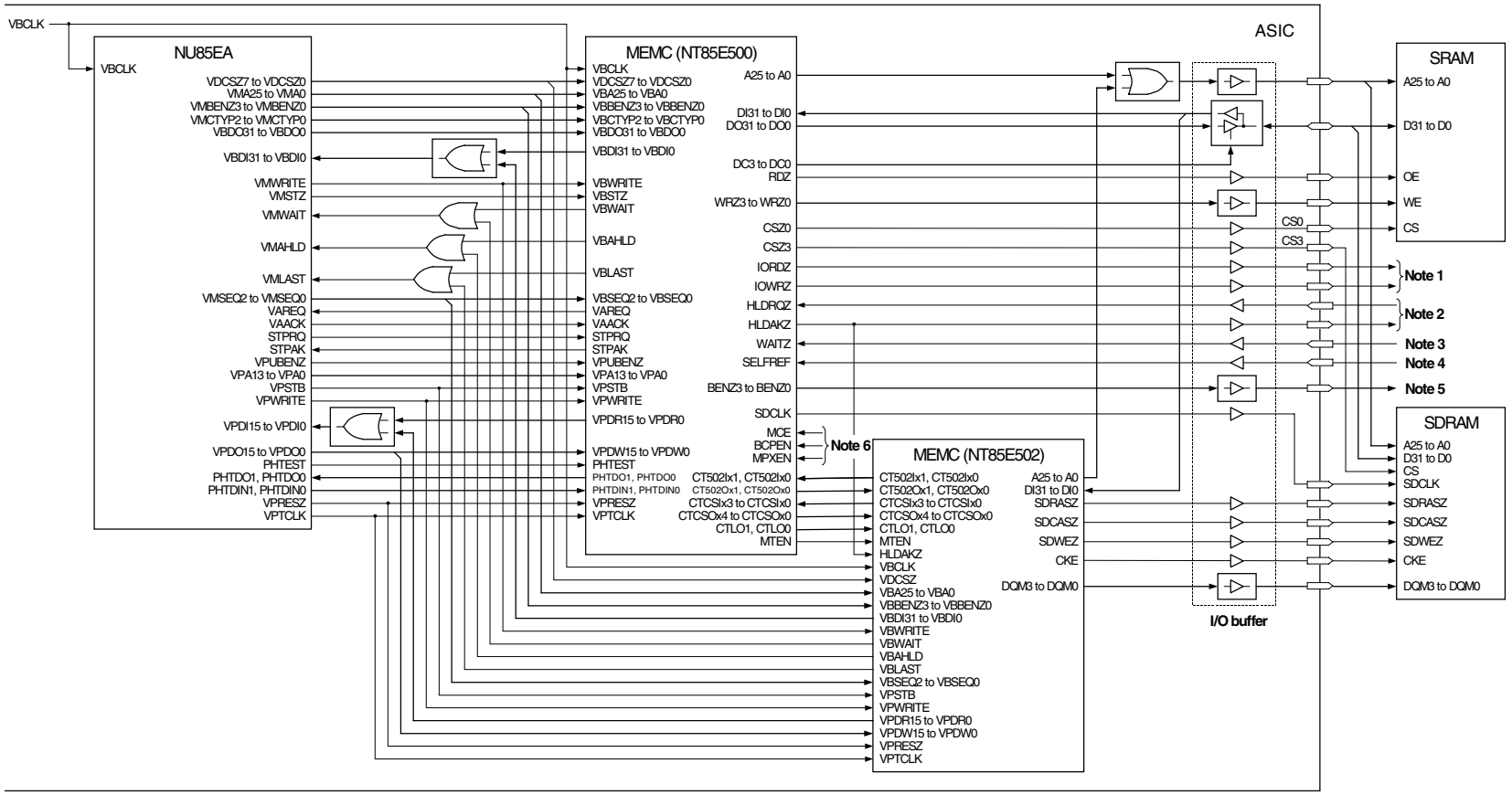
(3) Other pins

Make other pins the same as in normal mode. Refer to **2.2.4 Pin status** regarding the pin status.

APPENDIX A CONNECTION EXAMPLE

An example of the connection of the NU85EA, MEMCs (NT85E500 and NT85E502), and external memories (SRAM and SDRAM) is shown below.

Figure A-1. Connection Example of NU85EA, MEMCs and External Memories (SRAM and SDRAM)



Notes 1. Used for DMA flyby transfer

2. Used for bus hold cycle

3. Used for external wait control

Notes 4. Used for self-refresh request

5. Used when memory with a byte enable control function is connected

6. Used for initial value settings

APPENDIX B INDEX

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APPENDIX C REVISION HISTORY

A history of the revisions up to this edition is shown below. The page in the “Page” column indicates the page in the previous edition.

(1) 1st → 2nd edition

(1/2)

Page	Contents
p.16	Addition of **Note** to **1.1.1 (1) SRAM-and-I/O controller**
p.16	Modification of **1.1.1 (2) Page ROM controller**
p.19	Modification of **1.1.3 (c) Bus arbitration controller**
p.27	Modification of **1.2.2 (1) (n) VBAHLD**
p.27	Modification of **1.2.2 (1) (o) VBLAST**
p.28	Modification of **1.2.2 (1) (v) VPDV**
p.33	Modification of **1.2.3 Recommended connection of unused pins**
p.34	Modification of **Table 1-4 Pin Status in Each Operating Mode**
p.37	Modification of **Caution** in **Figure 1-3 Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)**
p.41	Addition of description to **1.3.4 (1) External wait function**
p.41	Addition of description and figure to **1.3.4 (2) Data wait control registers and external waits**
p.45	Modification of **Figure 1-9 SRAM Write Timing**
p.56	Modification of **Figure 1-17 Page ROM Read Timing**
p.58	Modification of **1.3.8 (1) Bus hold procedure**
p.58	Modification of **1.3.8 (2) Bus hold release procedure**
p.60	Addition of **Caution** to **1.3.9 Bus cycle period control register (BCP)**
p.80	Addition of **Remark** to **2.1 Outline**
p.81	Modification of **2.1.1 Features**
p.89	Modification of **2.2.2 (1) (i) VBAHLD**
p.90	Modification of **2.2.2 (1) (j) VBLAST**
p.90	Modification of **2.2.2 (1) (m) VPDV**
p.91	Modification of **2.2.2 (3) (g) DQM3 to DQM0**
p.92	Modification of **Table 2-3 Pin Status in Each Operating Mode**
p.94	Modification of **Caution 1** in **2.3.1 SDRAM configuration register n (SCRn)**
p.95	Modification of **Figure 2-4 SDRAM Configuration Register n (SCRn)**
pp.97 to 100	Addition of **(1) Address output and SDRAM connection** and **(2) Bank address output** to **2.3.1 SDRAM configuration register n (SCRn)**
p.101	Modification of **Figure 2-5 64 Mb SDRAM Connection Example**
p.104	Addition of **Remark 5** to **2.3.2 (2) Bus timing**
p.106	Modification of **Figure 2-9 SDRAM Single Read Cycle (32-Bit Data Bus, Word Access)**
pp.108, 109	Modification of **Figure 2-10 SDRAM Single Write Cycle (32-Bit Data Bus, Word Access)**
p.114	Modification of **Figure 2-15 SDRAM Sequential Write Cycle (16-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)**

(2/2)

Page	Contents
p.115	Modification of **Figure 2-16 SDRAM Sequential Write Cycle (8-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)**
p.117	Modification of **Figure 2-17 SDRAM Refresh Control Register n (RFSn)**
p.118	Addition of **2.3.4 CBR refresh function**
p.119	Modification of **Figure 2-18 SDRAM CBR Refresh Timing**
p.120	Modification of **2.3.5 (1) Self-refresh flow**
p.121	Modification of **Figure 2-19 SDRAM Self-Refresh Timing**
p.122	Addition of **2.3.6 Notes on refresh function**
p.123	Addition of **Figure 2-20 Refresh Timing During DMA Line Transfer**
p.124	Modification of **Figure 2-21 Connection of NT85E502 to NU85E in Test Mode**

[MEMO]

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