RHF310

Rad-hard 400 µA high-speed operational amplifier

Preliminary data

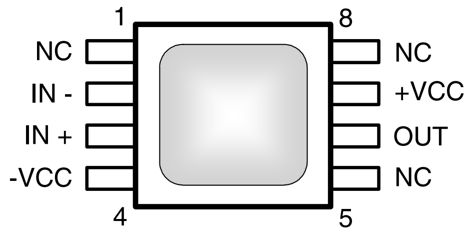
Features

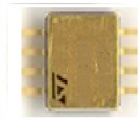
- OptimWatt™ device featuring ultra-low 2 mW consumption and low 400 µA quiescent current[(a)]
- Bandwidth: 120 MHz (gain = 2)
- Slew rate: 115 V/µs
- Specified on 1 kΩ
- Input noise: 7.5 nV/√ Hz
- Tested with 5 V power supply
- 300 krad MIL-STD-883 1019.7 ELDRS free compliant
- SEL immune at 125° C, LET up to 110 MEV.cm^2/mg
- SET characterized, LET up to 110 MEV.cm^2/mg
- QMLV qualified under SMD 5962-0723301
- Mass: 0.45 g

Applications

- Low-power, high-speed systems
- Communication and space equipment
- Harsh radiation environments
- ADC drivers

Pin connections
(top view)





The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package.

Description

The RHF310 is a very low power, high-speed operational amplifier. A bandwidth of 120 MHz is achieved while drawing only 400 µA of quiescent current. This low-power characteristic is particularly suitable for high-speed battery powered devices requiring dynamic performance. The RHF310 is a single operator available in a Flat-8 package, saving board space as well as providing excellent thermal performance.

Table 1. Device summary

Order code	SMD pin	Quality level	Package	Lead finish	Marking	EPPL	Packing
RHF310K1	-	Engineering model	Flat-8	Gold	RHF310K1	-	Strip pack
RHF310K-01V	5962F0723301VXC	QMLV-Flight	Flat-8	Gold	5962F0723101VXC	-	

Note: Contact your ST sales office for information on the specific conditions for products in die form and QML-Q versions.

a. OptimWatt™ is an STMIcroelectronics registered trademark that applies to products with specific features that optimize energy efficiency.

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1] (voltage difference between $-V_{CC}$ and $+V_{CC}$ pins)	6	V
V_{id}	Differential input voltage[2]	±0.5	V
V_{in}	Input voltage range[3]	±2.5	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient area	50	°C/W
R_{thjc}	Thermal resistance junction to case	40	°C/W
P_{max}	Maximum power dissipation[4] (at T_{amb} = 25° C) for T_j = 150° C	830	mW
ESD	HBM: human body model [5] pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 2 0.5	kV
	MM: machine model [6] pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 200 60	V
	CDM: charged device model (all pins)[7]	1.5	kV
	Latch-up immunity	200	mA

1. All voltages values are measured with respect to the ground pin.
2. Differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed V_{CC} +0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. This is a minimum value. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 5.5	V
V_{icm}	Common-mode input voltage	$-V_{CC}$ +1.5 V to $+V_{CC}$ -1.5 V	V
T_{amb}	Operating free-air temperature range[1]	-55 to +125	°C

1. Tj must never exceed +150°C. P = (T_j - T_{amb} / R_{thja} = (T_j - T_{case}) / R_{thjc} with P the power that the RHF310 must dissipate in the application.

2 Electrical characteristics

Table 4. Electrical characteristics for V_{CC} = ±2.5 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Input offset voltage		+125°C	-6.5		+6.5	mV
			+25°C	-6.5	1.7	+6.5	
			-55°C	-6.5		+6.5	
I_{ib+}	Non-inverting input bias current		+125°C			15	µA
			+25°C		3.1	12	
			-55°C			15	
I_{ib-}	Inverting input bias current		+125°C			7	µA
			+25°C		0.1	5	
			-55°C			7	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±1 V	+125°C	55			dB
			+25°C	57	61		
			-55°C	55			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{out}$)	ΔV_{CC} = 3.5 V to 5 V	+125°C	50			dB
			+25°C	65	82		
			-55°C	50			
PSRR	Power supply rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{out}$)	ΔV_{CC} = 200 mV_{pp} at 1 kHz	+25°C		50		dB
I_{CC}	Supply current	No load	+125°C			600	µA
			+25°C		400	530	
			-55°C			600	
Dynamic performance and output characteristics							
R_{OL}	Transimpedance	ΔV_{out}= ±1 V, R_L = 1 kΩ	+125°C	500			kΩ
			+25°C	600	1450		
			-55°C	500			
Bw	Small signal -3 dB bandwidth on 1k Ω load	R_{fb} = 3 kΩ, A_V = +1	+25°C		230		MHz
		R_{fb} = 510 Ω, A_V = +10	+25°C		26		
		R_{fb} = 3 kΩ, A_V = +2	+125°C	70			
			+25°C	70	120		
			-55°C	70			
	Gain flatness at 0.1 dB	V_{out} = 20 mV_{pp} A_V = +2, R_L = 1k Ω	+25°C		25		

Table 4. Electrical characteristics for V_{CC} = ±2.5 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
SR	Slew rate	V_{out} = 2 V_{pp}, A_V = +2, R_L = 100 Ω	+25°C		115		V/µs
V_{OH}	High level output voltage	R_L = 100 Ω	+125°C	1.5			V
			+25°C	1.55	1.65		
			-55°C	1.5			
V_{OL}	Low level output voltage	R_L = 100 Ω	+125°C			-1.5	V
			+25°C		-1.66	-1.55	
			-55°C			-1.5	
I_{out}	I_{sink} (1)	Output to GND	+125°C	70			mA
			+25°C	70	110		
			-55°C	70			
	I_{source} (2)	Output to GND	+125°C	60			
			+25°C	60	100		
			-55°C	60			
Noise and distortion							
eN	Equivalent input noise voltage (3)	F = 100 kHz	+25°C		7.5		nV/√ Hz
iN	Equivalent positive input noise current(3)	F = 100 kHz	+25°C		13		pA/√ Hz
	Equivalent negative input noise current(3)	F = 100 kHz	+25°C		6		pA/√ Hz
SFDR	Spurious free dynamic range	A_V = +2, V_{out} = 2 V_{pp}, R_L = 100 Ω	+25°C				dBc
		F = 1 MHz	+25°C		-87		
		F = 10 MHz	+25°C		-55		

1. See *Figure 10* for more details.
2. See *Figure 11* for more details.
3. See *Chapter 5 on page 15*.

Table 5. Closed-loop gain and feedback components

Gain (V/V)	+ 2	- 2	+ 4	- 4	+ 10	- 10
R_{fb} (Ω)	1.2k	1k	150	300	100	180

Figure 1. Frequency response, positive gain

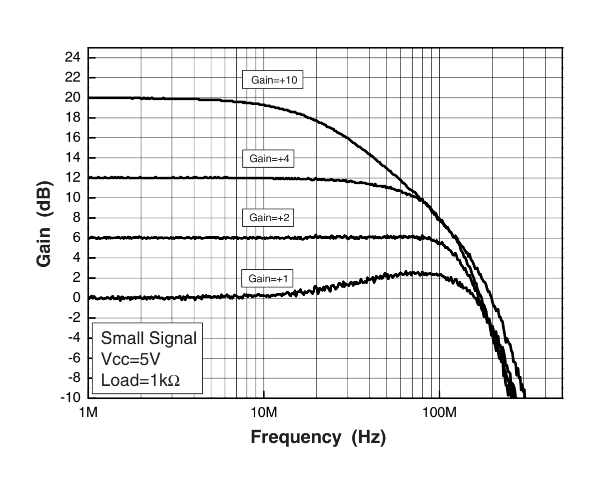


Figure 2. Frequency response vs. capa-load

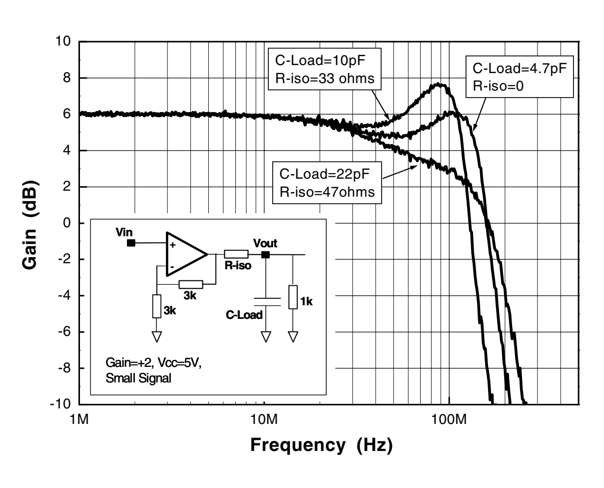


Figure 3. Output amplitude vs. load

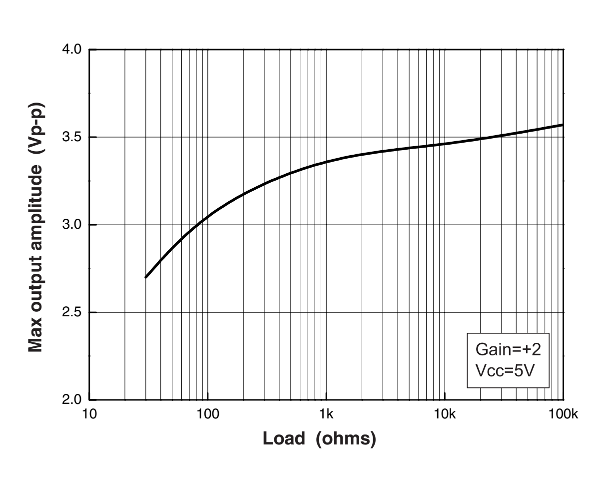


Figure 4. Input voltage noise vs. frequency

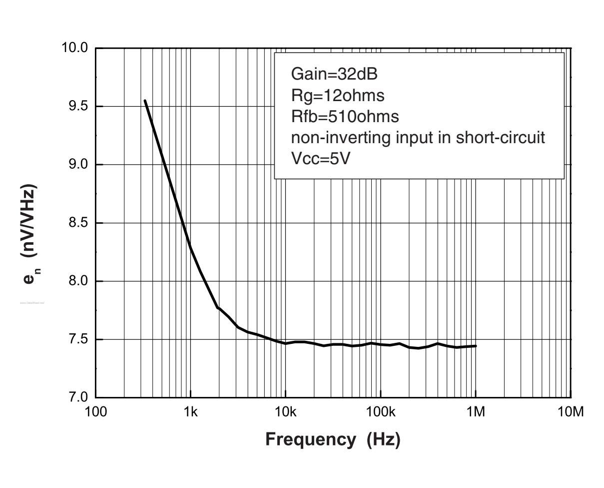


Figure 5. Distortion at 1 MHz

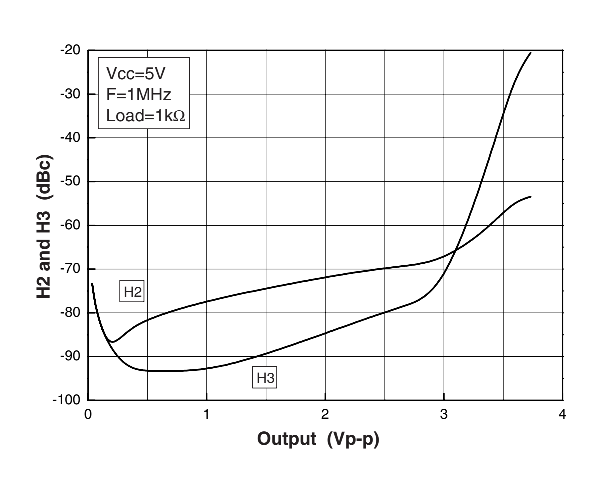


Figure 6. Distortion at 10 MHz

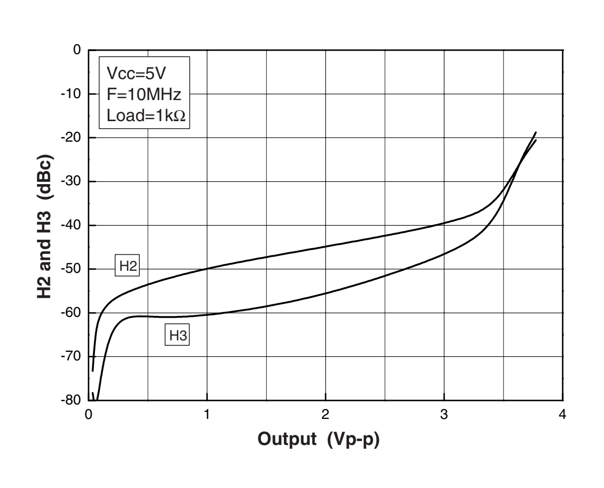


Figure 7. Positive slew rate on 1 kΩ load

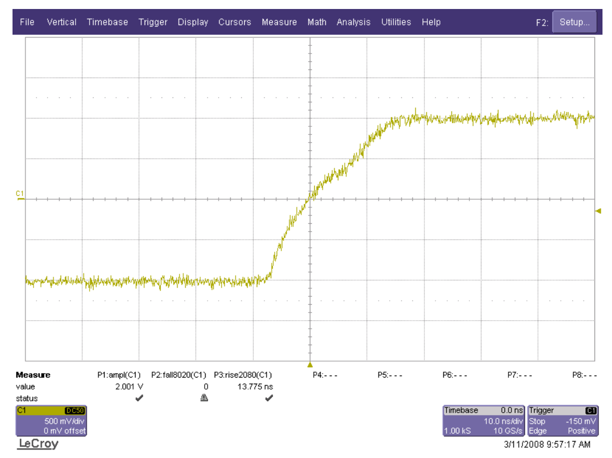


Figure 8. Negative slew rate on 1 kΩ load

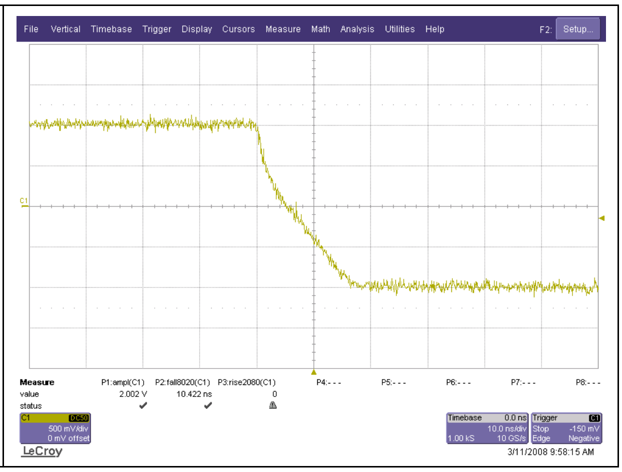


Figure 9. Quiescent current vs. V_{CC}

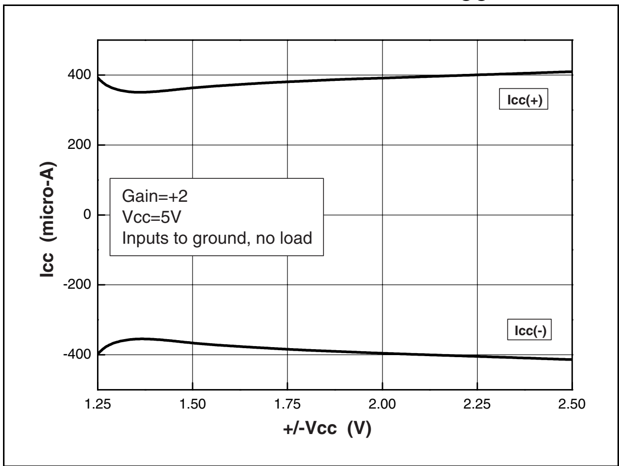


Figure 10. I_{sink}

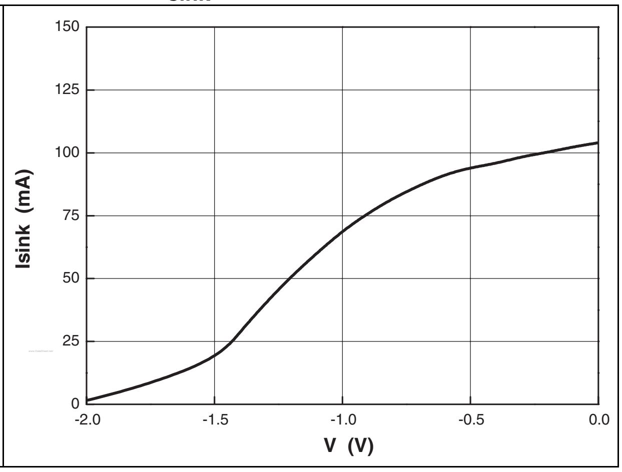


Figure 11. I_{source}

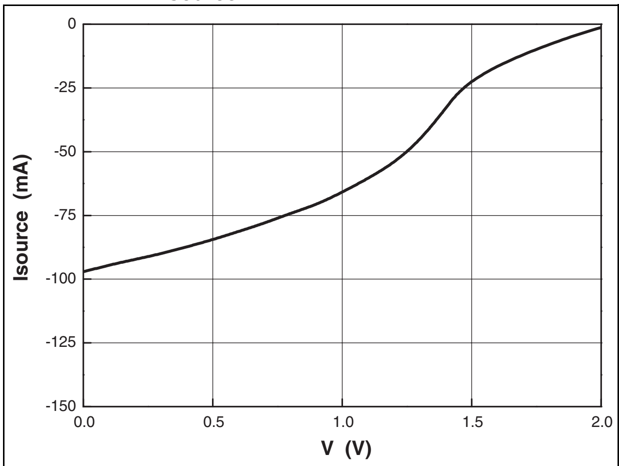


Figure 12. Bandwidth vs. temperature

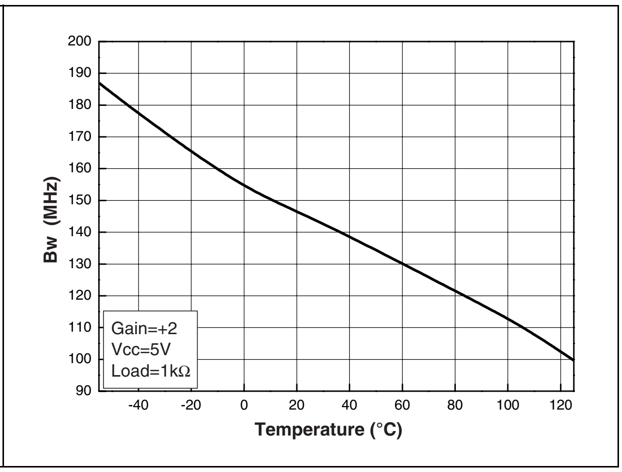


Figure 13. CMR vs. temperature

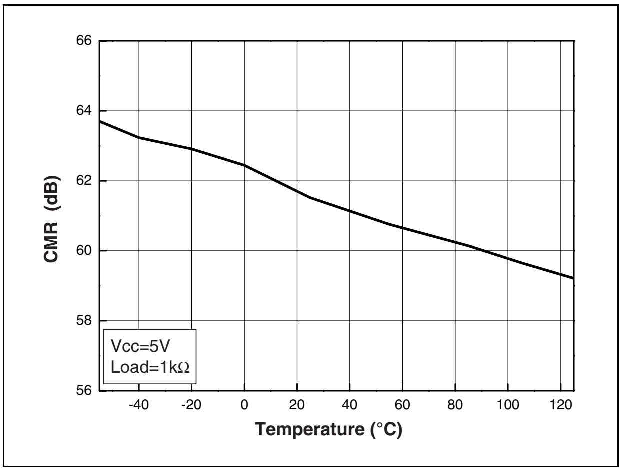


Figure 14. SVR vs. temperature

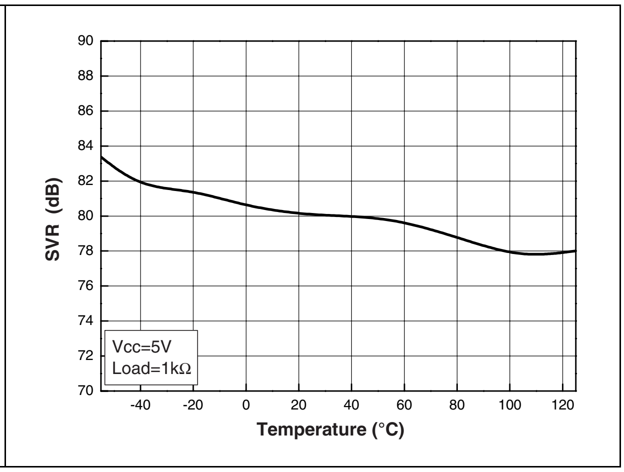


Figure 15. Slew rate vs. temperature

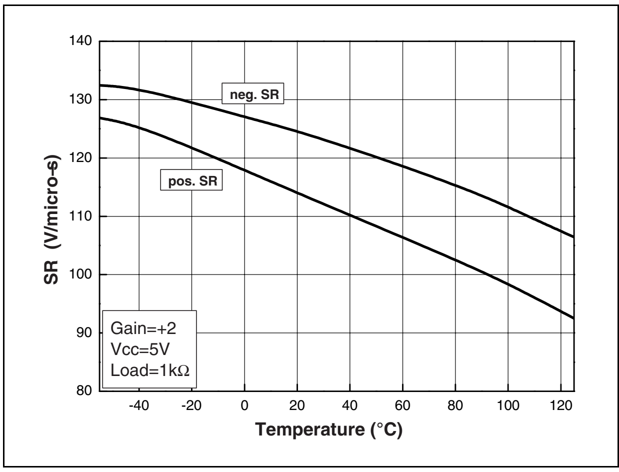


Figure 16. R_{OL} vs. temperature

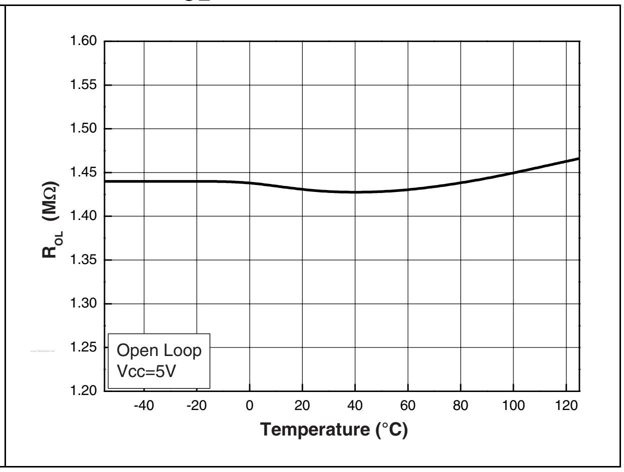


Figure 17. I_{bias} vs. temperature

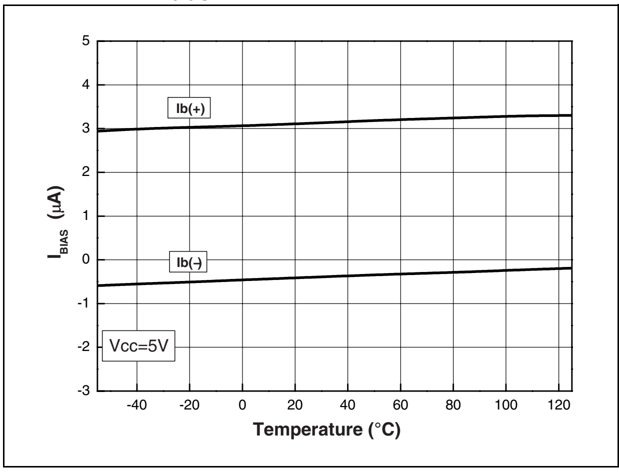


Figure 18. V_{io} vs. temperature

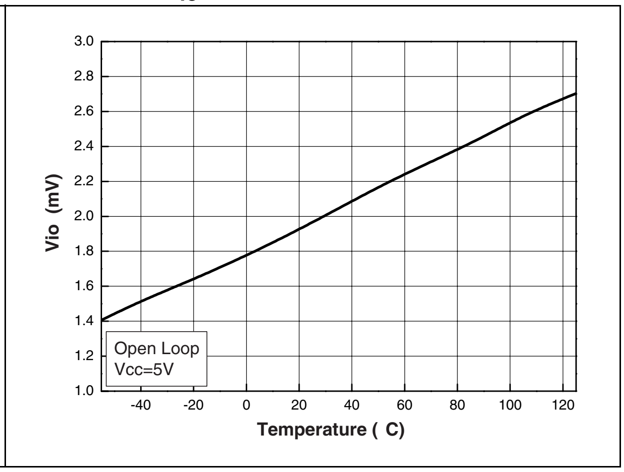


Figure 19. V_{OH} and V_{OL} vs. temperature

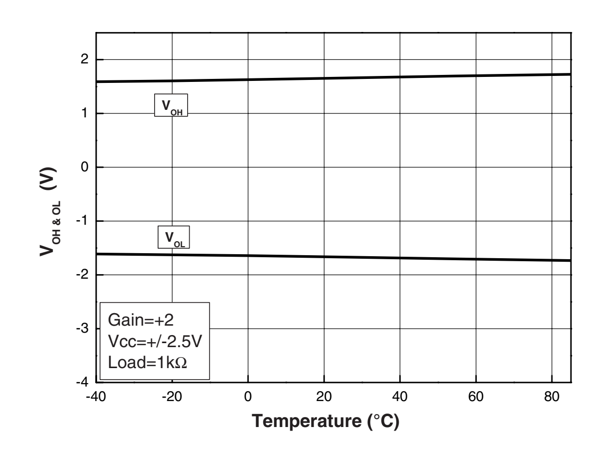


Figure 20. I_{out} vs. temperature

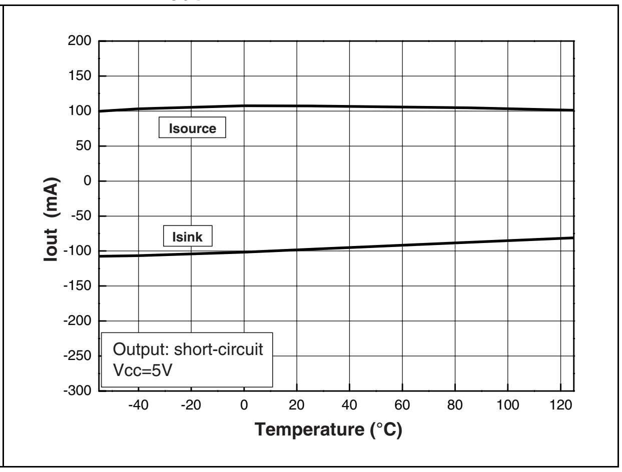
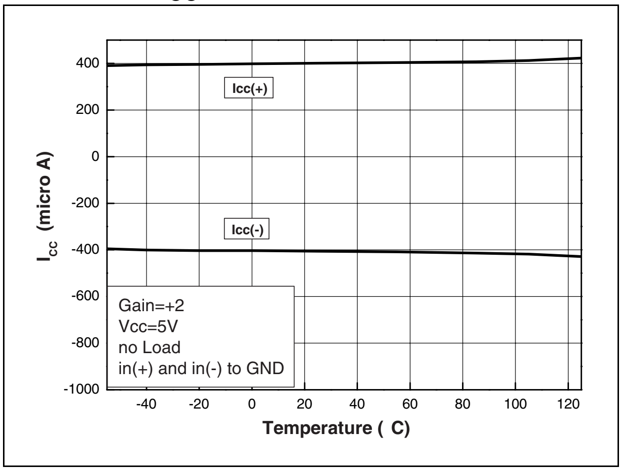


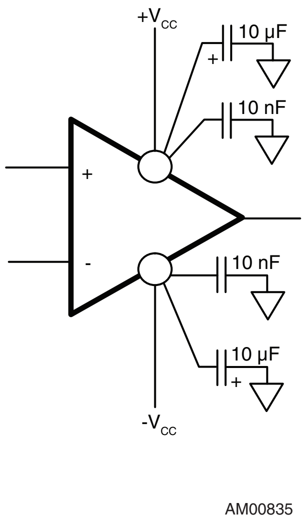
Figure 21. I_{CC} vs. temperature



3 Power supply considerations

Correct power supply bypassing is very important for optimizing the performance of the device in high-frequency ranges. The bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1 µF is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10 nF can be added, which should also be placed as close as possible to the IC pins. The bypass capacitors must be incorporated for both the negative and positive supply.

Figure 22. Circuit for power supply bypassing



3.1 Single power supply

If you use a single-supply system, biasing is necessary to obtain a positive output dynamic range between the 0 V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier provides an output swing from +0.9 V to +4.1 V on 1 kΩ loads.

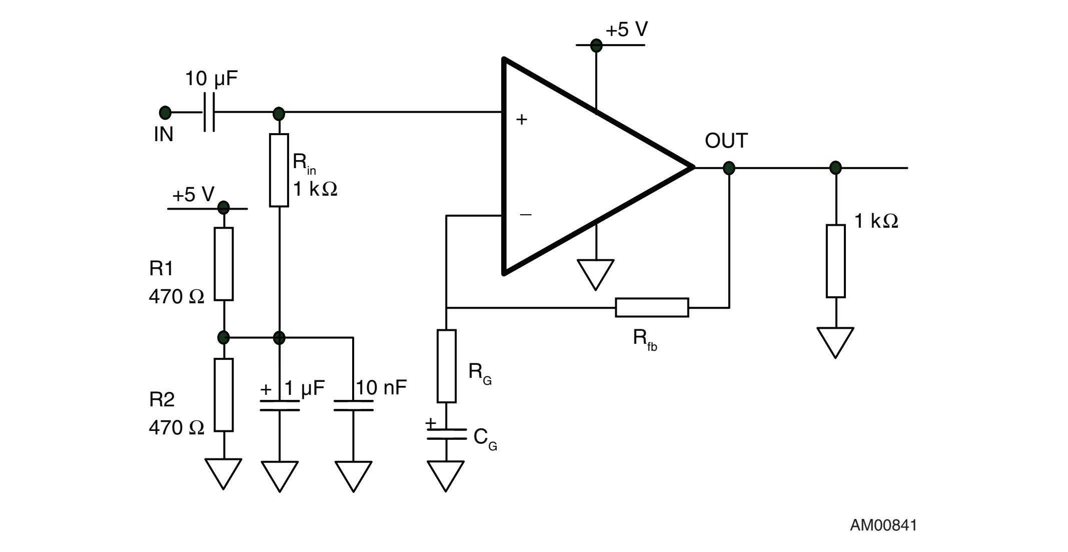
The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$) in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (55 µA maximum) as 1% of the current through the resistance divider, two resistances of 470 Ω can be used to maintain a mid supply.

The input provides a high-pass filter with a break frequency below 10 Hz, which is necessary to remove the original 0 V DC component of the input signal and to set it at $+V_{CC}/2$.

Figure 23 on page 12 illustrates a 5 V single power supply configuration.

A capacitor C_G is added in the gain network to ensure a unity gain at low frequencies to keep the right DC component at the output. C_G contributes to a high-pass filter with $R_{fb}//R_G$ and its value is calculated with a consideration of the cut-off frequency of this low-pass filter.

Figure 23. Circuit for +5 V single supply

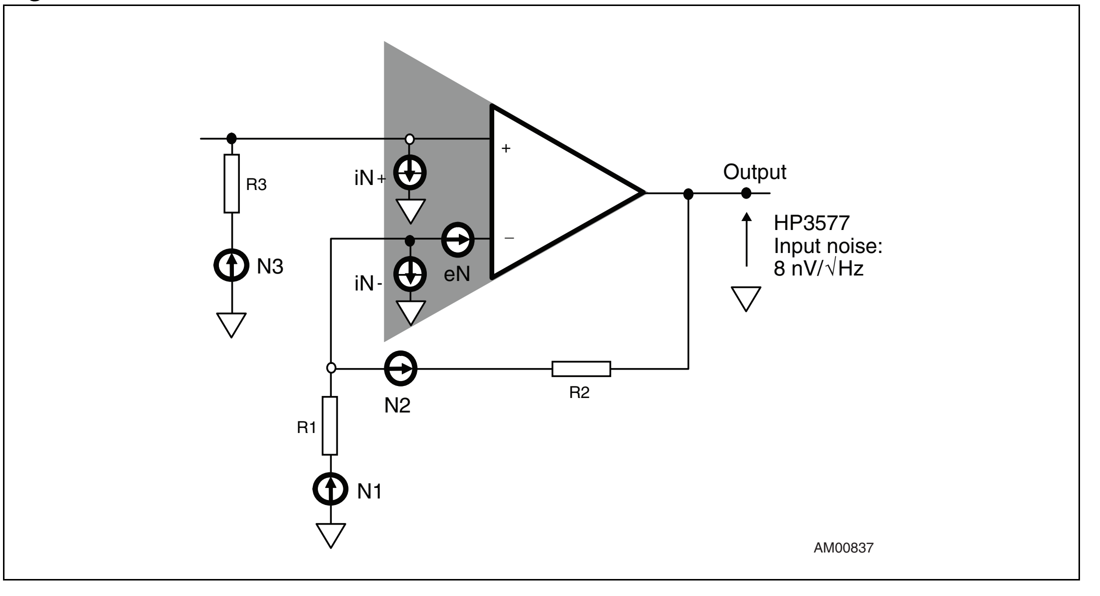


4 Noise measurements

The noise model is shown in *Figure 24*.

- eN: input voltage noise of the amplifier.
- iNn: negative input current noise of the amplifier.
- iNp: positive input current noise of the amplifier.

Figure 24. Noise model



The thermal noise of a resistance R is:

$$\sqrt{4kTR\Delta F}$$

where ΔF is the specified bandwidth, and k is the Boltzmann's constant, equal to 1,374.10-23J/°K. T is the temperature (°K).

On a 1 Hz bandwidth the thermal noise is reduced to:

$$\sqrt{4kTR}$$

The output noise eNo is calculated using the superposition theorem. However, eNo is not the simple sum of all noise sources but rather the square root of the sum of the square of each noise source, as shown in *Equation 1*.

Equation 1

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

Equation 2

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

Equation 3

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2}$$

The input noise is called **equivalent input noise** because it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and fifth terms of *Equation 2*, you obtain:

Equation 4

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

4.1 Measurement of the input voltage noise *eN*

Assuming a short-circuit on the non-inverting input (R3=0), from *Equation 4* you can derive:

Equation 5

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}$$

To easily extract the value of eN, the resistance R2 must be as low as possible. On the other hand, the gain must be high enough.

R3=0, gain: g=100

4.2 Measurement of the negative input current noise *iNn*

To measure the negative input current noise iNn, R3 is set to zero and *Equation 5* is used. This time, the gain must be lower in order to decrease the thermal noise contribution.

R3=0, gain: g=10

4.3 Measurement of the positive input current noise *iNp*

To extract iNp from *Equation 3*, a resistance R3 is connected to the non-inverting input. The value of R3 must be selected so as to keep its thermal noise contribution as low as possible against the iNp contribution.

R3=100 Ω, gain: g=10

5 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series of equations.

$$V_{out} = C_0 + C_1 V_{in} + C_2 V^2{}_{in} + \ldots + C_n V^n{}_{in}$$

where the input is $V_{in} = A\sin\omega t$, C_0 is the DC component, $C_1(V_{in})$ is the fundamental and C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A\sin\omega_1 t + A\sin\omega_2 t$$

therefore:

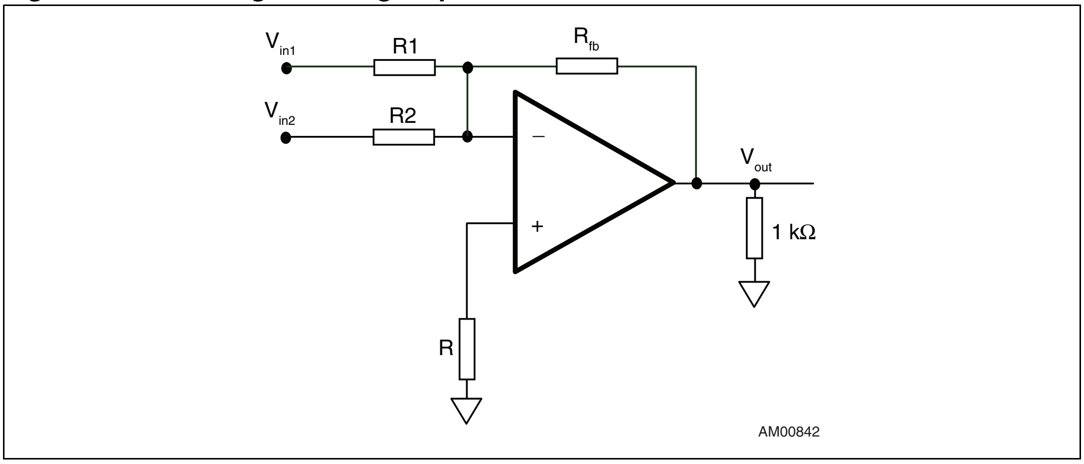
$$V_{out} = C_0 + C_1(A\sin\omega_1 t + A\sin\omega_2 t) + C_2(A\sin\omega_1 t + A\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + A\sin\omega_2 t)^n$$

From this expression, we can extract the distortion terms and the intermodulation terms from a single sine wave.

- Second-order intermodulation terms IM2 by the frequencies $(\omega_1-\omega_2)$ and $(\omega_1+\omega_2)$ with an amplitude of $C2A^2$.
- Third-order intermodulation terms IM3 by the frequencies $(2\omega_1-\omega_2)$, $(2\omega_1+\omega_2)$, $(-\omega_1+2\omega_2)$ and $(\omega_1+2\omega_2)$ with an amplitude of $(3/4)C3A^3$.

The intermodulation product of the driver is measured by using the driver as a mixer in a summing amplifier configuration (*Figure 25*). In this way, the non-linearity problem of an external mixing device is avoided.

Figure 25. Inverting summing amplifier



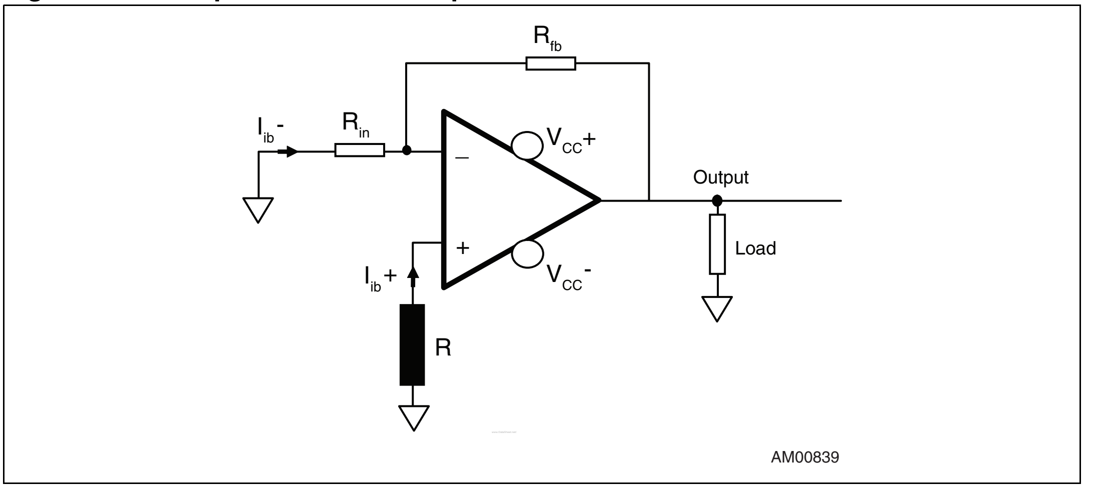
6 Bias of an inverting amplifier

A resistance is necessary to achieve good input biasing, such as resistance R shown in *Figure 26*.

The value of this resistance is calculated from the negative and positive input bias current. The aim is to compensate for the offset bias current, which can affect the input offset voltage and the output DC component. Assuming I_{ib-}, I_{ib+}, R_{in}, R_{fb} and a 0 V output, the resistance R is:

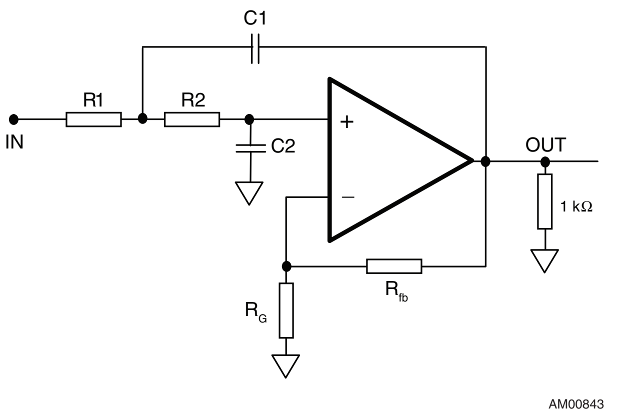
$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

Figure 26. Compensation of the input bias current



7 Active filtering

Figure 27. Low-pass active filtering, Sallen-Key



From the resistors R_{fb} and R_G it is possible to directly calculate the gain of the filter in a classic non-inverting amplification configuration.

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The response of the system is assumed to be:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated using the following expression.

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

The higher the gain, the more sensitive the damping factor. When the gain is higher than 1, it is preferable to use very stable resistor and capacitor values. In the case of R1=R2=R:

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

Due to a limited selection of capacitor values in comparison with the resistors, you can set C1=C2=C, so that:

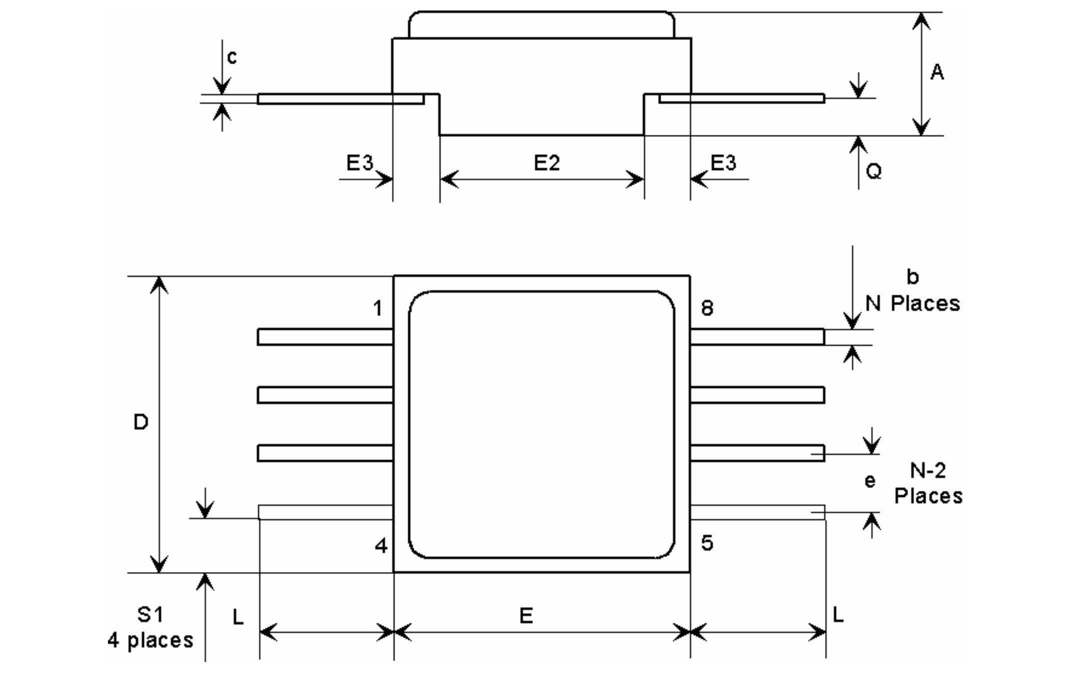
$$\zeta = \frac{2R_2 - R_1\frac{R_{fb}}{R_g}}{2\sqrt{R_1R_2}}$$

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 Ceramic Flat-8 package information

Figure 28. Ceramic Flat-8 package mechanical drawing



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 6. Ceramic Flat-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L		3.00			0.118	
Q	0.66	0.79	0.92	0.026	0.031	0.092
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

9 Revision history

Table 7. Document revision history

Date	Revision	Changes
26-May-2009	1	Initial release.
12-Jul-2010	2	Added *Mass* in *Features* on cover page. Added *Table 1: Device summary* on cover page, with full ordering information. Updated temperature limits for $T_{min} < T_{amb} < T_{max}$ in *Table 3: Operating conditions*.
27-Jul-2011	3	Added *Note: on page 20* and in the "Pin connections" diagram on the coverpage.

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