TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX573F,TC74LCX573FT,TC74LCX573FK

Low-Voltage Octal D-Type Latch with 5-V Tolerant Inputs and Outputs

The TC74LCX573 is a high-performance CMOS octal D-type latch. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage $(3.3\ V)\ VCC$ applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

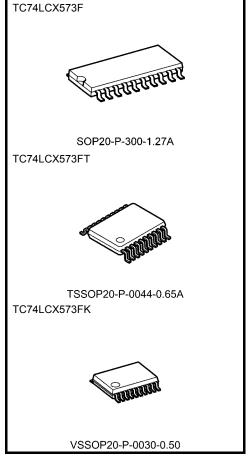
This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

Features

- Low-voltage operation: VCC = 1.65 to 3.6 V
- High-speed operation: $t_{pd} = 8.0 \text{ ns (max) (V}_{CC} = 3.0 \text{ to } 3.6 \text{ V)}$
- Output current: | I_{OH} | /I_{OL} = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: > ±500 mA
- Available in JEITA SOP, TSSOP and VSSOP (US)
- · Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 573 type

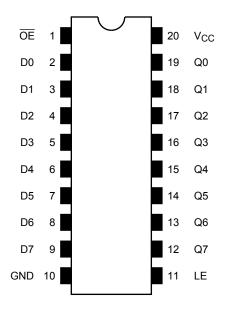


Weight

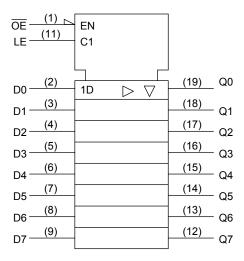
SOP20-P-300-1.27A : 0.22 g (typ.) TSSOP20-P-0044-0.65A : 0.08 g (typ.) VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Note: The Electrical Characteristics of $V_{CC}=1.8\pm0.15V$ is only applicable for products which manufactured from January 2009 onward.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

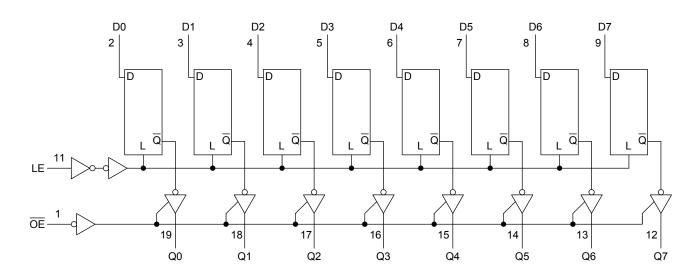
	Inputs				
ŌĒ	LE	D	Outputs		
Н	Х	Х	Z		
L	L	Х	Qn		
L	Н	L	L		
L	Н	Н	Н		

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram





Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
		-0.5 to 7.0 (Note 2)	
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
		(Note 3)	
Input diode current	I _{IK}	-50	mA
Output diode current	I _{OK}	±50 (Note 4)	mA
DC output current	lout	±50	mA
Power dissipation	P _D	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.65 to 3.6	V
Tower suppry voltage	VCC	1.5 to 3.6 (Note 2)	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to 5.5 (Note 3)	V
Output voltage		0 to V _{CC} (Note 4)	
Output current	la/la.	±24 (Note 5)	mA
Output current	I _{OH} /I _{OL}	±12 (Note 6)	ША
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5: $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$

Note 6: $V_{CC} = 2.7 \text{ to } 3.0 \text{ V}$

Note 7: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V



Electrical Characteristics

DC Characteristics ($Ta = -40 \text{ to } 85^{\circ}\text{C}$)

Characteristics		Symbol Test Condition		Γ	Min	Max	Unit	
		,	V _{CC} (V)		V _{CC} (V)			
					1.65 to 2.3	V _{CC} × 0.9	_	
	H-level	V_{IH}	_		2.3 to 2.7	1.7	_	
Input voltage					2.7 to 3.6	2.0	_	V
Input voltage					1.65 to 2.3	_	V _{CC} × 0.1	
	L-level	V_{IL}	_	-	2.3 to 2.7	_	0.7	
					2.7 to 3.6	_	0.8	
				$I_{OH} = -100 \mu A$	1.65 to 3.6	V _{CC} -0.2	_	
				I _{OH} = -4 mA	1.65	1.05	_	
	Harrel	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	\ \ \\ \ \\ \ \\ \\ \\ \\ \\ \\ \\ \\ \	$I_{OH} = -8 \text{ mA}$	2.3	1.7	_	V
	H-level	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -12 mA	2.7	2.2	_	
				I _{OH} = -18 mA	3.0	2.4	_	
Outrout valtage				I _{OH} = -24 mA	3.0	2.2	_	
Output voltage			V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.65 to 3.6	_	0.2	
				I _{OL} = 4 mA	1.65	_	0.45	
				I _{OL} = 8 mA	2.3	_	0.7	
	L-level	V _{OL}		I _{OL} = 12 mA	2.7	_	0.4	
				I _{OL} = 16 mA	3.0	_	0.4	
				I _{OL} = 24 mA	3.0	_	0.55	
Input leakage current		I _{IN}	$V_{IN} = 0 \text{ to } 5.5 \text{ V}$		1.65 to 3.6	_	±5.0	μΑ
3-state output OFF state current		loz	$V_{IN} = V_{IH}$ or V_{IL}		1.65 to 3.6		±5.0	μА
		102	V _{OUT} = 0 to 5.5 V		1.03 to 3.0		±3.0	μΛ
Power-off leakage cur	rent	l _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0	_	10.0	μΑ
Quiescent supply curr	Quiescent aupply aurrent		V _{IN} = V _{CC} or GND		1.65 to 3.6	_	10.0	
Quicocont supply cult	- Cint	Icc	V _{IN} /V _{OUT} = 3.6 to 5.5 V		1.65 to 3.6	_	±10.0	μΑ
Increase in I _{CC} per inp	out	Δlcc	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6	_	500	



AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition		Min	Max	Unit
Ondractoristics	Cymbol	rest condition	V _{CC} (V)	141111	IVIAX	O i iii
			1.8±0.15		30.0	ns
Propagation delay time	t_{pLH}	Figure 1, Figure 2	2.5±0.2	_	10.0	
(D-Q)	t _{pHL}	rigure 1, rigure 2	2.7	_	9.0	
			3.3 ± 0.3	1.5	8.0	
			1.8±0.15		30.0	
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.5±0.2		10.5	ns
(LE-Q)	t _{pHL}	rigure 1, rigure 2	2.7		9.5	113
			3.3 ± 0.3	1.5	8.5	
			1.8±0.15		34.0	
Output anable time	t _{pZL}	Figure 1 Figure 2	2.5±0.2	_	17.0	20
Output enable time	t _{pZH}	Figure 1, Figure 3	2.7	_	9.5	ns
			3.3 ± 0.3	1.5	8.5	
			1.8±0.15	_	28.0	
Outrot disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	2.5±0.2	_	14.0	ns
Output disable time			2.7	_	7.0	
			3.3 ± 0.3	1.5	6.5	
		Figure 1, Figure 2	1.8±0.15	10.0	_	ns
Minimum pulse width	4 (11)		2.5±0.2	5.0	_	
(LE)	t _w (H)		2.7	3.3		
			3.3 ± 0.3	3.3		
			1.8±0.15	10.0	_	- ns
Minimum outur timo			2.5±0.2	5.0	_	
Minimum setup time	t _s	Figure 1, Figure 2	2.7	2.5	_	
			3.3 ± 0.3	2.5		
			1.8±0.15	1.5	_	
Minimum hold time	4.	Figure 1, Figure 2	2.5±0.2	1.5	_	ns
	t _h		2.7	1.5	_	
			3.3 ± 0.3	1.5	_	
Output to output skew	t _{osLH}	(Nlota)	2.7		_	no
Output to output skew	t _{osHL}	(Note)	3.3 ± 0.3		1.0	ns

Note: Parameter guaranteed by design.

 $(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$



Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

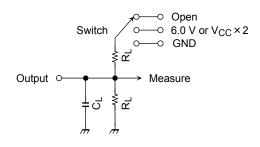
Characteristics	Symbol	Test Condition		V _{CC} (V)	Тур.	Unit
Input capacitance	C _{IN}	_		3.3	7	pF
Output capacitance	C _{OUT}	_		3.3	8	pF
Power dissipation capacitance	C _{PD}	$f_{IN} = 10 \text{ MHz}$	lote)	3.3	25	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$

AC Test Circuit



Parameter	Switch		
t _{pLH} , t _{pHL}	Open		
	6.0 V	@ V _{CC} =3.3±0.3V	
		@ V _{CC} =2.7V	
t _{pLZ} , t _{pZL}	V _{CC} ×2	@ V _{CC} =2.5±0.2V	
		@ V _{CC} =1.8±0.15V	
t _{pHZ} , t _{pZH}	GND		

Figure 1

6



AC Waveform

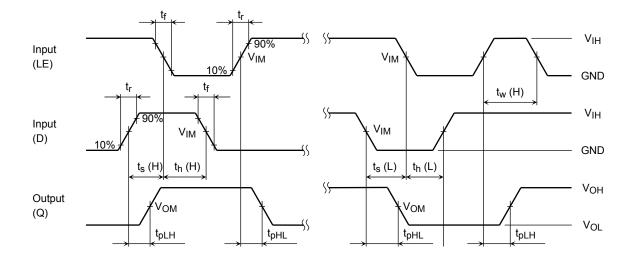


Figure 2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

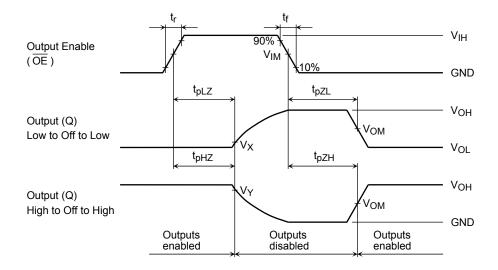


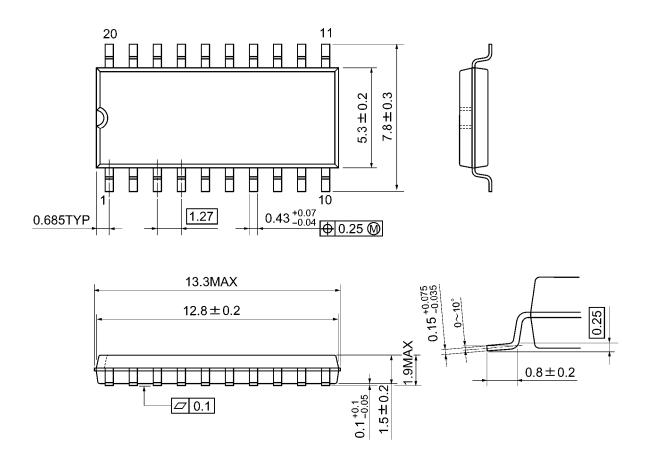
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

		Vcc				
	Symbol	$3.3\pm0.3~\textrm{V}$	2.5 ± 0.2 V	1.8 ± 0.15 V		
		2.7V	2.5 ± 0.2 V	1.6 ± 0.15 V		
Input	V _{IH}	2.7V	V _{CC}	V _{CC}		
	V _{IM}	1.5V	V _{CC} /2	V _{CC} /2		
	tr,tf	2.5ns	2.0ns	2.0ns		
Output	V _{OM}	1.5V	V _{OH} /2	V _{OH} /2		
	VX	V _{OL} +0.3V	V _{OL} +0.15V	V _{OL} +0.15V		
	VY	V _{OH} -0.3V	V _{OH} -0.15V	V _{OH} -0.15V		
Load	CL	50pF	30pF	30pF		
	R_{L}	500Ω	500Ω	1kΩ		



Package Dimensions

SOP20-P-300-1.27A Unit: mm

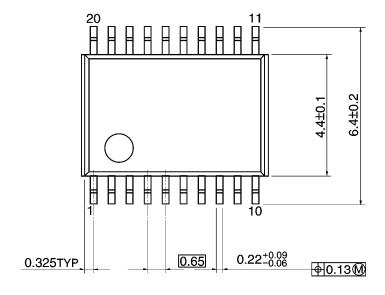


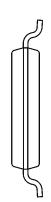
Weight: 0.22 g (typ.)

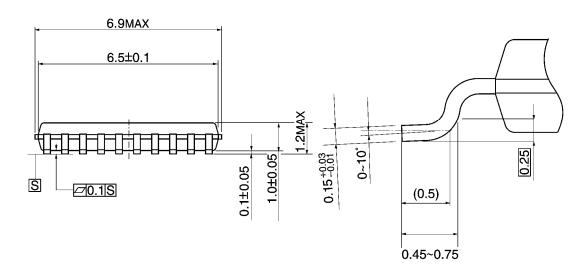
Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm





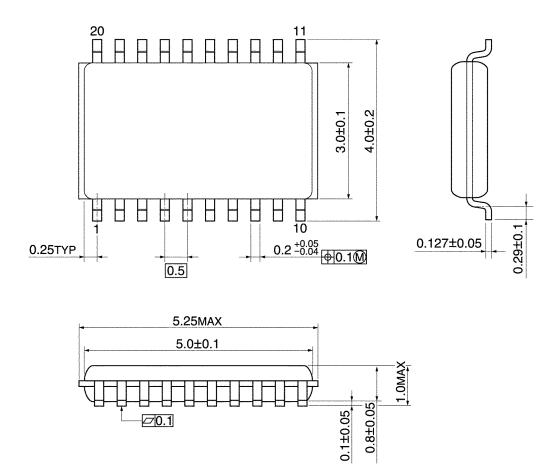


9

Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)

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11