



CYPRESS

PRELIMINARY

CY7C1361V25  
CY7C1363V25  
CY7C1365V25

## 256K x 36/256K x 32/512K x 18 Flowthrough SRAM

### Features

- Supports 113-MHz bus operations
- 256K x 36 / 256K x 32 / 512K x 18 common I/O
- Fast clock-to-output times
  - 7.5 ns (for 117-MHz device)
  - 8.5 ns (for 100-MHz device)
  - 10.0 ns (for 80-MHz device)
- Two-bit wrap-around counter supporting either interleaved or linear burst sequences
- Separate processor and controller address strobes provide direct interface with the processor and external cache controller
- Synchronous self-timed writes
- Asynchronous output enable
- Single 2.5V Power supply
- JEDEC-standard pinout
- Available as a 100-pin TQFP or 119 BGA
- "ZZ" Sleep Mode option

flowthrough SRAM designed to interface with high-speed microprocessors with minimal glue logic. Maximum access delay from the clock rise is 7.5 ns (117-MHz device). A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

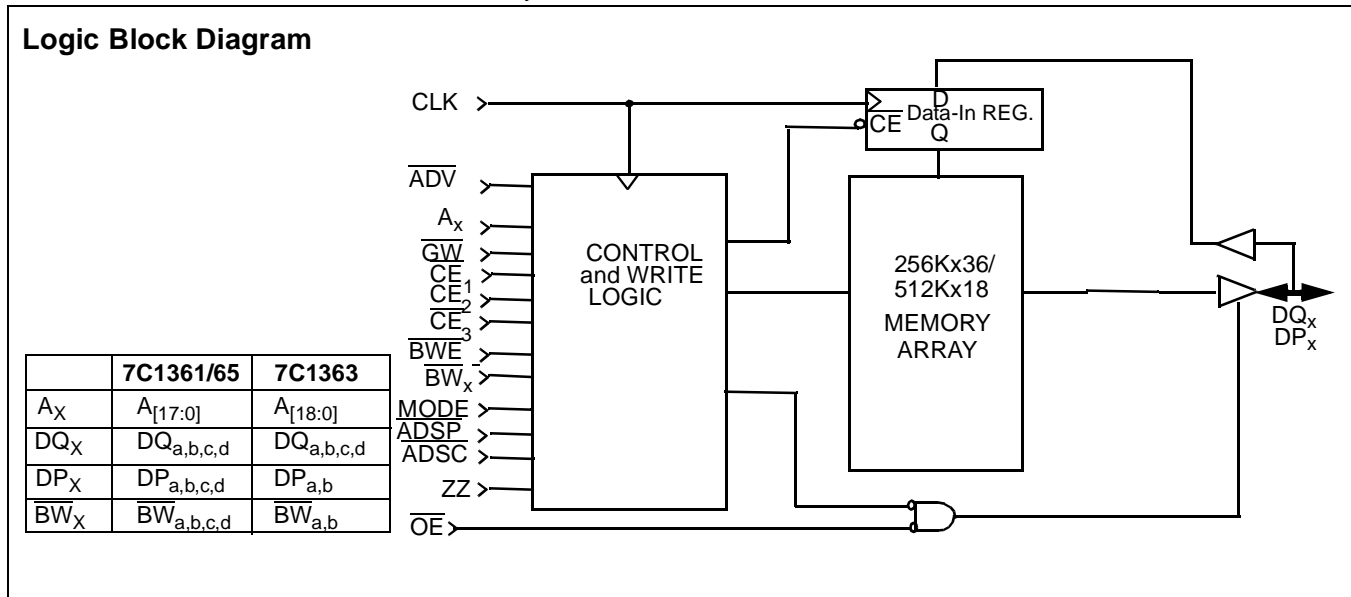
The CY7C1361V25/CY7C1365V25/CY7C1363V25 supports either the interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated by asserting either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC) at clock rise. Address advancement through the burst sequence is controlled by the  $\overline{ADV}$  input. Byte write operations are qualified with the Byte Write Select ( $BW_{a,b,c,d}$  for CY7C1361V25/CY7C1365V25 and  $BW_{a,b}$  for CY7C1363V25) inputs. A Global Write Enable ( $\overline{GW}$ ) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output three-state control.

### Functional Description

The CY7C1361V25, CY7C1365V25 and CY7C1363V25 are 2.5v, 256K x 36, 256K x 32 and 512K x 18 synchronous-

### Logic Block Diagram



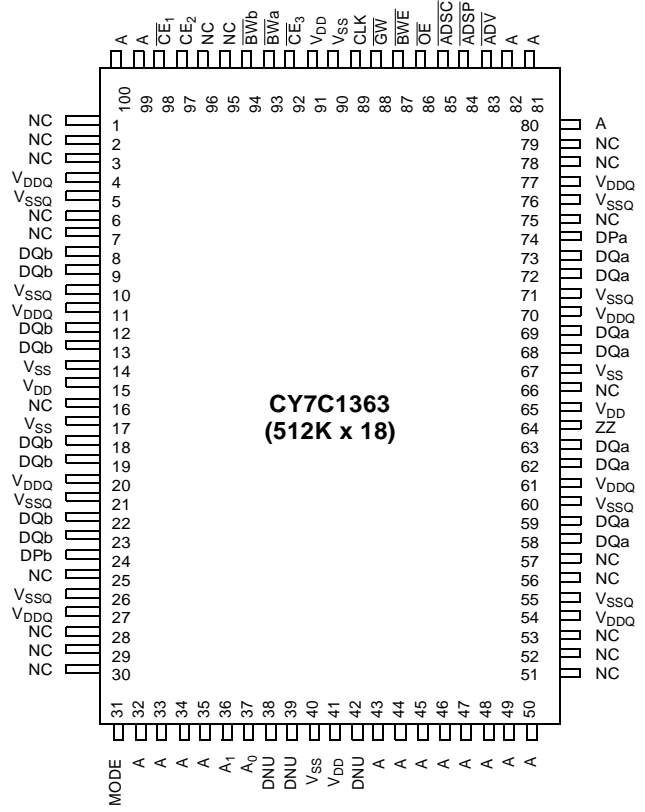
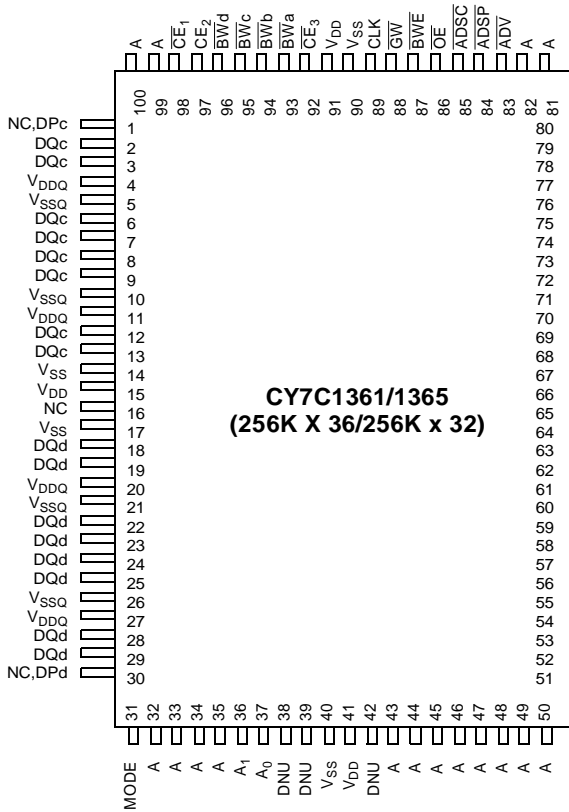
### Selection Guide

	7C1361-133 7C1365-133 7C1363-133	7C1361-117 7C1365-117 7C1363-117	7C1361-100 7C1365-100 7C1363-100	7C1361-80 7C1365-80 7C1363-80
Maximum Access Time (ns)	6.5	7.5	8.5	10.0
Maximum Operating Current (mA)	Commercial			
	350	300	260	210
Maximum CMOS Standby Current (mA)	10	10	10	10

Shaded areas contain advance information.

Pin Configurations

100-Pin TQFP



**Pin Configurations (continued)**
**119-Ball BGA  
CY7C1361/CY7C1365 (256K x 36, 256K x 32)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>c</sub>	NC,DP <sub>c</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	NC,DP <sub>b</sub>	DQ <sub>b</sub>
<b>E</b>	DQ <sub>c</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	DQ <sub>b</sub>	DQ <sub>b</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>b</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>c</sub>	DQ <sub>c</sub>	$\overline{\text{BW}}_c$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_b$	DQ <sub>b</sub>	DQ <sub>b</sub>
<b>H</b>	DQ <sub>c</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>b</sub>	DQ <sub>b</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>d</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>a</sub>	DQ <sub>a</sub>
<b>L</b>	DQ <sub>d</sub>	DQ <sub>d</sub>	$\overline{\text{BW}}_d$	NC	$\overline{\text{BW}}_a$	DQ <sub>a</sub>	DQ <sub>a</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQ <sub>a</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>d</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>a</sub>	DQ <sub>a</sub>
<b>P</b>	DQ <sub>d</sub>	NC,DP <sub>d</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC,DP <sub>a</sub>	DQ <sub>a</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	V <sub>SS</sub>	A	NC
<b>T</b>	NC	NC	A	A	A	NC	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	DNU	V <sub>DDQ</sub>

**CY7C1363 (512K x 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>b</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DP <sub>a</sub>	NC
<b>E</b>	NC	DQ <sub>b</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	NC	DQ <sub>a</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>a</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>b</sub>	$\overline{\text{BW}}_b$	$\overline{\text{ADV}}$	V <sub>SS</sub>	NC	DQ <sub>a</sub>
<b>H</b>	DQ <sub>b</sub>	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>b</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>b</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>a</sub>
<b>L</b>	DQ <sub>b</sub>	NC	V <sub>SS</sub>	NC	$\overline{\text{BW}}_a$	DQ <sub>a</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>b</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>b</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>a</sub>	NC
<b>P</b>	NC	DP <sub>b</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>a</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	V <sub>SS</sub>	A	NC
<b>T</b>	NC	A	A	NC	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	DNU	V <sub>DDQ</sub>

**Pin Definitions (100-Pin TQFP)**

x18 Pin Location	x36 Pin Location	Name	I/O	Description
37, 36, 32–25, 43–50, 80–82, 99, 100	37, 36, 32–35, 43–50, 81, 82, 99, 100	A0 A1 A	Input- Synchronous	Address Inputs used to select one of the address locations. Sampled at the rising edge of the CLK if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is active LOW, and $\overline{\text{CE}}_1$ , $\overline{\text{CE}}_2$ , and $\overline{\text{CE}}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
93, 94	93, 94, 95, 96	$\overline{\text{BW}}_a$ $\overline{\text{BW}}_b$ $\overline{\text{BW}}_c$ $\overline{\text{BW}}_d$	Input- Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{\text{BWE}}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	88	$\overline{\text{GW}}$	Input- Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{\text{BW}}_{a,b,c,d}$ and $\overline{\text{BWE}}$ ).
87	87	$\overline{\text{BWE}}$	Input- Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	89	CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{\text{ADV}}$ is asserted LOW, during a burst operation.
98	98	$\overline{\text{CE}}_1$	Input- Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_2$ and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH.
97	97	$\overline{\text{CE}}_2$	Input- Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device.
92	92	$\overline{\text{CE}}_3$	Input- Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ to select/deselect the device.
86	86	$\overline{\text{OE}}$	Input- Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a read cycle when emerging from a deselected state.
83	83	$\overline{\text{ADV}}$	Input- Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	84	$\overline{\text{ADSP}}$	Input- Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized. $\overline{\text{ADSP}}$ is ignored when $\overline{\text{CE}}_1$ is deasserted HIGH.
85	85	$\overline{\text{ADSC}}$	Input- Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[x:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized.
31	31	MODE	Input- Static	Selects burst order. When tied to GND selects linear burst sequence. When tied to $V_{\text{DDQ}}$ or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.

**Pin Definitions (100-Pin TQFP) (continued)**

x18 Pin Location	x36 Pin Location	Name	I/O	Description
64	64	ZZ	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved.
(a)58, 59, 62, 63, 68, 69, 72, 73 (b)8, 9, 12, 13, 18, 19, 22, 23	(a)52, 53, 56-59, 62, 63 (b)68, 69, 72-75, 78, 79 (c)2, 3, 6-9, 12, 13 (d)18, 19, 22-25, 28, 29	NC,DQ <sub>a</sub> NC,DQ <sub>b</sub> NC,DQ <sub>c</sub> NC,DQ <sub>d</sub>	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>x</sub> and DP <sub>x</sub> are placed in a three-state condition. On the CY7C1365 SRAM, these are not connect pins.
74, 24	51, 80, 1, 30	DP <sub>a</sub> DP <sub>b</sub> DP <sub>c</sub> DP <sub>d</sub>	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>a</sub> -DQ <sub>d</sub> and DP <sub>a</sub> -DP <sub>d</sub> are placed in a three-state condition.
15, 41, 65, 91	15, 41, 65, 91	V <sub>DD</sub>	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
17, 40, 67, 90	17, 40, 67, 90	V <sub>SS</sub>	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	V <sub>DDQ</sub>	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5V power supply.
5, 10, 21, 26, 55, 60, 71, 76	5, 10, 21, 26, 55, 60, 71, 76	V <sub>SSQ</sub>	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	16, 66	NC	-	No Connects.
42	42	DNU		Do Not Use Pins. This pin is used for the address expansion to the next density SRAM.
38, 39	38, 39	DNU		Do Not Use Pins. These pins should be left floating or tied to V <sub>SS</sub> .

**Pin Definitions (119-Ball BGA)**

x18 Pin Location	x36 Pin Location	Name	I/O	Description
4P, 4N, 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6B, 6T	4P, 4N, 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R	A0 A1 A	Input-Synchronous	Address Inputs used to select one of the address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$ , $CE_2$ , and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
5L, 3G	5L, 5G, 3G, 3L	$\overline{BW}_a$ $\overline{BW}_b$ $\overline{BW}_c$ $\overline{BW}_d$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
4M	4M	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{a,b,c,d}$ and $\overline{BWE}$ ).
4H	4H	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
4K	4K	CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
4E	4E	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH.
97	97	$CE_2$	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. This pin will be used for address expansion to the next density SRAM.
92	92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select/deselect the device.
4F	4F	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
4G	4G	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
4A	4A	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ADSP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
4B	4B	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[x:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.

**Pin Definitions (119-Ball BGA) (continued)**

x18 Pin Location	x36 Pin Location	Name	I/O	Description
3R	3R	MODE	Input-Static	Selects burst order. When tied to GND selects linear burst sequence. When tied to $V_{DDQ}$ or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
7T	7T	ZZ	Input-Asynchronous	ZZ "sleep" Input. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
(a)6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b)1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a)6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b)6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c)1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d)1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	NC, DQ <sub>a</sub> NC, DQ <sub>b</sub> NC, DQ <sub>c</sub> NC, DQ <sub>d</sub>	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>x</sub> and DP <sub>x</sub> are placed in a three-state condition.  On the CY7C1365 SRAM, these are not connect pins.
6D, 2P	6P, 6D, 2D, 2P	DP <sub>a</sub> DP <sub>b</sub> DP <sub>c</sub> DP <sub>d</sub>	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>a</sub> -DQ <sub>b</sub> and DP <sub>a</sub> -DP <sub>d</sub> are placed in a three-state condition.
U5	U5	TDO	JTAG Serial Output, Synchronous	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK.
U3	U3	TDI	JTAG Serial Input, Synchronous	Serial data-In to the JTAG circuit. Sampled on the rising edge of TCK.
U2	U2	TMS	TestMode Select, Synchronous	This pin controls the Test Access Port state machine. Sampled on the rising edge of TCK.
U4	U4	TCK	JTAG-Clock	Clock input to the JTAG circuitry.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	$V_{DD}$	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	$V_{SS}$	Ground	Ground for the device. Should be connected to ground of the system.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	$V_{DDQ}$	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5V power supply.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	-	No Connects.
6U	6U	DNU		Do Not Use Pins. These pins should be left floating.

## Functional Description

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{ADSP}$  or  $\overline{ADSC}$  is asserted LOW, (2)  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$  are all asserted active, and (3) the write signals ( $\overline{GW}$ ,  $\overline{BWE}$ ) are all deasserted HIGH.  $\overline{ADSP}$  is ignored if  $\overline{CE}_1$  is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data will be available at the data outputs a maximum to  $t_{CDV}$  after clock rise.  $\overline{ADSP}$  is ignored if  $\overline{CE}_1$  is HIGH.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1)  $\overline{ADSP}$  is asserted LOW, and (2)  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$  are all asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_x$ ) and  $\overline{ADV}$  inputs are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. The CY7C1361V25/CY7C1365V25/CY7C1363V25 provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input ( $\overline{BWE}$ ) with the selected Byte Write ( $\overline{BW}_{a,b,c,d}$  for CY7C1361V25/CY7C1365V25 and  $\overline{BW}_{a,b}$  for CY7C1363V25) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. All I/Os are three-stated during a byte write.

Because the CY7C1361V25/CY7C1365V25/CY7C1363V25 is a common I/O device, the Output Enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ_x$  inputs. Doing so will three-state the output drivers. As a safety precaution,  $DQ_x$  are automatically three-stated whenever a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$  write accesses are initiated when the following conditions are satisfied: (1)  $\overline{ADSC}$  is asserted LOW, (2)  $\overline{ADSP}$  is deasserted HIGH, (3)  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$  are all asserted active, and (4) the appropriate combination of the write inputs ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_x$ ) are asserted active to conduct a write to the desired byte(s).  $\overline{ADSC}$  is ignored if  $\overline{ADSP}$  is active LOW.

The address presented to  $A_{[18:0]}$  is loaded into the address register and the address advancement logic while being delivered to the RAM core. The  $\overline{ADV}$  input is ignored during this cycle. If a global write is conducted, the data presented to the  $DQ_x$  is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation

will remain unaltered. All I/Os are three-stated during a byte write.

Because the CY7C1361V25/CY7C1365V25/CY7C1363V25 is a common I/O device, the Output Enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ_x$  inputs. Doing so will three-state the output drivers. As a safety precaution,  $DQ_x$  are automatically three-stated whenever a write cycle is detected, regardless of the state of  $\overline{OE}$ .

## Burst Sequences

The CY7C1361V25/CY7C1365V25/CY7C1363V25 provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting  $\overline{ADV}$  LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

## Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ HIGH places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ,  $\overline{ADSP}$ , and  $\overline{ADSC}$  must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW. Leaving ZZ unconnected defaults the device into an active state.



**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{CCZZ}$	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		15	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

**Cycle Descriptions<sup>[1, 2, 3]</sup>**

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	$CE_2$	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ "sleep"	None	H	X	X	X	X	X	X	X	Hi-Z	X

**Note:**

- X = "don't care", 1 = HIGH, 0 = LOW.
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state.  $\overline{OE}$  is a "Don't Care" for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ = High-Z when  $\overline{OE}$  is inactive or when the device is deselected, and DQ = data when  $\overline{OE}$  is active.



**Write Cycle Description<sup>[1, 2, 3]</sup>**

Function (1361/1365)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 - DQ <sub>a</sub>	1	0	1	1	1	0
Write Byte 1 - DQ <sub>b</sub>	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - DQ <sub>c</sub>	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - DQ <sub>d</sub>	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Function (1363)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	1	1	X	X
Read	1	0	1	1
Write Byte 0 - DQ <sub>a</sub> and DP <sub>a</sub>	1	0	1	0
Write Byte 1 - DQ <sub>b</sub> and DP <sub>b</sub>	1	0	0	1
Write All Bytes	1	0	0	0
Write All Bytes	0	X	X	X

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1361/63 incorporates a serial boundary scan Test Access Port (TAP) in the FBGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

### Test Access Port (TAP) - Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

### Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (See TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuit-

ry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### *Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a xx-bit-long register, and the x18 configuration has a yy-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the

SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE / PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### *EXTEST*

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does not recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE / PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE / PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

#### *IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### *SAMPLE / PRELOAD*

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE / PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE / PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

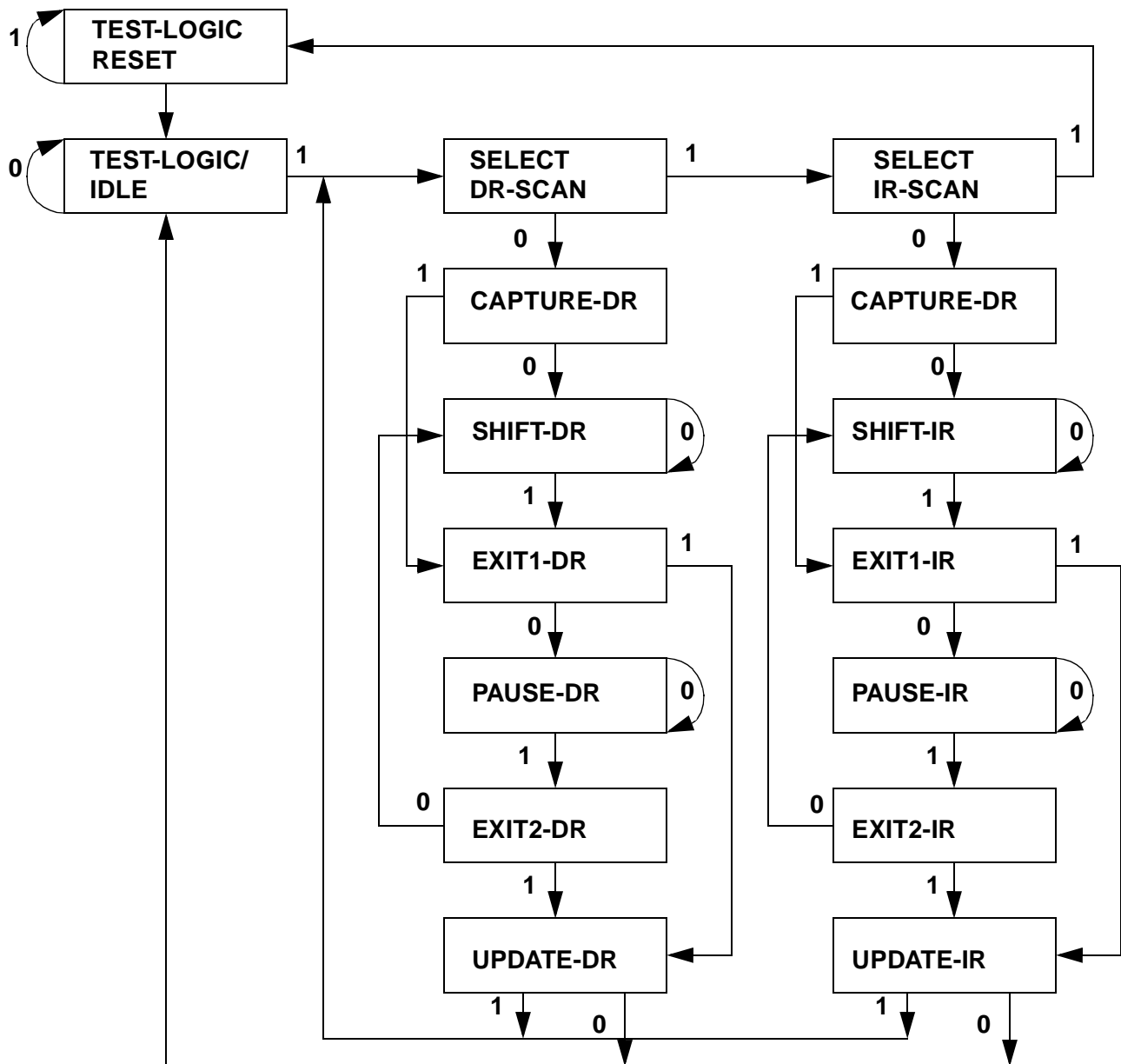
Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE / PRELOAD instruction will have the same effect as the Pause-DR command.

#### *BYPASS*

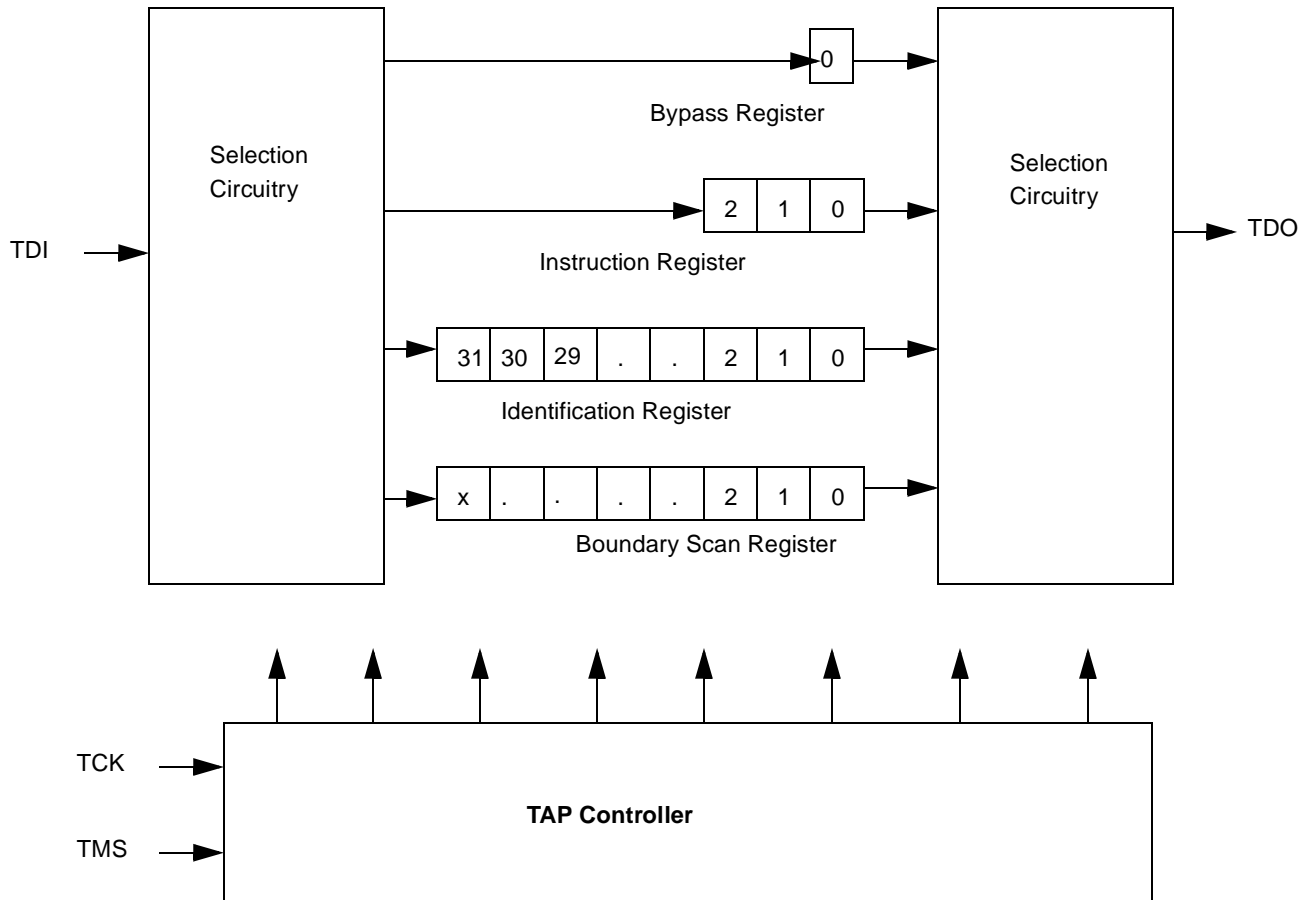
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

#### *Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

**TAP Controller State Diagram**


Note: The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

**TAP Controller Block Diagram**

**TAP Electrical Characteristics** Over the Operating Range<sup>[4, 5]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2.0 mA	1.7		V
V <sub>OH2</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 mA	2.1		V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.0 mA		0.7	V
V <sub>OL2</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 mA		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		1.7	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.7	V
I <sub>X</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	mA

**Notes:**

- All Voltage referenced to Ground.
- Overshoot: V<sub>IH</sub>(AC) ≤ V<sub>DD</sub>+1.5V for t<sub>≤t<sub>TCYC</sub>/2</sub>, Undershoot: V<sub>IL</sub>(AC) ≤ 0.5V for t<sub>≤t<sub>TCYC</sub>/2</sub>, Power-up: V<sub>IH</sub> < 2.6V and V<sub>DD</sub> < 2.4V and V<sub>DDQ</sub> < 1.4V for t < 200 ms.

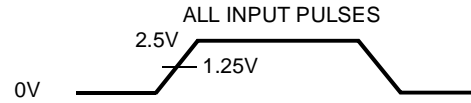
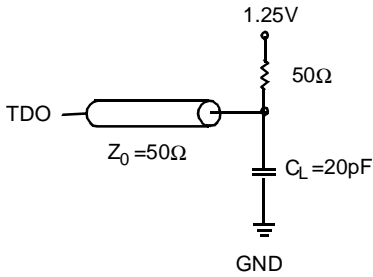
**TAP AC Switching Characteristics** Over the Operating Range<sup>[6, 7]</sup>

Parameter	Description	Min.	Max.	Unit
$t_{TCYC}$	TCK Clock Cycle Time	100		ns
$t_{TF}$	TCK Clock Frequency		10	MHz
$t_{TH}$	TCK Clock HIGH	40		ns
$t_{TL}$	TCK Clock LOW	40		ns
<b>Set-up Times</b>				
$t_{TMSS}$	TMS Set-up to TCK Clock Rise	10		ns
$t_{TDIS}$	TDI Set-up to TCK Clock Rise	10		ns
$t_{CS}$	Capture Set-up to TCK Rise	10		ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK Clock Rise	10		ns
$t_{TDIH}$	TDI Hold after Clock Rise	10		ns
$t_{CH}$	Capture Hold after Clock Rise	10		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		20	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns

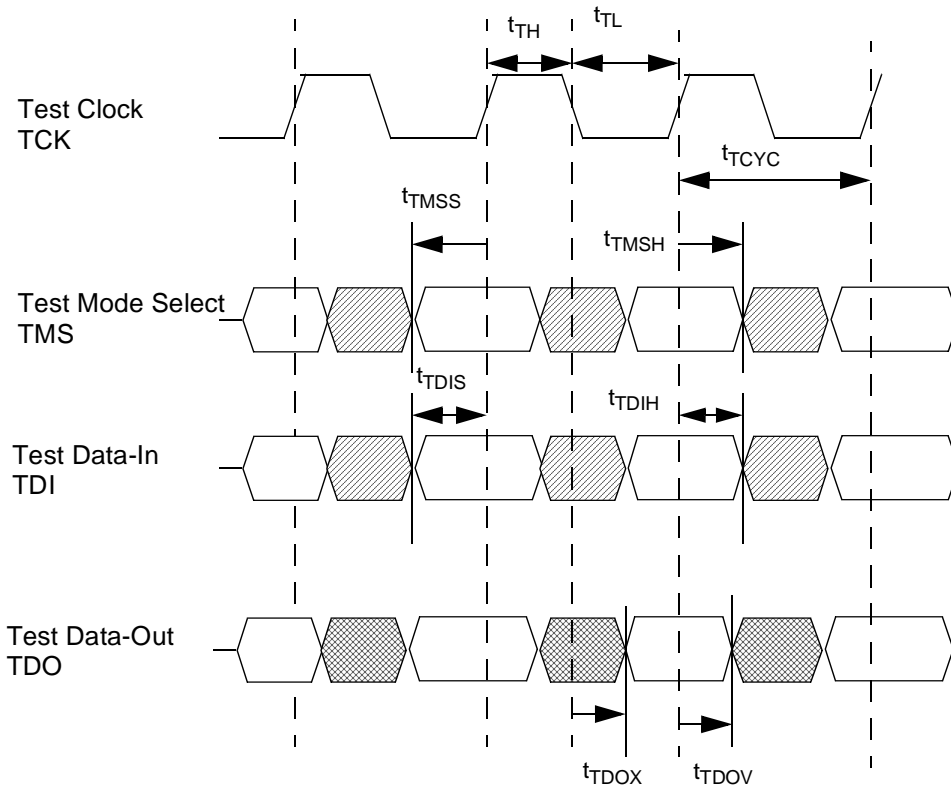
**Notes:**

6.  $t_{CS}$  and  $t_{CH}$  refer to the set-up and hold time requirements of latching data from the boundary scan register.
7. Test conditions are specified using the load in TAP AC test conditions.  $t_R/t_F = 1$  ns.

**TAP Timing and Test Conditions**



(a)





**Identification Register Definitions**

Instruction Field	Value	Description
Revision Number (31:28)	TBD	Reserved for version number
Device Depth (27:23)	TBD	Defines depth of SRAM
Device Width (22:18)	TBD	Defines with of the SRAM
Cypress Device ID (17:12)	TBD	Reserved for future use
Cypress JEDEC ID (11:1)	TBD	Allows unique identification of SRAM vendor
ID Register Presence (0)	TBD	Indicate the presence of an ID register

**Scan Register Sizes**

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	TBD

**Identification Codes**

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.



**Boundary Scan Order**

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	TBD	TBD	36	TBD	TBD
2	TBD	TBD	37	TBD	TBD
3	TBD	TBD	38	TBD	TBD
4	TBD	TBD	39	TBD	TBD
5	TBD	TBD	40	TBD	TBD
6	TBD	TBD	41	TBD	TBD
7	TBD	TBD	42	TBD	TBD
8	TBD	TBD	43	TBD	TBD
9	TBD	TBD	44	TBD	TBD
10	TBD	TBD	45	TBD	TBD
11	TBD	TBD	46	TBD	TBD
12	TBD	TBD	47	TBD	TBD
13	TBD	TBD	48	TBD	TBD
14	TBD	TBD	49	TBD	TBD
15	TBD	TBD	50	TBD	TBD
16	TBD	TBD	51	TBD	TBD
17	TBD	TBD	52	TBD	TBD
18	TBD	TBD	53	TBD	TBD
19	TBD	TBD	54	TBD	TBD
20	TBD	TBD	55	TBD	TBD
21	TBD	TBD	56	TBD	TBD
22	TBD	TBD	57	TBD	TBD
23	TBD	TBD	58	TBD	TBD
24	TBD	TBD	59	TBD	TBD
25	TBD	TBD	60	TBD	TBD
26	TBD	TBD	61	TBD	TBD
27	TBD	TBD	62	TBD	TBD
28	TBD	TBD	63	TBD	TBD
29	TBD	TBD	64	TBD	TBD
30	TBD	TBD	65	TBD	TBD
31	TBD	TBD	66	TBD	TBD
32	TBD	TBD	67	TBD	TBD
33	TBD	TBD	68	TBD	TBD
34	TBD	TBD	69	TBD	TBD
35	TBD	TBD	70	TBD	TBD

**Boundary Scan Order**

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
71	TBD	TBD		TBD	TBD
72	TBD	TBD		TBD	TBD
73	TBD	TBD		TBD	TBD
74	TBD	TBD		TBD	TBD
75	TBD	TBD		TBD	TBD
76	TBD	TBD		TBD	TBD
77	TBD	TBD		TBD	TBD
78	TBD	TBD		TBD	TBD
79	TBD	TBD		TBD	TBD
80	TBD	TBD		TBD	TBD
81	TBD	TBD		TBD	TBD
82	TBD	TBD		TBD	TBD
83	TBD	TBD		TBD	TBD
84	TBD	TBD		TBD	TBD
85	TBD	TBD		TBD	TBD
86	TBD	TBD		TBD	TBD
87	TBD	TBD		TBD	TBD
88	TBD	TBD		TBD	TBD
89	TBD	TBD		TBD	TBD
90	TBD	TBD		TBD	TBD
91	TBD	TBD		TBD	TBD
92	TBD	TBD		TBD	TBD
93	TBD	TBD		TBD	TBD
94	TBD	TBD		TBD	TBD
95	TBD	TBD		TBD	TBD
96	TBD	TBD		TBD	TBD
97	TBD	TBD		TBD	TBD
98	TBD	TBD		TBD	TBD
99	TBD	TBD		TBD	TBD



**PRELIMINARY**

**CY7C1361V25  
CY7C1363V25  
CY7C1365V25**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on V<sub>DD</sub> Relative to GND..... -0.5V to +3.6V  
 DC Voltage Applied to Outputs in High Z State<sup>[9]</sup>..... -0.5V to V<sub>DDQ</sub> + 0.5V

DC Input Voltage<sup>[9]</sup> ..... -0.5V to V<sub>DDQ</sub> + 0.5V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[8]</sup>	V <sub>DD</sub> /V <sub>DDQ</sub>
Com'l	0°C to +70°C	2.5V ± 5%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V <sub>DD</sub>	Power Supply Voltage		2.375	2.625	V	
V <sub>DDQ</sub>	I/O Supply Voltage		2.375	2.625	V	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.0		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 1.0 mA		0.2	V	
V <sub>IH</sub>	Input HIGH Voltage		1.7	V <sub>DD</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[9]</sup>		-0.3	0.7	V	
I <sub>X</sub>	Input Load Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	mA	
	Input Current of MODE		-30	30	mA	
	Input Current of ZZ	Input = V <sub>SS</sub> Input = V <sub>DDQ</sub>	-5	30	mA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-1.0	1.0	mA	
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		350	mA
			8.8-ns cycle, 113 MHz		300	mA
			10-ns cycle, 100 MHz		260	mA
			12.5-ns cycle, 80 MHz		210	mA
I <sub>SB1</sub>	Automatic CS Power-Down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		90	mA
			8.8-ns cycle, 113 MHz		80	mA
			10-ns cycle, 100 MHz		70	mA
			12.5-ns cycle, 80 MHz		65	mA
I <sub>SB2</sub>	Automatic CS Power-Down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = 0		10	mA	
I <sub>SB3</sub>	Automatic CS Power-Down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		45	mA
			8.8-ns cycle, 113 MHz		40	mA
			10-ns cycle, 100 MHz		35	mA
			12.5-ns cycle, 80 MHz		30	mA
I <sub>SB4</sub>	Automatic CS Power-Down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0		25	mA	

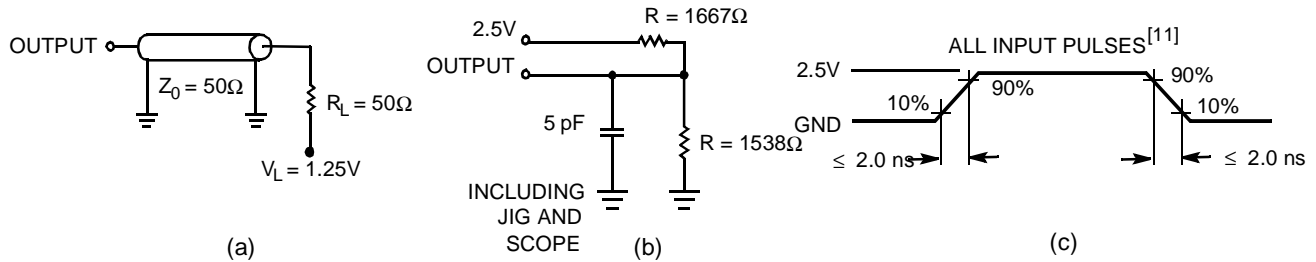
Shaded areas contain advance information.

**Notes:**

- 8. T<sub>A</sub> is the case temperature.
- 9. Minimum voltage equals -2.0V for pulse durations of less than 20 ns.

**Capacitance<sup>[10]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = V_{DDQ} = 2.5\text{V}$	4	pF
$C_{CLK}$	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

**AC Test Loads and Waveforms**

**Notes:**

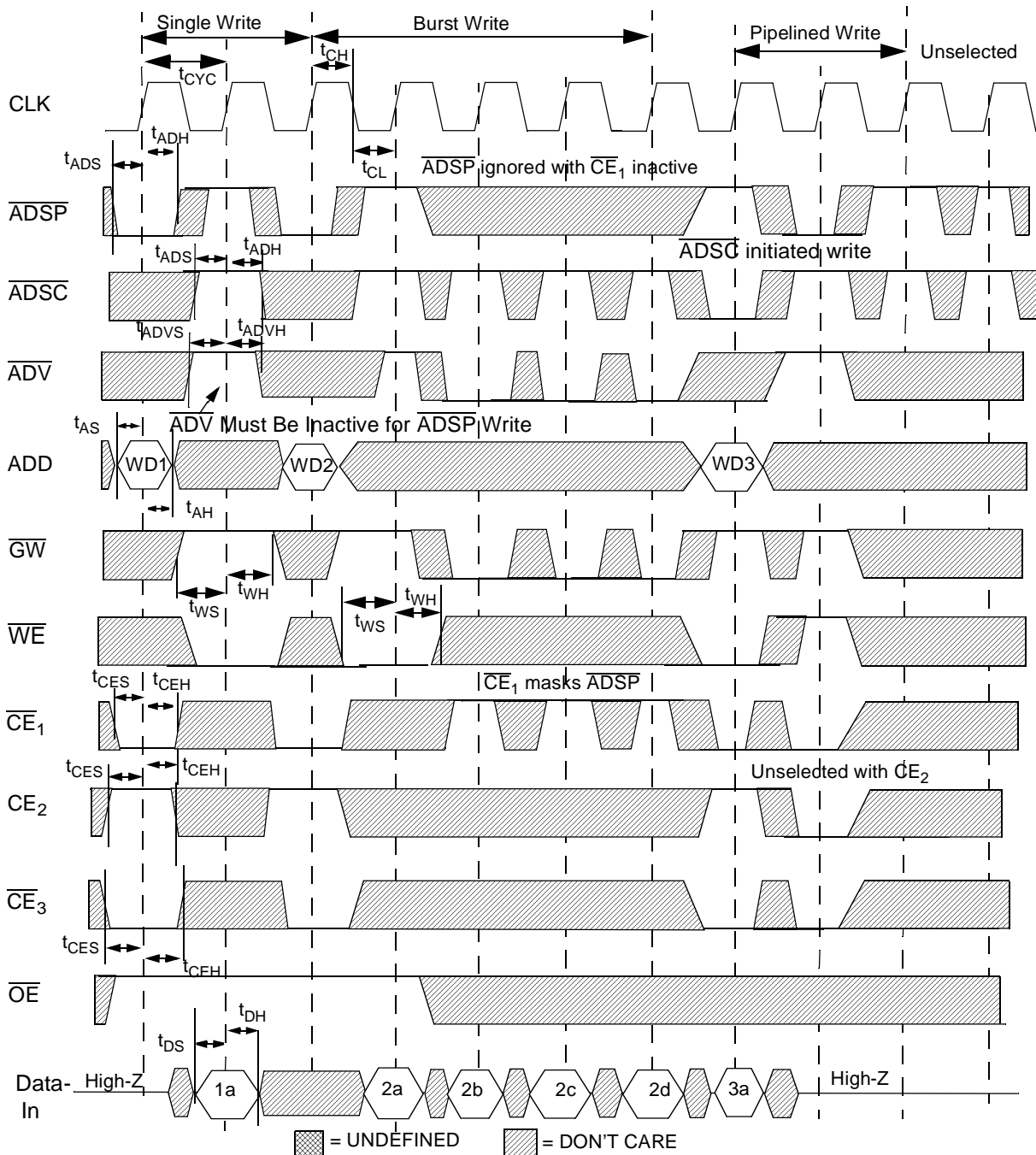
10. Tested initially and after any design or process changes that may affect these parameters.  
 11. Input waveform should have a slew rate of  $\geq 1\text{ V/ns}$ .

**Switching Characteristics** Over the Operating Range<sup>[12, 13, 14]</sup>

Parameter	Description	-133		-117		-100		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Clock Cycle Time	7.5		8.5		10.0		12.5		ns
t <sub>CH</sub>	Clock HIGH	1.9		3.0		3.2		4.0		ns
t <sub>CL</sub>	Clock LOW	1.9		3.0		3.2		4.0		ns
t <sub>AS</sub>	Address Set-Up Before CLK Rise	1.5		2		2		2.0		ns
t <sub>AH</sub>	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>CO</sub>	Data Output Valid After CLK Rise		6.5		7.5		8.5		10.0	ns
t <sub>DOH</sub>	Data Output Hold After CLK Rise	1.5		1.5		1.5		1.5		ns
t <sub>ADS</sub>	ADSP, ADSC Set-Up Before CLK Rise	1.5		2		2		2.0		ns
t <sub>ADH</sub>	ADSP, ADSC Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>WES</sub>	BWE, GW, BW[3:0] Set-Up Before CLK Rise	1.5		2		2		2.0		ns
t <sub>WEH</sub>	BWE, GW, BW[3:0] Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>ADVS</sub>	ADV Set-Up Before CLK Rise	1.5		2.0		2.0		2.0		ns
t <sub>ADVH</sub>	ADV Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>DS</sub>	Data Input Set-Up Before CLK Rise	1.5		2.0		2.0		2.0		ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>CES</sub>	Chip enable Set-Up	1.5		2		2		2.0		ns
t <sub>CEH</sub>	Chip enable Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t <sub>CHZ</sub>	Clock to High-Z <sup>[13, 14, 15]</sup>	0	3.5	0	3.5	0	3.5	0	3.5	ns
t <sub>CLZ</sub>	Clock to Low-Z <sup>[13, 14, 15]</sup>	0		0		0		0		ns
t <sub>EOHZ</sub>	OE HIGH to Output High-Z <sup>[13, 14]</sup>		3.5		3.5		3.5		3.5	ns
t <sub>EOLZ</sub>	OE LOW to Output Low-Z <sup>[13, 14]</sup>	0		0		0		0		ns
t <sub>EOV</sub>	OE LOW to Output Valid <sup>[13, 14]</sup>		3.5		4.2		5.0		5.0	ns

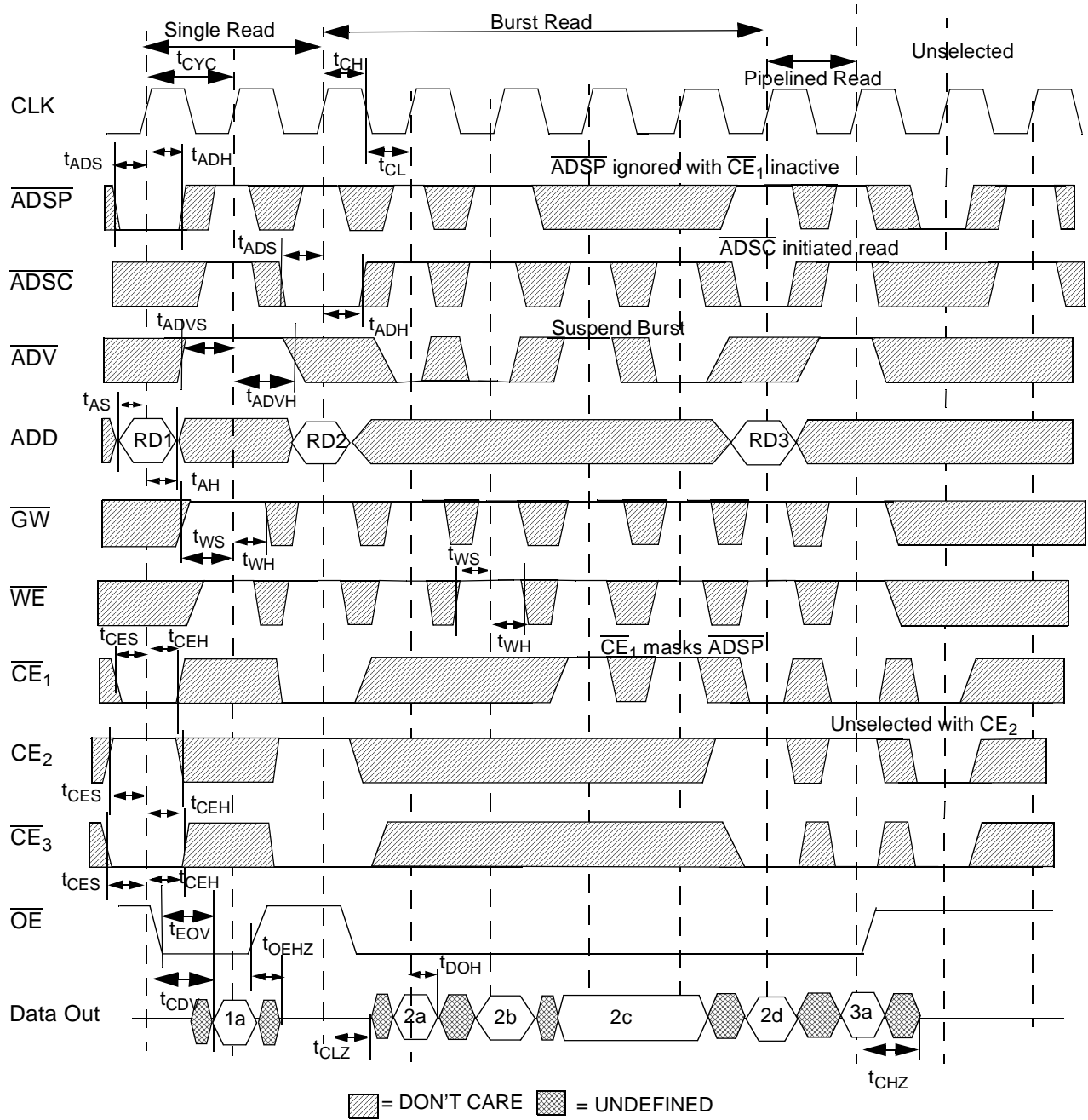
**Notes:**

12. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and load capacitance. Shown in (a), (b) and (c) of AC test loads.
13. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OEV</sub>, t<sub>EOLZ</sub>, and t<sub>EOHZ</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any given voltage and temperature, t<sub>CHZ</sub> (max.) is less than t<sub>CLZ</sub> (min.).
15. This parameter is sampled and not 100% tested.

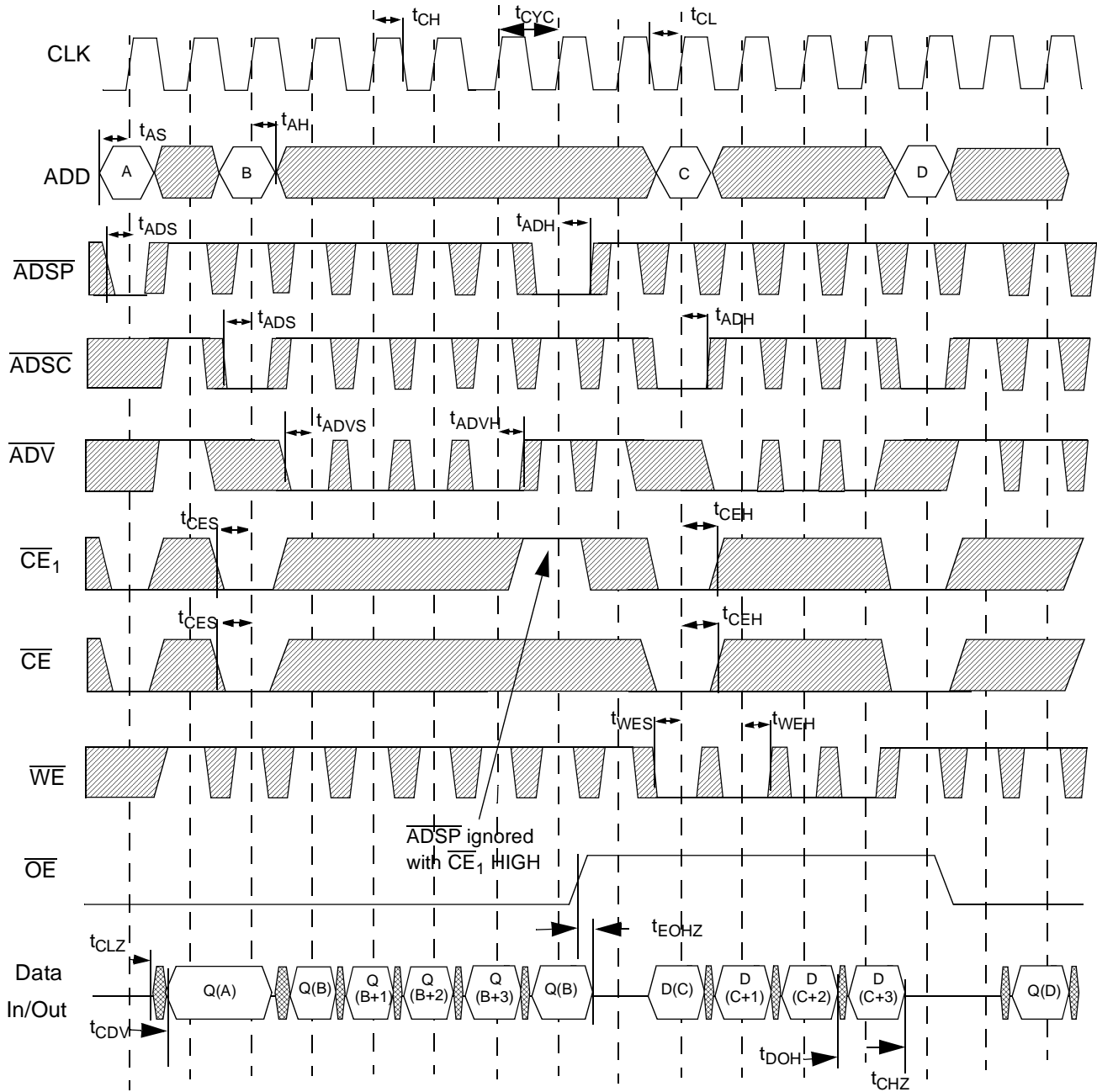
**Timing Diagrams**
**Write Cycle Timing<sup>[16, 17]</sup>**

**Notes:**

- 16.  $\overline{WE}$  is the combination of  $\overline{BWE}$ ,  $\overline{BW}_x$ , and  $\overline{GW}$  to define a write cycle (see Write Cycle Description table).
- 17.  $WD_x$  stands for Write Data to Address X.

**Timing Diagrams** (continued)

**Read Cycle Timing**<sup>[16, 18]</sup>

**Note:**

18. RDx stands for Read Data from Address X.

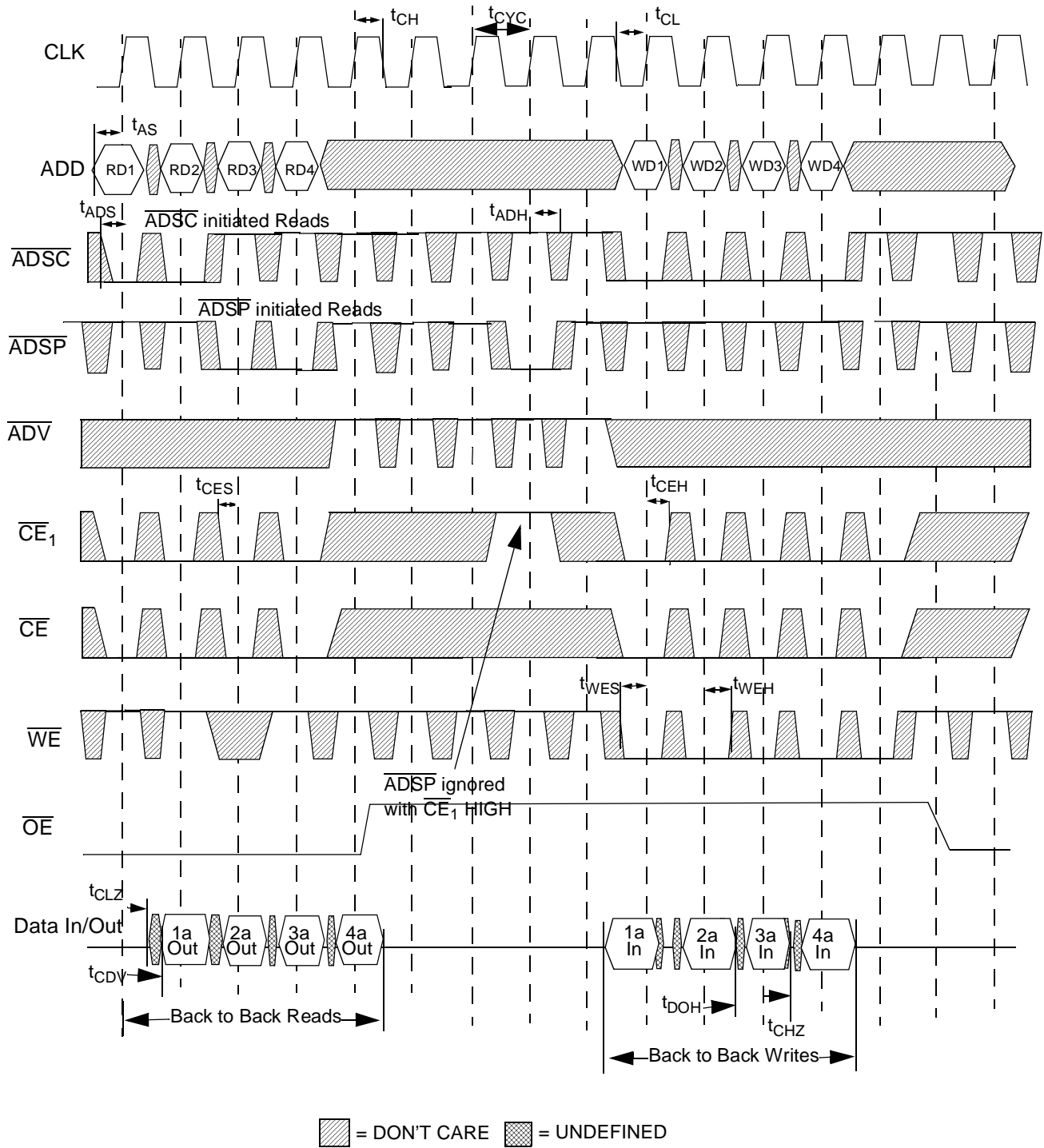
**Timing Diagrams (continued)**
**Read/Write Timing**


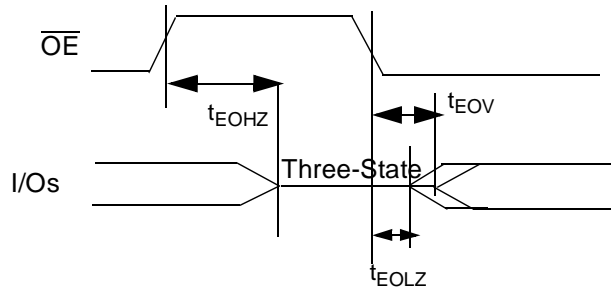
Device originally deselected

$\overline{WE}$  is the combination of  $\overline{BWE}$ ,  $\overline{BW}_x$ , and  $\overline{GW}$  to define a write cycle (see Write Cycle Description table).  
 $\overline{CE}$  is the combination of  $CE_2$  and  $\overline{CE}_3$ . All chip selects need to be active in order to select the device. RAX stands for Read Address X, WAX stands for Write Address X, DX stands for Data-in X, Qx stands for Data-out X.

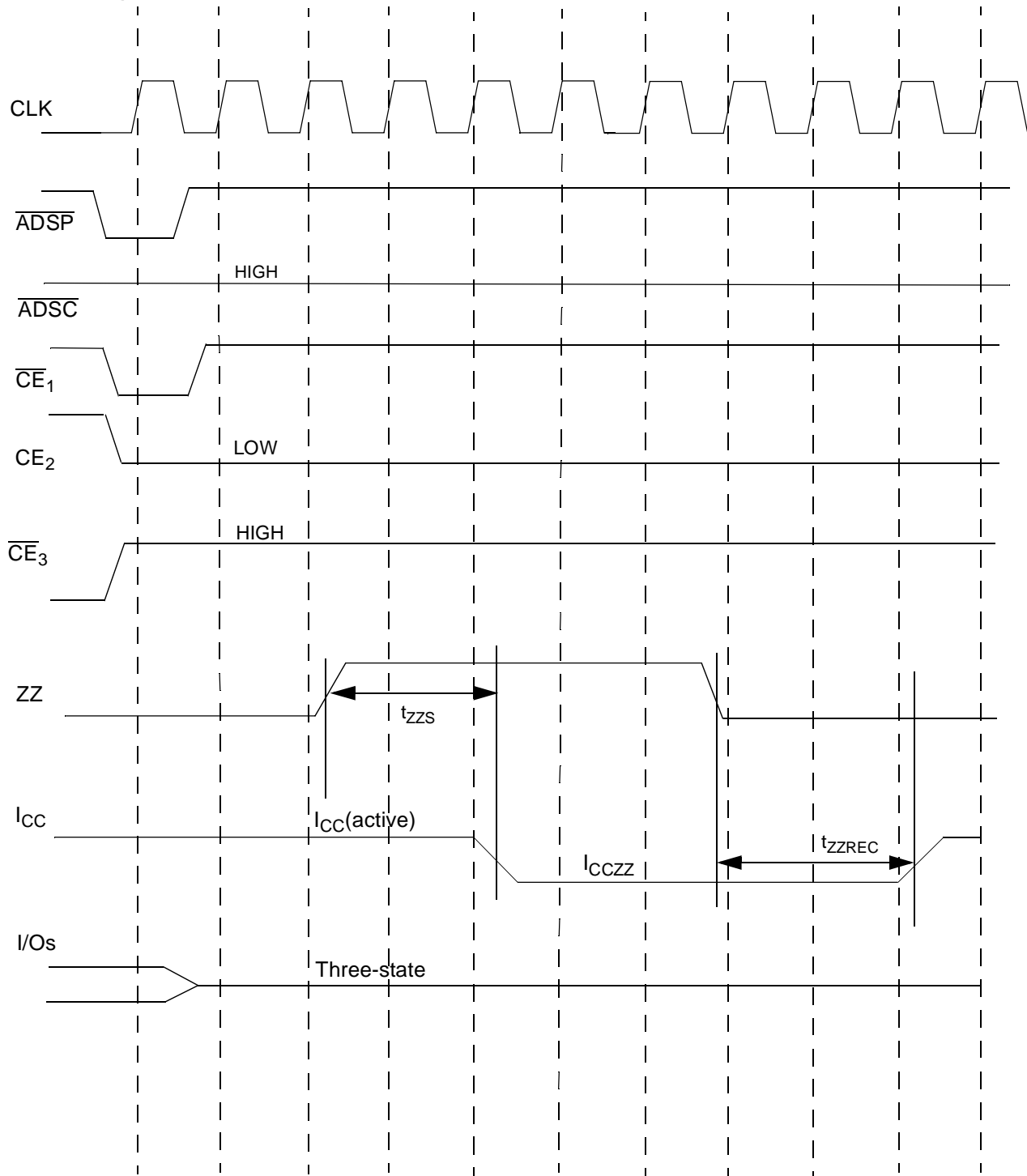
▨ = DON'T CARE    ▩ = UNDEFINED



**Timing Diagrams (continued)**
**Pipeline Timing**


**Timing Diagrams** (continued)**OE Switching Waveforms**

**Timing Diagrams** (continued)

**ZZ Mode Timing** [19, 20]

**Notes:**

19. Device must be deselected when entering ZZ mode. See Cycle Description for all possible signal conditions to deselect the device.
20. I/Os are in three-state when exiting ZZ sleep mode.



**PRELIMINARY**

**CY7C1361V25  
CY7C1363V25  
CY7C1365V25**

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1361V25-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1361V25-117AC			
100	CY7C1361V25-100AC			
80	CY7C1361V25-80AC			
133	CY7C1363V25-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1363V25-117AC			
100	CY7C1363V25-100AC			
80	CY7C1363V25-80AC			
133	CY7C1365V25-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1365V25-117AC			
100	CY7C1365V25-100AC			
80	CY7C1365V25-80AC			
133	CY7C1361V25-133BGC	BG119	119-Ball BGA	Commercial
117	CY7C1361V25-117BGC			
100	CY7C1361V25-100BGC			
80	CY7C1361V25-80BGC			
133	CY7C1363V25-133BGC	BG119	119-Ball BGA	Commercial
117	CY7C1363V25-117BGC			
100	CY7C1363V25-100BGC			
80	CY7C1363V25-80BGC			
133	CY7C1365V25-133BGC	BG119	119-Ball BGA	Commercial
117	CY7C1365V25-117BGC			
100	CY7C1365V25-100BGC			
80	CY7C1365V25-80BGC			

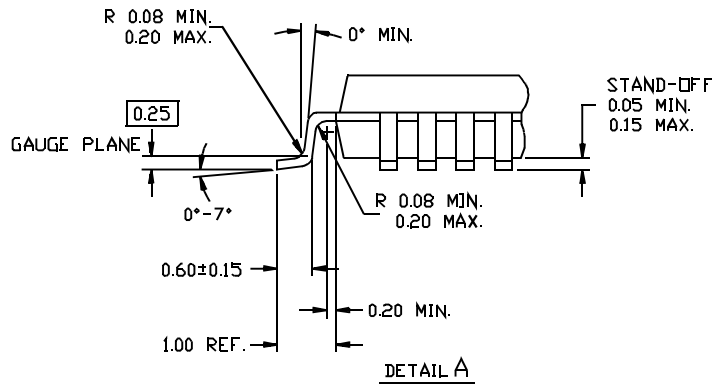
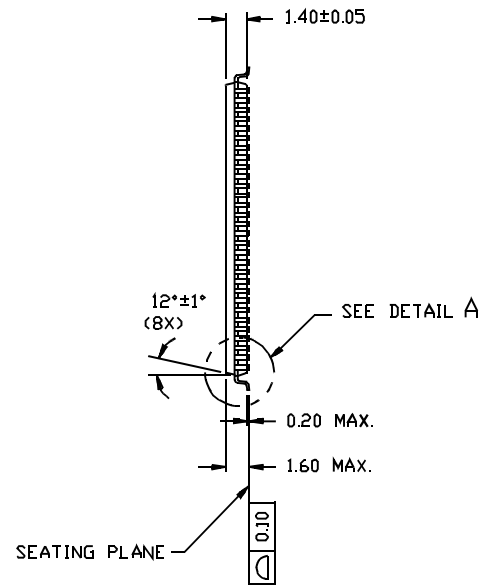
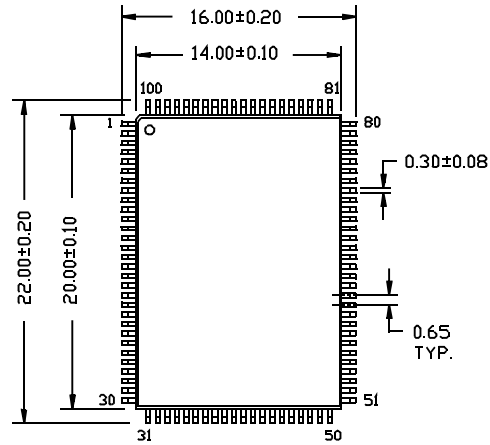
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**Package Diagrams**

**100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101**

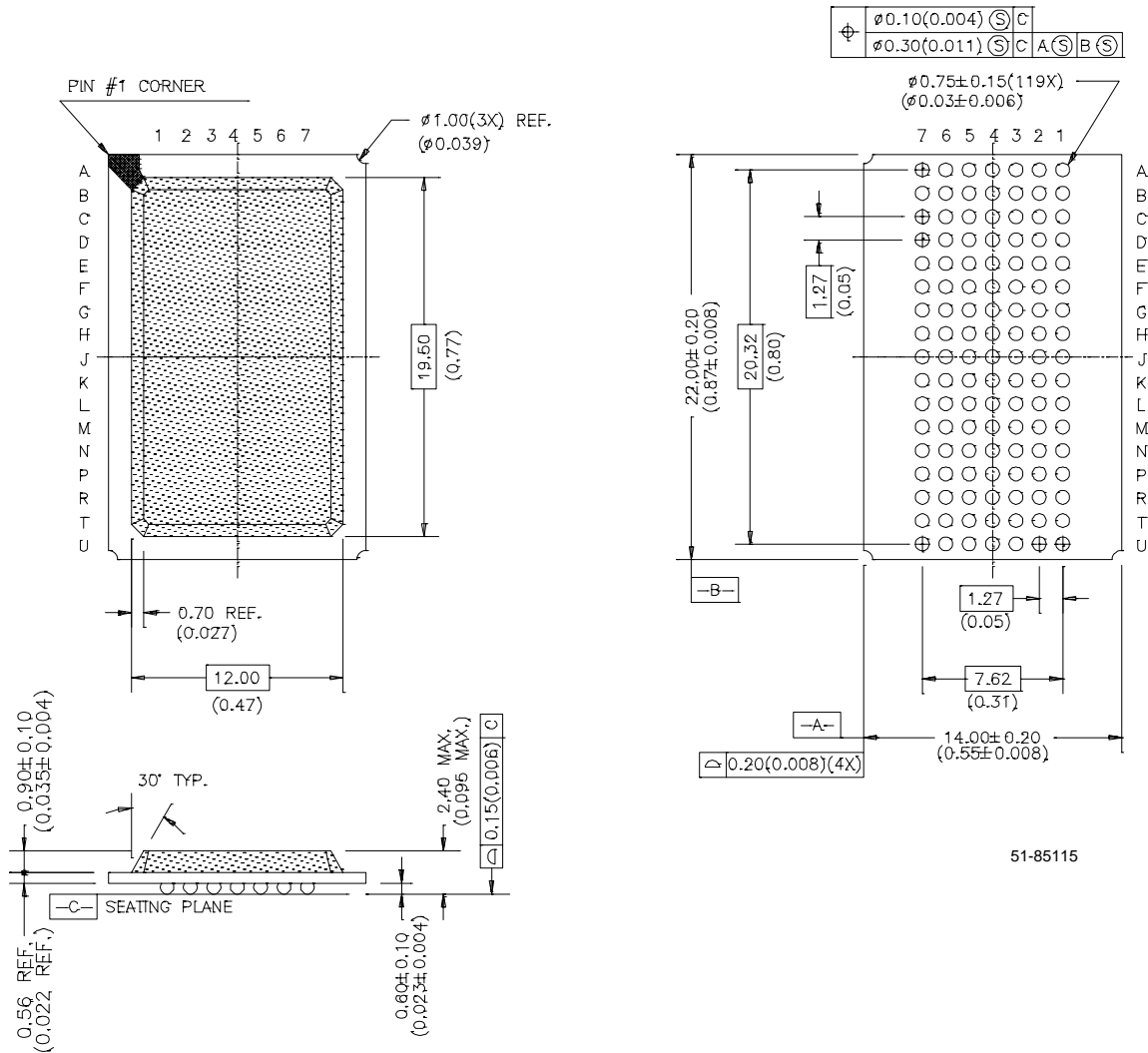
DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

**Package Diagrams (continued)**
**119-Lead FBGA (14 x 22 x 2.4 mm) BG119**

DIMENSION IN MILLIMETERS (INCHES)



51-85115

**Revision History**

Document Title: CY7C1361V25/CY7C1363V25/CY7C1365V25				
Document Number: 38-00761				
REV.	ECN NO.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
**	2561	4/29/99	SKX	1. New Data Sheet
*A	2684	9/10/99	SKX	1. Updated the BGA pinout 2. Added revision history