CYPRESS SEMICONDUCTOR

CY7C183
CY7C184

2 x 4096 x 16 Cache RAM

Features

- **Pin-programmable into direct-mapped or two-way set-associative format**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 20 ns**
- **Common I/O**
- **Internal address latch**
- **TTL-compatible inputs and outputs**
- **Compatible with Intel 82385 Cache Controller**

Functional Description

The CY7C183 and CY7C184 are high-performance monolithic CMOS static RAMs that contain 128 Kbits organized into either two two-way set-associative blocks of 4K x 16 RAM or one directly mapped 8K x 16-bit RAM.

They are designed specifically for use with the Intel 82385 Cache Controller, and their addresses are latched on the falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The CY7C183 has all address bits latched by the ALE signal except A_{12}. This signal bypasses the latch and has a faster access time. All address bits are latched by the ALE signal in the CY7C184. The mode pin controls whether the device is configured as a direct-mapped 8K x 16 RAM or a two-way set-associative 2 x 4K x 16 RAM. When mode is HIGH, the device is placed in the two-way mode. In this mode, the upper address bit, A_{12}, is a "don't care" and is externally wired to ground. When mode is LOW, the device is placed in the direct mode.

Writing is accomplished in the two-way mode by taking $\overline{CE}$ LOW and by driving the respective $\overline{CS}_x$ and $\overline{WE}_x$ signals LOW. $\overline{CS}_0$ enables bits D_0-D_7 while $\overline{CS}_1$ enables bits D_8-D_{15}. $\overline{WE}_A$ and $\overline{WE}_B$ enable cache banks A and B, respectively, to receive the data present on the data bus. $\overline{OE}_A$ and $\overline{OE}_B$ similarly enable cache banks A and B, respectively, to drive the data bus.

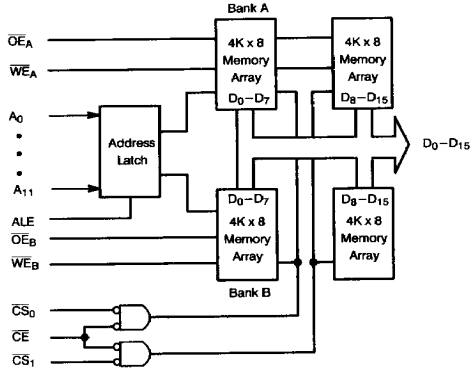
Writing is accomplished in the direct mode by tying $\overline{WE}_A$ and $\overline{WE}_B$ together externally, and using them as a single write enable.

Reading is accomplished in the two-way mode by taking $\overline{CE}$ LOW, forcing the appropriate $\overline{OE}_x$ and $\overline{CS}_x$ signals LOW and the $\overline{WE}_x$ signal HIGH. The contents of the memory location specified on the address pins will appear on the 16 outputs. Activation of $\overline{OE}_A$ and $\overline{OE}_B$ simultaneously will cause both banks to be deselected.

Reading is accomplished in the direct mode by tying $\overline{OE}_A$ and $\overline{OE}_B$ together externally and using them as a single output enable.

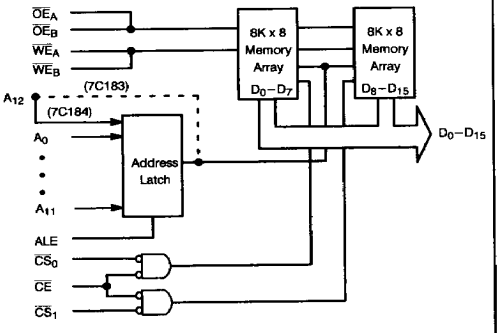
Logic Block Diagrams

Two-Way Set Associative (Mode = HIGH)



C183-1

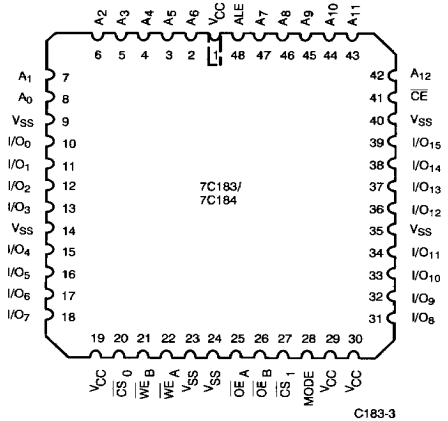
Direct Map (Mode = LOW)



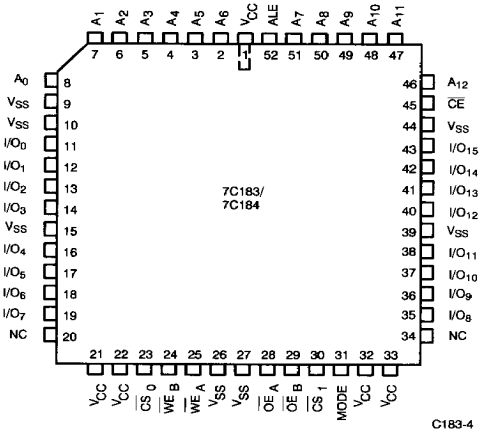
C183-2

Pin Diagrams

LCC
Top View



PLCC
Top View



Selection Guide

		7C183–20 7C184–20	7C183–25 7C184–25	7C183-35 7C184-35	7C183-45 7C184-45
Maximum Address Access Time (ns)	Commercial	20	25	35	45
	Military			35	45
Maximum Output Enable Access Time (ns)	Commercial	8	10	14	16
	Military			14	16
Maximum Operating Current (mA)	Commercial	250	220	170	140
	Military			200	160

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage[1] ..... +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL–STD–883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = – 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3]

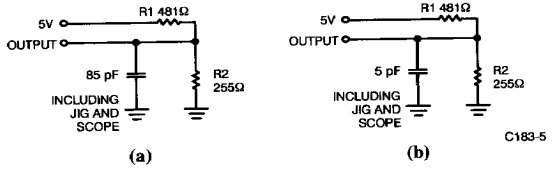
Parameters	Description	Test Conditions		7C183-20 7C184-20 Min.	7C183-20 7C184-20 Max.	7C183-25 7C184-25 Min.	7C183-25 7C184-25 Max.	7C183-35 7C184-35 Min.	7C183-35 7C184-35 Max.	7C183-45 7C184-45 Min.	7C183-45 7C184-45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA Read Cycle[5] Duty Cycle = 45%	Com'l		250		220		170		140	mA
			Mil						200		160	

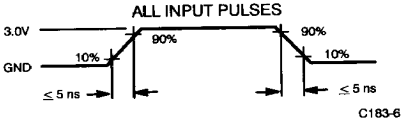
Shaded area contains preliminary information.

Capacitance[6]

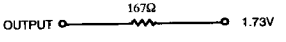
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. At a given duty cycle, Write Cycle I_{CC} is equal to 1.4 times Read Cycle I_{CC}.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range[3,7]

Parameters	Description	7C183–20 7C184–20		7C183–25 7C184–25		7C183–35 7C184–35		7C183–45 7C184–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[8]										
t_{RC}	Read Cycle Time	20		25		35		45		ns
t_{AA}	Address to Data Valid		20		25		35		45	ns
$t_{AA\ A12}$[9]	Address to Data Valid A_{12}		15		17		25		35	ns
t_{CE}	Chip Enable to Data Valid		10		12		15		20	ns
t_{CS}	Chip Select to Data Valid		10		12		15		20	ns
t_{OE}	$\overline{OE}_x$ LOW to Data Valid		8		10		14		16	ns
t_{OHA}	Output Hold from AddressChange	3		3		3		3		ns
t_{OHL}	Output Hold from ALE HIGH	3		3		3		3		ns
t_{LZCE}	$\overline{CE}$, $\overline{CS}_x$ LOW to Low Z	3		3		3		3		ns
t_{LZOE}	$\overline{OE}_x$ LOW to Low Z	0		0		0		0		ns
t_{HZCE}	$\overline{CE}$, $\overline{CS}_x$ HIGH to High Z		12		15		25		30	ns
t_{HZOE}	$\overline{OE}_x$ HIGH to High Z		8		9		10		12	ns
t_{PALE}	ALE Pulse Width	8		8		10		12		ns
t_{SALE}	Address Set-Up to ALE Low	3		4		6		8		ns
t_{HALE}	Address Hold from ALE Low	4		4		4		4		ns
WRITE CYCLE[10]										
t_{WC}	Write Cycle Time	20		25		35		45		ns
t_{AW}	Address Set-Up to Write End	15		20		30		40		ns
t_{SCE}	Chip Enable to Write End	15		20		25		30		ns
t_{SCS}	Chip Select to Write End	15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	8		10		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{PWE}	Write Enable Pulse Width	15		20		25		30		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}_x$ HIGH to Low Z	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		12		15		15		20	ns
t_{PALE}	ALE Pulse Width	8		8		10		12		ns
t_{SALE}	Address Set-Up to ALE Low	4		4		6		8		ns
t_{HALE}	Address Hold from ALE Low	4		4		4		4		ns

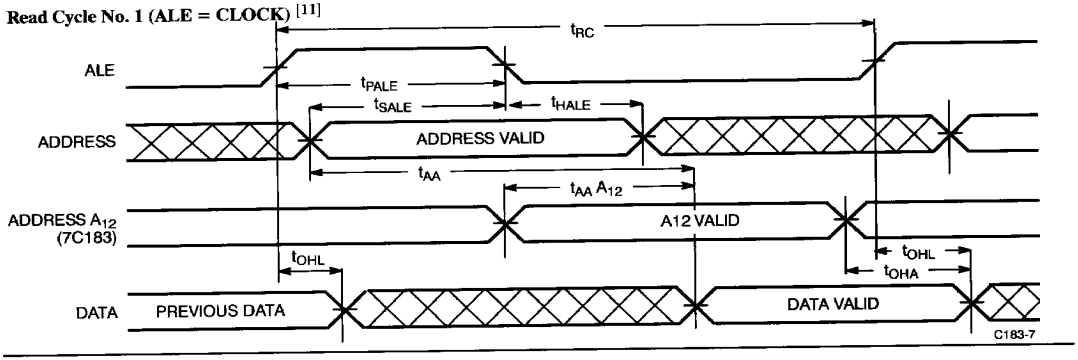
Shaded area contains preliminary information.

Notes:

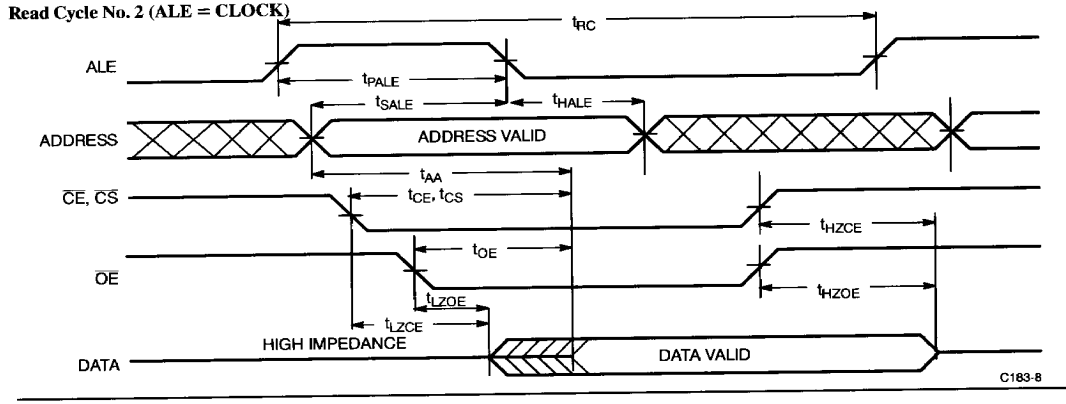
8. Both $\overline{WE}_A$ and $\overline{WE}_B$ must be HIGH for read cycle.
9. CY7C183 only.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$, $\overline{CS}_x$, and $\overline{WE}_x$. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

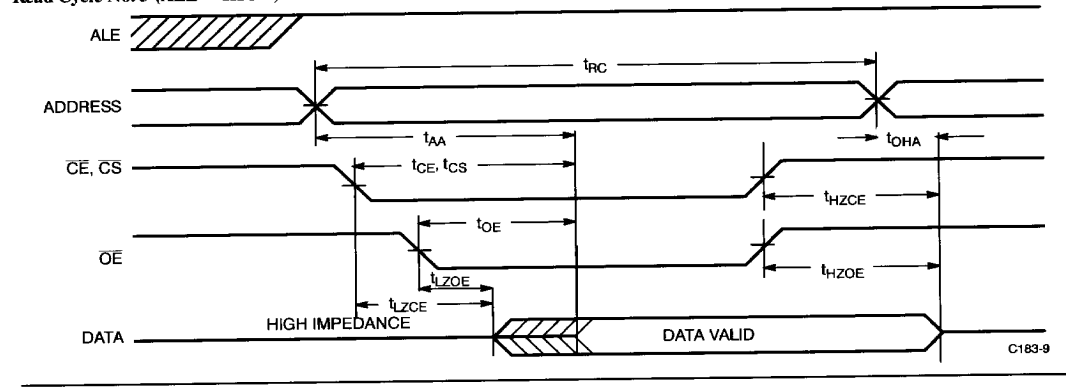
Read Cycle No. 1 (ALE = CLOCK) [11]



Read Cycle No. 2 (ALE = CLOCK)



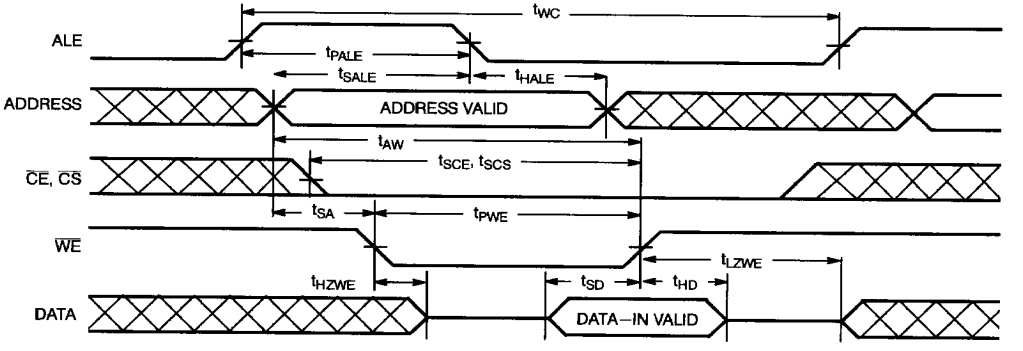
Read Cycle No. 3 (ALE = HIGH) [12, 13]



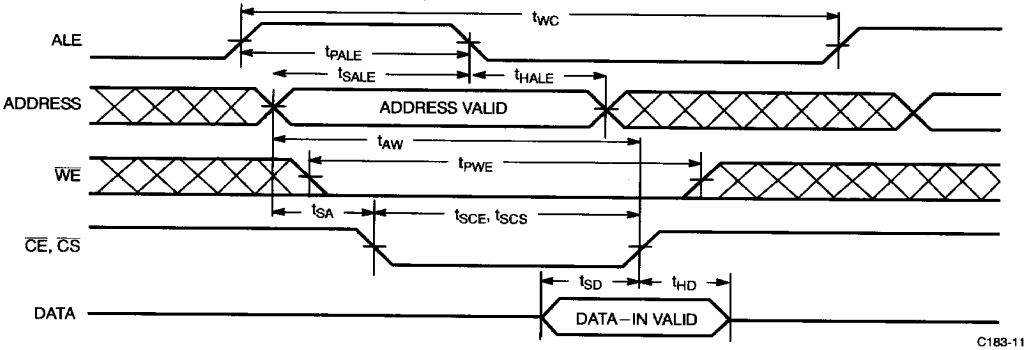
Notes:
11. Device is continuously selected, $\overline{CE}$ and $\overline{CS}$ are LOW.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

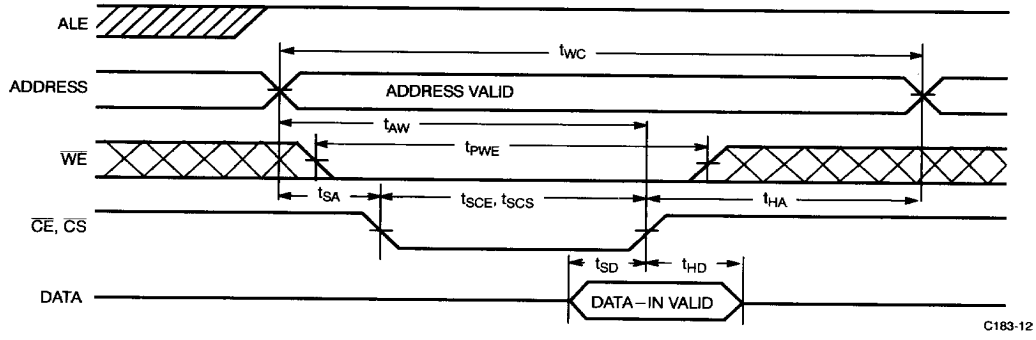
Write Cycle No. 1 (ALE = CLOCK, $\overline{WE}$ Controlled) [14]



Write Cycle No. 2 (ALE = CLOCK, $\overline{CE}$/$\overline{CS}$ Controlled) [14]



Write Cycle No. 3 (ALE = HIGH, $\overline{CE}$/$\overline{CS}$ Controlled) [14]



Note:
14. $\overline{OE}$ is deselected (HIGH).

Truth Tables

Two-Way Mode (Mode = HIGH)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{OE_A}$	$\overline{OE_B}$	$\overline{WE_A}$	$\overline{WE_B}$	Operation
H	X	X	X	X	X	X	Outputs High Z, Write Disabled
L	H	H	X	X	X	X	Outputs High Z, Write Disabled
X	X	X	H	H	X	X	Outputs High Z
X	X	X	L	L	X	X	Outputs High Z
L	L	H	L	H	H	H	Read $I/O_0-I/O_7$ Bank A
L	L	H	H	L	H	H	Read $I/O_0-I/O_7$ Bank B
L	H	L	L	H	H	H	Read $I/O_8-I/O_{15}$ Bank A
L	H	L	H	L	H	H	Read $I/O_8-I/O_{15}$ Bank B
L	L	L	L	H	H	H	Read $I/O_0-I/O_{15}$ Bank A
L	L	L	H	L	H	H	Read $I/O_0-I/O_{15}$ Bank B
L	L	H	X	X	L	H	Write $I/O_0-I/O_7$ Bank A
L	L	H	X	X	H	L	Write $I/O_0-I/O_7$ Bank B
L	H	L	X	X	L	H	Write $I/O_8-I/O_{15}$ Bank A
L	H	L	X	X	H	L	Write $I/O_8-I/O_{15}$ Bank B
L	L	L	X	X	L	H	Write $I/O_0-I/O_{15}$ Bank A
L	L	L	X	X	H	L	Write $I/O_0-I/O_{15}$ Bank B
L	L	H	X	X	L	L	Write $I/O_0-I/O_7$ Banks A and B
L	H	L	X	X	L	L	Write $I/O_8-I/O_{15}$ Banks A and B
L	L	L	X	X	L	L	Write $I/O_{20}-I/O_{15}$ Banks A and B

Direct Mode (Mode = LOW)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{OE_A}$	$\overline{OE_B}$	$\overline{WE_A}$	$\overline{WE_B}$	Operation
H	X	X	X	X	X	X	Outputs High Z, Write Disabled
L	H	H	X	X	X	X	Outputs High Z, Write Disabled
X	X	X	H	H	X	X	Outputs High Z
L	L	H	L	L	H	H	Read $I/O_0-I/O_7$
L	H	L	L	L	H	H	Read $I/O_8-I/O_{15}$
L	L	L	L	L	H	H	Read $I/O_0-I/O_{15}$
L	L	H	X	X	L	L	Write $I/O_0-I/O_7$
L	H	L	X	X	L	L	Write $I/O_8-I/O_{15}$
L	L	L	X	X	L	L	Write $I/O_0-I/O_{15}$

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C183–20JC	J69	Commercial
25	CY7C183–25JC	J69	Commercial
35	CY7C183–35JC	J69	Commercial
	CY7C183–35LMB	L68	Military
45	CY7C183–45JC	J69	Commercial
	CY7C183–45LMB	L68	Military

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C184–20JC	J69	Commercial
25	CY7C184–25JC	J69	Commercial
35	CY7C184–35JC	J69	Commercial
	CY7C184–35LMB	L68	Military
45	CY7C184–45JC	J69	Commercial
	CY7C184–45LMB	L68	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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