SHARP ®

Integrated Circuits Group

ID244G01

8MB Flash Memory Card

(Model No.: ID244G01)

Spec No.: EL094092A

Issue Date: October 7, 1997

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- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

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● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. General Descriptions

The SHARP ID244G01, which panel design is SHARP standard, is a 8MB Flash Memory PC Card conforms to PCMCIA Release 2.0 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

2.1	Type	8MB Flash Memory Card (Conforms to PCMCIA Rel.2.0)
2.2	Memory Capacity	
	Common Memory	8M words×8 bits or 4M words×16 bits
	Attribute Memory	EEPROM Model 2k words×8 bits read/write

Note) We have another type of attribute memory as follows,
   No EEPROM Model. (5 words×8 bits read only in card's control circuit)
   Sample card name: ID244G02. Customers can choose one model from two.

2.3	Supply Voltage	
	Read Cycle	$Vcc=5\pm0.5V$, Vpp1, Vpp2=0~1.5V
	Read/Program/Erase Cycle	$Vcc=5\pm0.5V$, Vpp1, Vpp2=5.0V±0.5V/12.0V±0.6V
2.4	Erase Unit	Block(64k bytes/byte access, 128k bytes/word access)
2.5	Program/Erase Cycles	100,000 cycles
2.6	Interface	Parallel I/O Interface
2.7	Function Table	See Function Table in page.6
2.8	External Dimensions	54×85.6×3.3 mm
2.9	Pin Connections	See Pin Connections in page.4
2.10	Type of Connector	Conforms to PCMCIA Rel.2.0 Card Use Connector (JC20-J68S-NB3 by JAE, FCN-568J068-G/0 by Fujitsu or ICM-C68S-TS13-5035A by JST)
2.11	Average Weight	30g
2.12	Operating Temp Range	0 to 60℃
2.13	Storage Temp Range	-20 to 65℃
2.14	External Appearance	External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales.
2.15	Manufacturer's Code	The manufacturer's code shall be printed on the memory card directly or on the seal which is then attached to the memory card.
2.16	Brand Name	The user's brand name will be used.
2.17	Not designed or rated radiation hardened.	

3. Block Diagram

Card
Connector

CARD CONTROL CIRCUIT

D0~D15

A0~A22

$\overline{REG}$

$\overline{CE1}$

$\overline{CE2}$

$\overline{WE}$

$\overline{OE}$

$\overline{CMCS0}$~$\overline{CMCS3}$

D8~D15

D0~D7

A1~A20

$\overline{MWE0}$

$\overline{MWE1}$

$\overline{MOE}$

RY/$\overline{BY}$

AND

8Mbit Flash Memory
VPP2 VCC VCC
VPP VCC $\overline{PWD}$
D0~D7 $\overline{CE}$
A0~A19 $\overline{WE}$
RY/$\overline{BY}$ $\overline{OE}$
GND

8Mbit Flash Memory
VPP1 VCC VCC
VPP VCC $\overline{PWD}$
D0~D7 $\overline{CE}$
A0~A19 $\overline{WE}$
RY/$\overline{BY}$ $\overline{OE}$
GND

8Mbit Flash Memory
VPP2 VCC VCC
VPP VCC $\overline{PWD}$
D0~D7 $\overline{CE}$
A0~A19 $\overline{WE}$
RY/$\overline{BY}$ $\overline{OE}$
GND

8Mbit Flash Memory
VPP1 VCC VCC
VPP VCC $\overline{PWD}$
D0~D7 $\overline{CE}$
A0~A19 $\overline{WE}$
RY/$\overline{BY}$ $\overline{OE}$
GND

RDY/$\overline{BSY}$

WP

BVD1

BVD2

VCC

VPP1

VPP2

$\overline{CD1}$

$\overline{CD2}$

GND

$\overline{AMWE}$

$\overline{AMCS}$

WP

VCC

EEPROM
VCC
D0~D7 $\overline{CE}$
A0~A10 $\overline{WE}$
          $\overline{OE}$
GND

4. Pin Connections

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	18	Vpp1	35	GND	52	Vpp2
2	D3	19	A16	36	$\overline{CD1}$	53	A22
3	D4	20	A15	37	D11	54	A23(NC)
4	D5	21	A12	38	D12	55	A24(NC)
5	D6	22	A7	39	D13	56	A25(NC)
6	D7	23	A6	40	D14	57	NC
7	$\overline{CE1}$	24	A5	41	D15	58	NC
8	A10	25	A4	42	$\overline{CE2}$	59	NC
9	$\overline{OE}$	26	A3	43	NC	60	NC
10	A11	27	A2	44	NC	61	$\overline{REG}$
11	A9	28	A1	45	NC	62	BVD2
12	A8	29	A0	46	A17	63	BVD1
13	A13	30	D0	47	A18	64	D8
14	A14	31	D1	48	A19	65	D9
15	$\overline{WE}$ / $\overline{PGM}$	32	D2	49	A20	66	D10
16	RDY/ $\overline{BSY}$	33	$\overline{WP}$	50	A21	67	$\overline{CD2}$
17	Vcc	34	GND	51	Vcc	68	GND

Pin Descriptions:

D0~D7	Data Bus (Input/Output)
D8~D15	Data Bus (Input/Output)
A0~A22	Address Bus (Input)
$\overline{CE1}$, $\overline{CE2}$	Card Enable (Input)
$\overline{OE}$	Output Enable (Input)
$\overline{WE}$/$\overline{PGM}$	Write Enable/Program (Input)
$\overline{CD1}$, $\overline{CD2}$	Card Detect (Output)(Card Inserted Detection Signal)
$\overline{WP}$	Write Protect (Output)(in write protect mode, the WP output signal is "HIGH")
Vpp1	Program/Erase Power Supply(Even Byte)
Vpp2	Program/Erase Power Supply(Odd Byte)
$\overline{REG}$	Register Select (Input)
BVD1, BVD2	Battery Voltage Detect(Always "HIGH")
RDY/$\overline{BSY}$	Ready/Busy (Output)

Notes: Pin 54: Address bit 23, Pin 55: Address bit 24, Pin 56: Address bit 25 are no connection.

5. Function

5.1 Memory Block

5.1.1 Memory Configuration   8Mbits Flash Memory x 8 Devices.

5.1.2 Memory Erase Unit   Block Erase

Block :   Byte Mode   64k bytes
           Word Mode   128k bytes

D15	D8	D7	D0	
High byte		Low byte		x16 mode
		Even byte		x8 mode
		Odd byte		

7FFFFFH

DEVICE PAIR 3

600000H

5FFFFFH

DEVICE PAIR 2

400000H

3FFFFFH

1M x 8bits   1M x 8bits

DEVICE PAIR 1

200000H

1FFFFFH

DEVICE PAIR 0

000000H

Device Pair

Addr		Hi	Lo
FFFFFH	15.		
F0000H			
EFFFFH	14. Hi-Device Block	Lo-Device Block
E0000H			
DFFFFH	13.		
D0000H			
CFFFFH	12. Odd-Device Block	Even-Device Block
C0000H			
BFFFFH	11.		
B0000H			
AFFFFH	10. 64k x 8	64k x 8
A0000H			
9FFFFH	9.		
90000H			
8FFFFH	8.		
80000H			
7FFFFH	7.		
70000H			
6FFFFH	6.		
60000H			
5FFFFH	5.		
50000H			
4FFFFH	4.		
40000H			
3FFFFH	3.		
30000H			
2FFFFH	2.		
20000H			
1FFFFH	1.		
10000H			
0FFFFH	0.		
00000H			

1M x8bits

Block Pair

5.2 Function Table

$\overline{CE1}$	$\overline{CE2}$	A0	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	Vpp1	Vpp2	Vcc	Operation	D0-D7	D8-D15	Status
H	H	×	×	×	H	VppL	VppL	Vcc		Hi-Z	Hi-Z	Standby
L	H	L	H	L	H	VppL	VppL	Vcc	Read(×8)	Do(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppL	VppL	Vcc	Read(×8)	Do(Odd))	Hi-Z	Byte
L	L	×	H	L	H	VppL	VppL	Vcc	Read(×16)	Do(Even)	Do(Odd)	Word
H	L	×	H	L	H	VppL	VppL	Vcc	Read(×8)	Hi-Z	Do(Odd)	Byte
L	×	×	×	H	H	VppL	VppL	Vcc	Outpu Disable	Hi-Z	Hi-Z	Byte
H	L	×	×	H	H	VppL	VppL	Vcc	Outpu Disable	Hi-Z	Hi-Z	Byte
L	H	L	L	H	H	VppH	VppX	Vcc	Program(×8)	Di(Even)	Don't care	Byte
L	H	H	L	H	H	VppX	VppH	Vcc	Program(×8)	Di(Odd)	Don't care	Byte
L	L	×	L	H	H	VppH	VppH	Vcc	Program(×16)	Di(Even)	Di(Odd)	Word
H	L	×	L	H	H	VppX	VppH	Vcc	Program(×8)	Don't care	Di(Odd)	Byte
L	H	L	H	L	H	VppH	VppX	Vcc	Verify(×8)	Do(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppX	VppH	Vcc	Verify(×8)	Do(Odd)	Hi-Z	Byte
L	L	×	H	L	H	VppH	VppH	Vcc	Verify(×16)	Do(Even)	Do(Odd)	Word
H	L	×	H	L	H	VppX	VppH	Vcc	Verify(×8)	Hi-Z	Do(Odd)	Byte
L	H	H	L	L	H	VppH	VppX	Vcc	*1 Prohibited	——	——	——
L	H	L	L	L	H	VppX	VppH	Vcc	*1 Prohibited	——	——	——
L	L	×	L	L	H	VppH	VppH	Vcc	*1 Prohibited	——	——	——
H	L	×	L	L	H	VppX	VppH	Vcc	*1 Prohibited	——	——	——

*1. Do not use this mode as it will result in write errors.

H	:	High	L	:	Low
Di	:	Input Data	Do	:	Output Data
Vcc	:	4.5~5.5V	VppL	:	0.0~1.5V
VppX	:	VppL or VppH			

× : Don't care
Hi-Z: High Impedance
VppH: 4.5~5.5V/11.4~12.6V

Caution: When the write protect switch is in protect-mode, the WP signal is "HIGH"
and write operation are not allowed.

5.3 Software Command(8/16 Bits Operation ():16 Bits Operation)

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle			
		Operation	Address	Data	Operation	Address	Data Input	Data Output
Read Array /Reset	1	Write	R A	FFH/ (FFFFH)	——	——	——	——
Read Intelligent Identifier	3	Write	D A	90H/ (9090H)	Read	I A	——	I I D
Read Status Register	2	Write	D A	70H/ (7070H)	Read	D A	——	S R D
Clear Status Register	1	Write	D A	50H/ (5050H)	——	——	——	——
Erase Setup /Erase Confirm	2	Write	B A	20H/ (2020H)	Write	B A	D0H/ (D0D0H)	——
Erase Suspend/ Erase Resume	2	Write	B A	B0H/ (B0B0H)	Write	B A	D0H/ (D0D0H)	——
Byte Write Setup/Write	2	Write	W A	40H/ (4040H)	Write	W A	W D	——
Alternate Byte Write Setup/Write	2	Write	W A	10H/ (1010H)	Write	W A	W D	——

Note)1. This Table shows the basic form of Erase, Verify and Program Verify.
　　　　Refer Programming Flowchart, Erase Algorithm in detail.
　　　2. Bus operations are defined in function table in page.
　　　3. I A :Device Identifier Address　　　I I D :Device Identifier Data

	D A	I A			I I D	
		8Bits (Even Device)	8Bits (Odd Device)	16Bits	Byte (8Bits)	Word (16Bits)
Manufacturer Code	000000H~1FFFFFH	000000H	000001H	000000H	89H	8989H
Device Code	000000H~1FFFFFH	000002H	000003H	000001H	A6H	A6A6H

　　　　R A　: Read Address　　　W A　: Write Address　　　W D　: Write Data
　　　　D A　: Device Address (Any Address in device is acceptable.)
　　　　B A　: Erase Block Address (Erase Size is 64k Bytes.)
　　　　S R D : Status Register Data

　　　4. Either 40H(4040H) or 10H(1010H) are recognized by the WSM as the
　　　　　Byte Write Setup Command.

a) Read Array/Reset Command:(FFH/FFFFH)
By writing this command, device/devices pair become read mode. The device remains enable for reads until the Command User Interface contents are altered.

b) Intelligent Identifier Command:(90H/9090H):
After writing this command into the Command User Interface, a read cycle retrieves the manufacturer Code and device Code. To terminate the Operation, it is necessary to write another valid command into the register.

c) Read Status Register Command:(70H/7070H):
By Writing this command, the Status Register may be read at any time to determine when a byte or block erase operation is complete, and whether that operation completed successfully. Refer to Status Register definition in page.9 . After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface.

d) Clear Status Register Command:(50H/5050H)
Status bits which show error, the Erase Status(SR.5), Byte Write Status(SR.4) bits and the Vpp Status bit(SR.3) can be reset by the Clear Status Machine Register Command.

e) Erase Setup/Erase Command:(20H/2020H)/(D0H/D0D0H):
Erase is executed one block(64kB for 1 device, 128kB for 2 devices) at a time.
This command is functional when Vpp=VppH and an Erase Setup Command is first written to the Command User Interface, followed by the Erase Confirm Command. After that, the device automatically outputs Status Register data when read. The CPU can detect the completion of the erase event by analyzing the output of the RDY/BSY pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked.
If erase error is detected, the Status Register should be cleared.

f) Erase Suspend/Erase Resume Command:(B0H/B0B0H)/(D0H/D0D0H)
The Erase Suspend command allows block erase interruption in order to read data from another block of memory. The device continues to output Status Register data when read, after the Erase Suspend Command is written. Polling the WSM Status and Erase Suspend Statu Status bits will determine when the erase operation has been suspended. RDY/BSY pin will also transition to V_{OH}. At this point, a Read Array Command can be written to the Command User Interface to read data from blocks other than that which is suspended. Vpp must remain at VppH while device is in Erase Suspend. Erase Resume Command , at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RDY/BSY pin will return to V_{OL}. After the Erase Resume is written, the device automatically output Status Register data when read.

g) Byte Write Setup/Write Command:(40H/4040H) or (10H/1010H)
This command is functional when Vpp=VppH and an Byte Write Setup Command is first written to the Command User Interface, followed by a second write specifying the address and data to be written. The WSM then take over, controlling the byte write and write verify algorithms internally. After the two command byte sequence is written to it, the device automatically outputs Status Register data when read. The CPU can detect the completion of the byte write event by analyzing the output of the RDY/BSY pin , or the WSM Status bits of the Status Register.

5.4 Status Register
The memory devices in this card have Status Register which shows state of the device.

Byte Access ×8 Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
	WSMS	ESS	ES	BWS	VPPS	RFU	RFU	RFU

Register	Contents
SR.7 = Write State Machine Status 　　　1 = Ready 　　　0 = Busy	When set "1"s, read, erase, data write is acceptable.
SR.6 = Erase Suspend Status 　　　1 = Erase Suspend 　　　0 = Erase In Progress/Completed	Check whether Erase Suspend Command is executed or not.
SR.5 = Erase Status 　　　1 = Error In Block Erase 　　　0 = Successful Block Erase	Set "1"s when fail to Erase. Reset by the Clear Status Register Command.
SR.4 = Byte Write Status 　　　1 = Error In Byte Write 　　　0 = Successful Byte Write	Set "1"s when fail to Byte write. Reset by the Clear Status Register Command.
SR.3 = Vpp Status 　　　1 = Vpp Low Detect;Operation Abort 　　　0 = Vpp OK	Set "1"s when Vpp, which is needed in Byte Write or Erase operation, is below VppH. Reset by the Clear Status Register Command.
SR.2~SR.0 = Reserved for Future Use	

Word Access ×16 bits

bit15　　　　　　　　　　　　　　　　　　　bit8 bit7　　　　　　　　　　　　　　bit0

SR. 15	SR. 14	SR. 13	SR. 12	SR. 11	SR. 10	SR.9	SR.8	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
Odd Byte device								Even Byte device							

5.5 Programming Flowchart
   (Byte Mode)
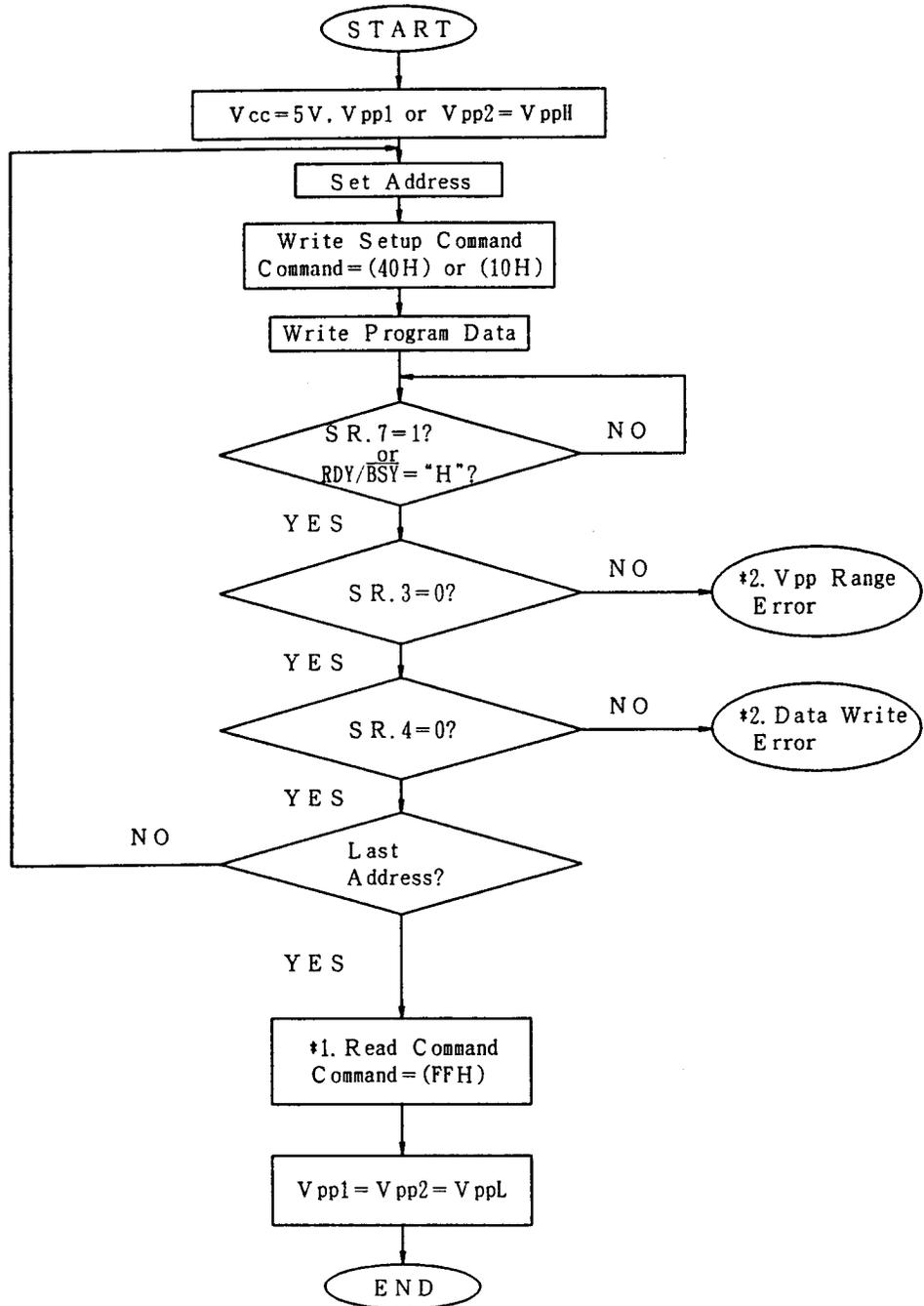
```
                    ┌─────────┐
                    │  START  │
                    └────┬────┘
                         │
          ┌──────────────┴───────────────┐
          │ Vcc=5V, Vpp1 or Vpp2=VppH     │
          └──────────────┬───────────────┘
                         │
              ┌──────────┴──────────┐
              │    Set Address      │
              └──────────┬──────────┘
                         │
              ┌──────────┴──────────┐
              │ Write Setup Command  │
              │ Command=(40H) or (10H)│
              └──────────┬──────────┘
                         │
              ┌──────────┴──────────┐
              │ Write Program Data   │
              └──────────┬──────────┘
                         │
                    ╱────┴────╲
                   ╱ SR.7=1?   ╲    NO
                  ╱    or        ╲──────┐
                  ╲ RDY/BSY="H"? ╱       │
                   ╲────┬────╲ ╱         │
                       YES                │
                        │←───────────────┘
                    ╱────┴────╲      NO      ┌──────────┐
                   ╱ SR.3=0?   ╲─────────────│ *2. Vpp Range│
                   ╲──────────╱               │    Error  │
                       YES                    └──────────┘
                        │
                    ╱────┴────╲      NO      ┌──────────┐
                   ╱ SR.4=0?   ╲─────────────│ *2. Data Write│
                   ╲──────────╱               │    Error  │
                       YES                    └──────────┘
                        │
            NO      ╱────┴────╲
           ┌───────╱  Last     ╲
           │       ╲ Address?  ╱
           │        ╲─────────╱
           │            YES
           │             │
           │   ┌─────────┴─────────┐
           │   │ *1. Read Command  │
           │   │ Command=(FFH)     │
           │   └─────────┬─────────┘
           │             │
           │   ┌─────────┴─────────┐
           │   │ Vpp1=Vpp2=VppL    │
           │   └─────────┬─────────┘
           │             │
           │        ┌────┴────┐
           │        │   END   │
           │        └─────────┘
```

Note) *1. Write FFH after the last block write operation to reset the device to
         Read Array Mode.
     *2. If error is detected, clear the Status Register before attempting retry
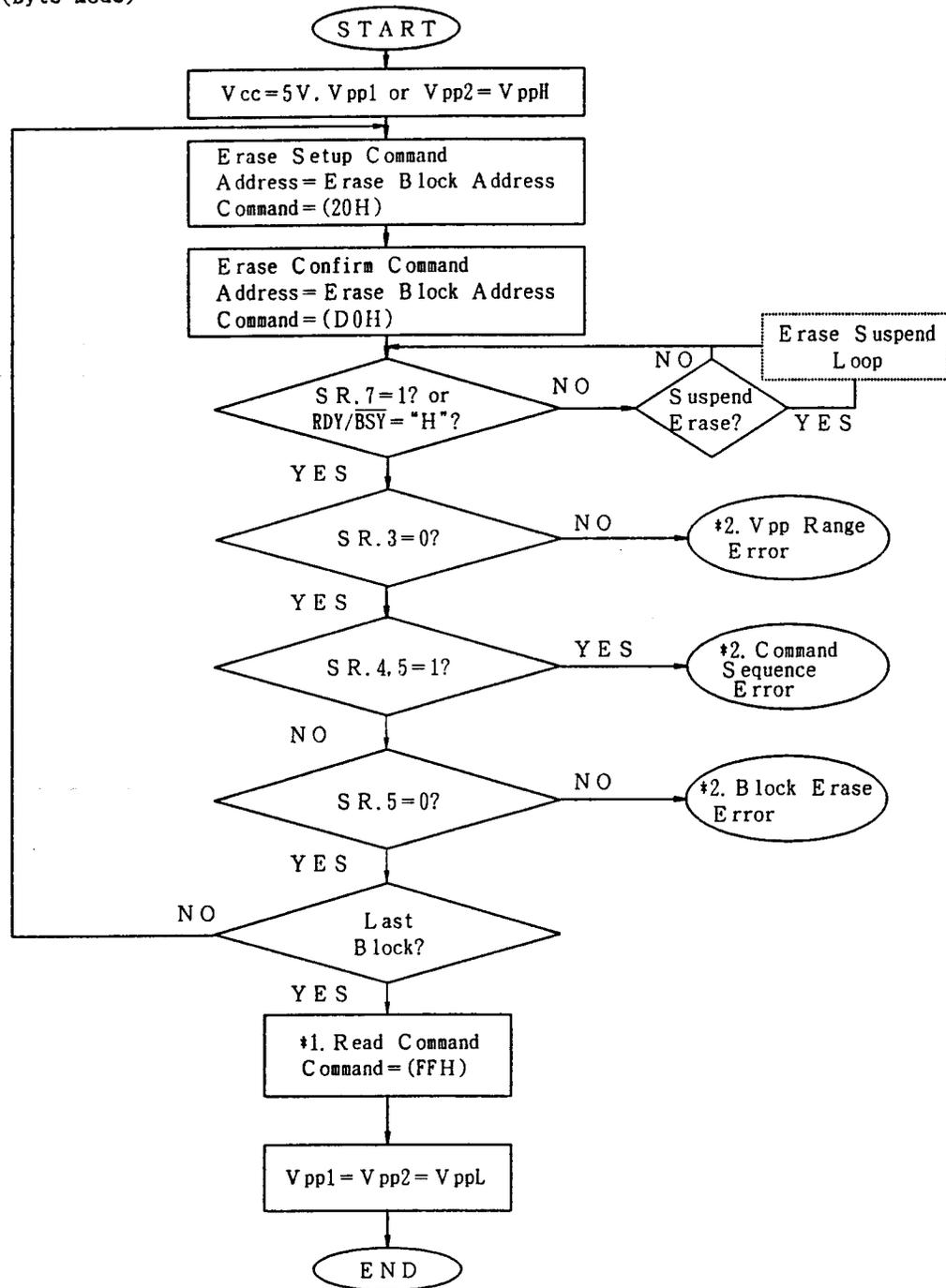   or other error recovery.

Programming Flowchart
(Word Mode)
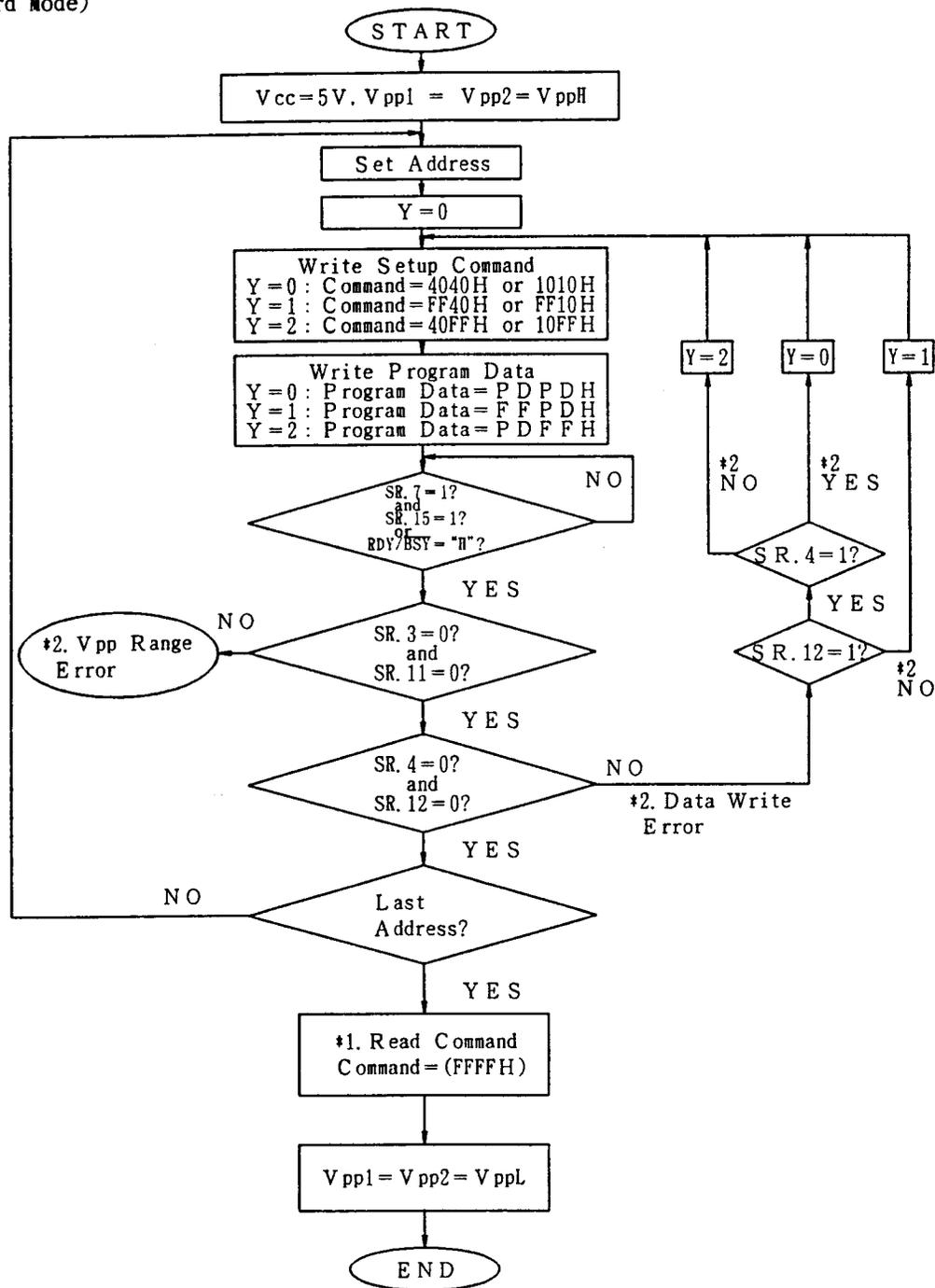
```
                    ( S T A R T )
                          |
          +-------------------------------+
          | Vcc=5V, Vpp1 = Vpp2=VppH      |
          +-------------------------------+
                          |
          +---------------------+
          |   Set Address       |
          +---------------------+
          +---------------------+
          |      Y = 0          |
          +---------------------+
          +--------------------------------------+
          |       Write Setup Command            |
          | Y=0 : Command=4040H or 1010H         |
          | Y=1 : Command=FF40H or FF10H         |
          | Y=2 : Command=40FFH or 10FFH         |
          +--------------------------------------+
          +--------------------------------------+
          |       Write Program Data             |      [Y=2]  [Y=0]  [Y=1]
          | Y=0 : Program Data=PDPDH             |
          | Y=1 : Program Data=FFPDH             |
          | Y=2 : Program Data=PDFFH             |
          +--------------------------------------+

                    < SR.7 = 1?
                      and              > NO
                      SR.15 = 1?
                      or                        *2    *2
                      RDY/BSY = "H"? >          NO    YES
                          |
                         YES                    < S R.4 = 1? >
                                                      |
         NO       < SR.3 = 0?                        YES
  ( *2. Vpp Range <    and      >          < S R.12 = 1? >  *2
    Error )         SR.11 = 0?                              NO
                          |
                         YES

                    < SR.4 = 0?
                      and        >  NO
                      SR.12 = 0?              *2. Data Write
                          |                       Error
                         YES

    NO          < Last
         <        Address? >
                          |
                         YES
          +---------------------+
          | *1. Read Command    |
          | Command = (FFFFH)   |
          +---------------------+
          +---------------------+
          | Vpp1 = Vpp2 = VppL  |
          +---------------------+
                          |
                    ( E N D )
```

Note) *1. Write FFFFH after the last block write operation to reset the device to
          Read Array Mode.
      *2. If error is detected, clear the Status Register before attempting retry
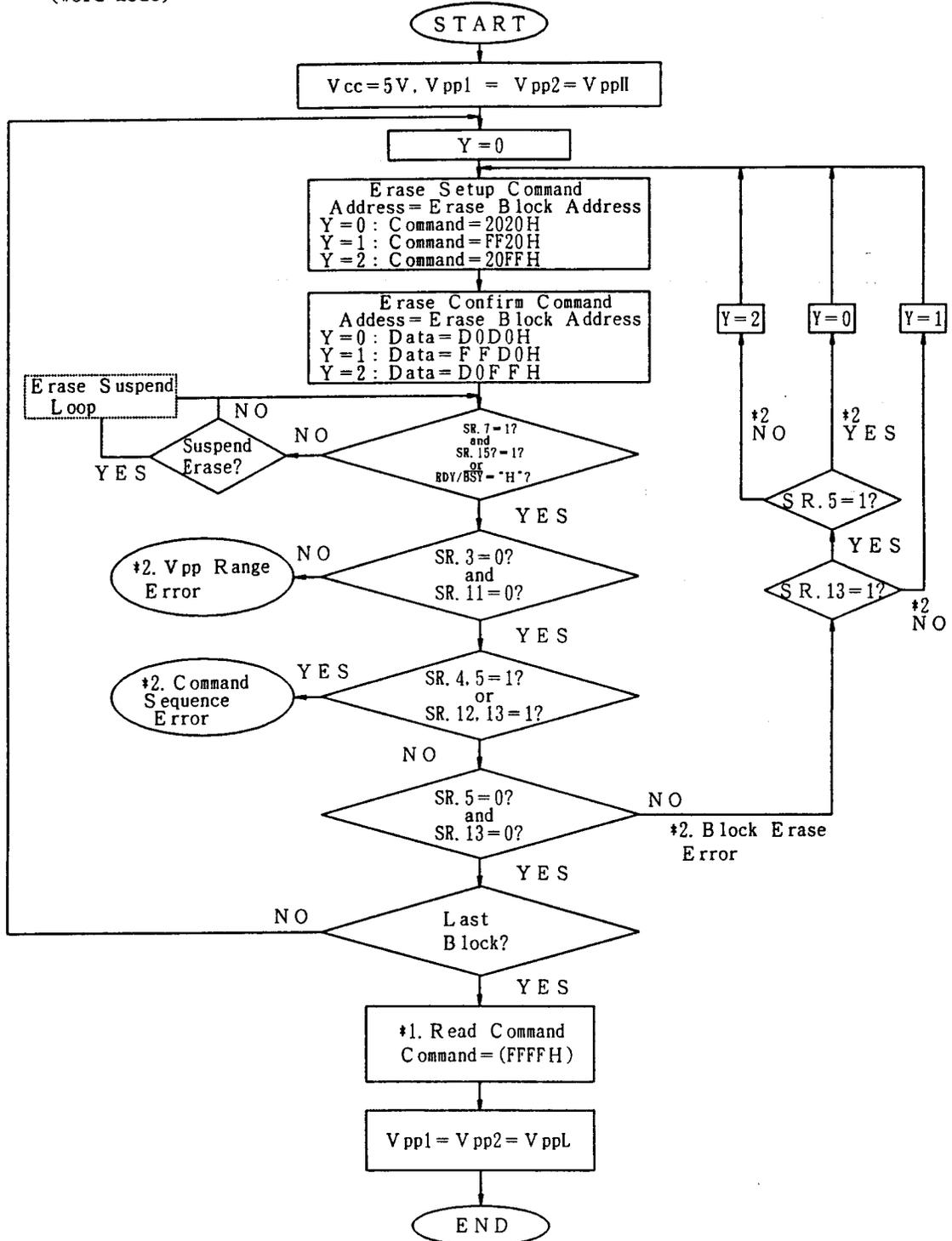   or other error recovery.

5.6 Erase Algorithm
    (Byte Mode)

```
                            ( START )
                                │
             ┌──────────────────▼──────────────────┐
             │  V cc = 5 V. V pp1 or  V pp2 = V ppH │
             └──────────────────┬──────────────────┘
     ┌───────────────────►      │
     │       ┌─────────────────▼──────────────────┐
     │       │  Erase Setup Command               │
     │       │  Address = Erase Block Address      │
     │       │  Command = (20H)                    │
     │       └─────────────────┬──────────────────┘
     │       ┌─────────────────▼──────────────────┐
     │       │  Erase Confirm Command             │
     │       │  Address = Erase Block Address      │         ┌───────────────────┐
     │       │  Command = (D0H)                    │         │ Erase Suspend     │
     │       └─────────────────┬──────────────────┘         │ Loop              │
     │                         │                NO          └───────────────────┘
     │              ┌──────────▼──────────┐  NO  ┌───────────┐           ▲
     │              │   S R. 7 = 1? or    ├─────►│ Suspend   │           │
     │              │   RDY/BSY = "H"?    │      │ Erase?    ├──── YES ──┘
     │              └──────────┬──────────┘      └───────────┘
     │                        YES
     │              ┌──────────▼──────────┐  NO      ┌──────────────────┐
     │              │    S R. 3 = 0?      ├─────────►│ *2. Vpp Range    │
     │              └──────────┬──────────┘          │     Error        │
     │                        YES                    └──────────────────┘
     │              ┌──────────▼──────────┐  YES     ┌──────────────────┐
     │              │    S R. 4, 5 = 1?   ├─────────►│ *2. Command      │
     │              └──────────┬──────────┘          │     Sequence     │
     │                         NO                    │     Error        │
     │              ┌──────────▼──────────┐  NO      └──────────────────┘
     │              │    S R. 5 = 0?      ├─────────►┌──────────────────┐
     │              └──────────┬──────────┘          │ *2. Block Erase  │
     │                        YES                    │     Error        │
     │   NO         ┌──────────▼──────────┐          └──────────────────┘
     └──────────────┤    Last Block?      │
                    └──────────┬──────────┘
                              YES
                    ┌──────────▼──────────┐
                    │ *1. Read Command    │
                    │     Command = (FFH) │
                    └──────────┬──────────┘
                    ┌──────────▼──────────┐
                    │ V pp1 = V pp2 = V ppL│
                    └──────────┬──────────┘
                               │
                           ( END )
```

Note) *1. Write FFH after the last block erase operation to reset the device to
         Read Array Mode.
     *2. If error is detected, clear the Status Register before attempting retry
         or other error recovery.

Erase Algorithm
(Word Mode)

START

$Vcc = 5V$, $Vpp1 = Vpp2 = VppII$

$Y = 0$

Erase Setup Command
Address = Erase Block Address
$Y = 0$: Command = 2020H
$Y = 1$: Command = FF20H
$Y = 2$: Command = 20FFH

Erase Confirm Command
Address = Erase Block Address
$Y = 0$: Data = D0D0H
$Y = 1$: Data = FFD0H
$Y = 2$: Data = D0FFH

$Y = 2$ $Y = 0$ $Y = 1$

Erase Suspend
Loop

Suspend
Erase?   NO   SR. 7 = 1?
and
SR. 15? = 1?
or
RDY/BSY = "H"?

NO

YES

*2
NO   *2
YES

SR. 5 = 1?

YES

*2. Vpp Range
Error   NO   SR. 3 = 0?
and
SR. 11 = 0?

YES

SR. 13 = 1?

*2
NO

*2. Command
Sequence
Error   YES   SR. 4, 5 = 1?
or
SR. 12, 13 = 1?

NO

SR. 5 = 0?
and
SR. 13 = 0?   NO

*2. Block Erase
Error

YES

NO   Last
Block?

YES

*1. Read Command
Command = (FFFFH)

$Vpp1 = Vpp2 = VppL$

END

Note) *1. Write FFFFH after the last block erase operation to reset the device to
Read Array Mode.
*2. If error is detected, clear the Status Register before attempting retry
or other error recovery.

6. Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{cc}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-0.3 to Vcc+0.3(Max:7.0)	V
Output Voltage	V_{OUT}	-0.3 to Vcc+0.3(Max:7.0)	V
Operating Temperature	T_{OPR}	0 to +60	℃
Storage Temperature	T_{STG}	-20 to +65	℃

7. Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Operating Temperature	T_{OPR}	0	+60	℃
Supply Voltage	V_{cc}	4.5	5.5	V
Input Voltage High	V_{IH}	3.5	V_{cc}+0.3	V
Input Voltage Low	V_{IL}	-0.3	1.5	V

8. Capacitance

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	—	17	—	pF	Vcc=5V±10%
Input/Output Capacitance	C_{IO}	—	17	—	pF	f=1MHz, Ta=25℃

9. Read Operation
  9.1 D C Characteristics   (Vcc=4.5~5.5V, Ta=0~60℃)

	PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
1	Operating Voltage	High Temperature	V_{cc}	4.50	—	5.50	V	
		Low Temperature						
*¹2	Current Consumption	Static Operatin Current	I_{SB}	—	—	2.0	mA	X16, Address :PingPong
		Dynamic Operating Current	I_{CC}	—	—	80		
3	Input Voltage	Input Voltage Level High	V_{IH}	3.5	—	Vcc+0.3	V	Vcc= 4.5~5.5V
		Input Voltage Level Low	V_{IL}	-0.3	—	1.5		
4	Input Current	A0~A20, D0~D15	I_{LI}	-10		70	μA	V_I=Vcc, 0V
		$\overline{CE1}, \overline{CE2}, \overline{OE}, \overline{WE}, \overline{REG}$		-70	—	10		
5	Output Voltage	High	V_{OH}	Vcc-0.5	—	—	V	I_{OH}=-2mA(*²) I_{OH}=-4μA(*³)
		Low	V_{OL}	—	—	0.4		I_{OL}= 4mA

PingPong:Scan the target address, with accessing the target and another address alternately.
 *¹ (1) Static Operating Current:With the memory card's voltage at 5.5V and the $\overline{CE1}, \overline{CE2}$
     $\overline{OE}, \overline{WE}$ and $\overline{REG}$ signals "HIGH"(V_{IH}=Vcc-0.2V), A0 signal "LOW"(V_{IL}≤0.2V) the current
     consumption is measured with the output open.
   (2) Dynamic Operating Current : With the memory card's Vcc at 5.5V and Vpp1=Vpp2 at
     12.6V, current consumption during access is measured with the output open.
     (Access time: 200ns) The current depends on addressing.
 *² D0~D15
 *³ BVD1, BVD2, RDY/$\overline{BSY}$, WP

 9.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=0.0~1.5V, Ta=0~60℃)
    Testing Conditions:
         1) Input Pulse Level   : 0.8~3.5V
         2) Input Rise/Fall Time   : 10ns
         3) Input/Output Timing Reference Level : 1.5V
         4) Output Load   : 1TTL+C_L(100pF) (including scope
                                                   and jig capacitance)
       9.2.1 Read Cycle   (Vcc=4.5~5.5V, Vpp=0.0~1.5V, Ta=0~60℃)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Read Cycle Time	t_{AVAV}	t_{cR}	200	—	n s
Address Access Time	t_{AVQV}	$t_a(A)$	—	200	
Card Enable Access Time	t_{ELQV}	$t_a(CE)$	—	200	
Output Enable Access Time	t_{GLQV}	$t_a(OE)$	—	100	
Output Disable Time from $\overline{CE}$*	t_{EHQV}	$t_{dis}(CE)$	—	90	
Output Disable Time from $\overline{OE}$*	t_{GHQZ}	$t_{dis}(OE)$	—	90	
Output Enable Time from $\overline{CE}$	t_{ELQX}	$t_{en}(CE)$	5	—	
Output Enable Time from $\overline{OE}$	t_{GLQX}	$t_{en}(OE)$	5	—	
Data Valid from Add Change		$t_v(A)$	0	—	

 *Time until output becomes floating.(The output voltage is not defined.)

○ Read CYCLE(1)   ($\overline{CE2}$ = V$_{IH}$ Fixed) , 8 Bits Output
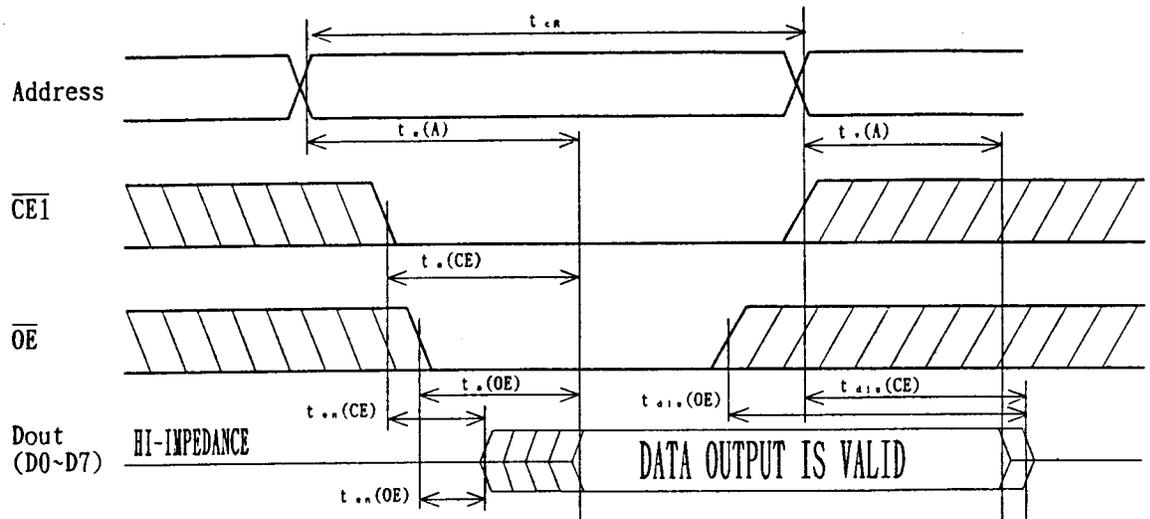
t_{cR}

Address

$t_a(A)$ $t_a(A)$

$\overline{CE1}$

$t_a(CE)$

$\overline{OE}$

$t_a(OE)$ $t_{dis}(OE)$ $t_{dis}(CE)$

$t_{en}(CE)$

Dout
(D0~D7)   HI-IMPEDANCE   DATA OUTPUT IS VALID

$t_{en}(OE)$

Note) 1. $\overline{WE}$="HIGH", during a read cycle.
     2. Either "HIGH" or "LOW" in diagonal areas.
     3. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE)
     have concluded.

○ Read Cycle(2)   ($\overline{CE1}$ = V$_{IH}$ Fixed), 8 Bits Output
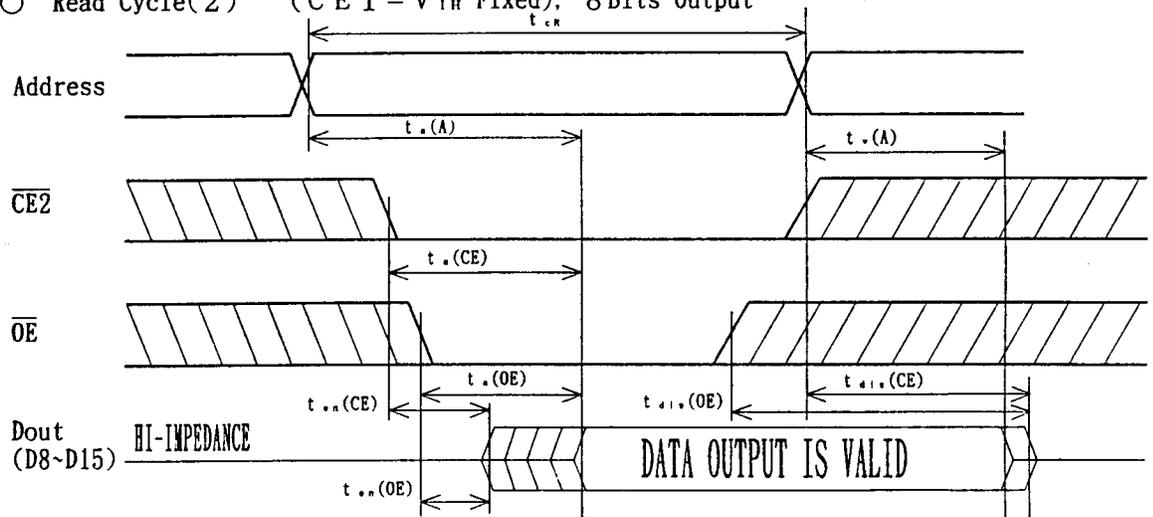
t_{cR}

Address

$t_a(A)$ $t_a(A)$

$\overline{CE2}$

$t_a(CE)$

$\overline{OE}$

$t_a(OE)$ $t_{dis}(OE)$ $t_{dis}(CE)$

$t_{en}(CE)$

Dout
(D8~D15)   HI-IMPEDANCE   DATA OUTPUT IS VALID

$t_{en}(OE)$

Note) 1. $\overline{WE}$="HIGH", during a read cycle.
     2. Either "HIGH" or "LOW" in diagonal areas.
     3. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE)
     have concluded.

○ Read Cycle（3）．１６Bits Output
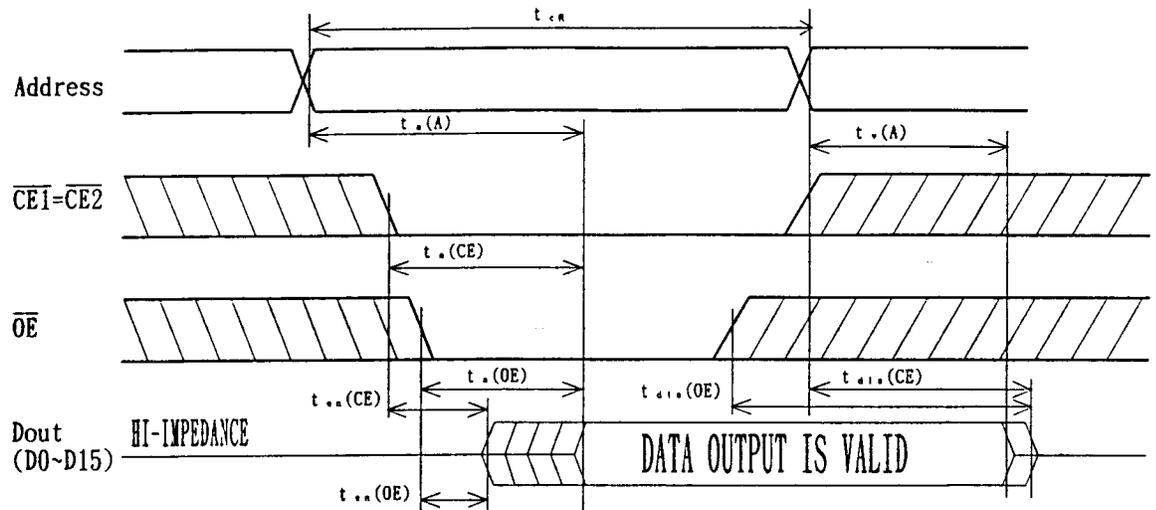
Note）1. WE="HIGH", during a read cycle.
   2. Either "HIGH" or "LOW" in diagonal areas.
   3. Change CE1 and CE2 at the same time.
   4. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE) have concluded.

10. Programming Operation
10.1 DC Characteristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION	
Vpp1, Vpp2 operating Voltage	Read	V_{PPL}	0	1.5	V		
	Program	V_{PPH}	4.5	5.5		Vpp=4.5~5.5V	
			11.4	12.6		Vpp=11.4~12.6V	
Vpp1, Vpp2 operating Current (X16 Mode)	Read	I_{SB2}	–	1.6	mA	Input open	
	Program	I_{PP}	–	45		RMS	Vpp=4.5~5.5V
			–	20			Vpp=11.4~12.6V
Vcc operating Current	Standby	I_{SB1}	–	2		Input open	
	Program	I_{CC}	–	75		RMS	X16 Mode
Input Voltage		V_{IL}	-0.3	1.5	V		
		V_{IH}	3.5	Vcc+0.3			
Output Voltage During Verify		V_{OL}	–	0.4		I_{OL}= 4mA	
		V_{OH}	Vcc-0.5	–		I_{OH}=-2mA	

Note）1. Power on Vcc before power on Vcc, power off Vcc after power off Vpp.
   2. Keep Vpp including its overshoot, below 13V.
   3. Card insertion or removal while applying Vpp=12V may cause a loss of integrity.
   4. Do not turn on or turn off during CE="LOW".
   5. If V_{IH} goes above Vcc+0.3V, normal operation is not assured.

10.2　A C Characteristics　　(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)
Testing Conditions:
1) Input Pulse Level　　　　　　　　　　　 : 0.8~3.5V
2) Input Rise/Fall Time　　　　　　　　　 : 10ns
3) Input/Output Timing Reference Level　 : 1.5V
4) Output Load　　　　　　　　　　　　　 : 1TTL+C$_L$(100pF) (including scope and jig capacitance)

10.2.1　Program Cycle
$\overline{WE}$ Controlled　　　　　　　　(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time		t$_{AVAV}$	t$_{cw}$	200	—	ns
Address Setup Time		t$_{AVWL}$	t$_{su}$(A)	20	—	
Write Recovery Time		t$_{WHAX}$	t$_{rec}$(WE)	30	—	
Data Setup Time for $\overline{WE}$		t$_{DVWH}$	t$_{su}$(D-WEH)	60	—	
Data Hold Time		t$_{WHDX}$	t$_h$(D)	30	—	
Write Recovery Before Read		t$_{WHGL}$		10	—	
Card Enable Setup time for $\overline{WE}$		t$_{ELWH}$	t$_{su}$(CE-WEH)	140	—	
Address Setup for $\overline{WE}$		t$_{AVWH}$	t$_{su}$(A-WEH)	140	—	
Card Enable Hold Time		t$_{WHEH}$		15	—	
Write Pulse Width		t$_{WLWH}$	t$_w$(WE)	120	—	
Write Pulse Width High		t$_{WHWL}$	t$_w$(WEH)	30	—	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t$_{WHRL}$		—	150	
Duration of write operation	Vpp=4.5~5.5V	t$_{WHQV}$		6.5	—	μs
	Vpp=11.4~12.6V			4.8	—	
Vpp Setup to $\overline{WE}$ Going High		t$_{VPWH}$		100	—	
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t$_{QVVL}$		0	—	ns

$\overline{CE}$ Controlled　　　　　　　　(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time		t$_{AVAV}$	t$_{cw}$	200	—	ns
Address Setup Time		t$_{AVEL}$	t$_{su}$(A)	20	—	
Write Recovery Time		t$_{EHAX}$	t$_{rec}$(CE)	30	—	
Data Setup Time for $\overline{CE}$		t$_{DVEH}$	t$_{su}$(D-CEH)	60	—	
Data Hold Time		t$_{EHDX}$	t$_h$(D)	30	—	
Write Recovery Before Read		t$_{EHGL}$		10	—	
Write Enable Setup time for $\overline{CE}$		t$_{WLEH}$	t$_{su}$(WE-CEH)	140	—	
Address Setup for $\overline{CE}$		t$_{AVEH}$	t$_{su}$(A-CEH)	140	—	
Write Enable Hold Time		t$_{EHWH}$		0	—	
Write Pulse Width		t$_{ELEH}$	t$_w$(CE)	120	—	
Write Pulse Width High		t$_{EHEL}$	t$_w$(CEH)	30	—	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t$_{EHRL}$		—	150	
Duration of write operation	Vpp=4.5~5.5V	t$_{EHQV}$		6.5	—	μs
	Vpp=11.4~12.6V			4.8	—	
Vpp Setup to $\overline{WE}$ Going High		t$_{VPEH}$		100	—	
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t$_{QVVL}$		0	—	ns

1. Set $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when Vpp changes from VppL to VppH or vice versa.

○ Program Cycle ($\overline{WE}$ Controlled)

Vcc POWER-UP & STANDBY

WRITE BYTE WRITE OR ERASE SETUP COMMAND

WRITE VALID ADDRESS & DATA(BYTE WRITE) OR ERASE CONFIRM COMMAND

AUTOMATED BYTE WRITE OR ERASE DELAY

READ STATUS REGISTER READ

WRITE READ ARRY COMMAND

Address

$\overline{CE}$

$\overline{OE}$

$\overline{WE}$

DATA

RDY/$\overline{BSY}$

Vpp

A_{IN} A_{IN}

D_{IN} D_{IN} VALID SRD D_{IN}

HI-IMPEDANCE

$t_{su}(A)$ $t_{su}(A-\overline{WEH})$ $t_{rec}(\overline{WE})$

t_{cw} $t_{w}(\overline{WEH})$ $t_{w}(\overline{WE})$ t_{WHBH} t_{WHGL}

$t_{su}(CE-\overline{WEH})$ $t_{su}(D-\overline{WEH})$ $t_{su}(D)$ t_{WHQV1} t_{WHRL} t_{QVVL}

t_{VPVH}

V_{IH} V_{IL}

Note) While the data signal is in output mode, do not apply an opposite phase signal.

○ Program Cycle (CE Controlled)

| Vcc POWER UP & STANDBY | WRITE BYTE WRITE OR ERASE SETUP COMMAND | WRITE VALID ADDRESS & DATA (BYTE WRITE) OR ERASE CONFIRM COMMAND | AUTOMATED BYTE WRITE OR ERASE DELAY | READ STATUS REGISTER DATA | WRITE READ ARRAY COMMAND |

Address

$\overline{WE}$

$\overline{OE}$

$\overline{CE}$

DATA

RDY/$\overline{BSY}$

Vpp

Voltage levels: V_{IH}, V_{IL}, V_{OH}, V_{OL}, V_{PPH}, V_{PPL}

A_{IN}, D_{IN}, VALID SRD, HI-IMPEDANCE

Timing parameters: $t_{su}(A)$, t_{cw}, $t_{w}(CEH)$, $t_{su}(WE-CEH)$, $t_{su}(D-CEH)$, $t_{su}(D)$, $t_{w}(CE)$, $t_{w}(A-CEH)$, $t_{rec}(CE)$, t_{GHWH}, t_{EHGL}, t_{GHQV1}, t_{EHRL}, t_{QVVL}, t_{VPEH}

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11. Erase Operation
11.1 DC Charactristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION	
Vpp1, Vpp2 Operating Voltage	Read	V_{PPL}	0	1.5	V		
	Program	V_{PPHE}	4.5	5.5		Vpp=4.5~5.5V	
			11.4	12.6		Vpp=11.4~12.6V	
Vpp1, Vpp2 Operating Current (X16 Mode)	Standby	I_{SB2}	–	1.6	mA	I/O open	
	Erase	I_{PP}	–	45		RMS	Vpp=4.5~5.5V
			–	20			Vpp=11.4~12.6V
	Erase Suspend	I_{PPS}	–	1.6		CE1, CE2=V_{IH}, RMS	
Vcc Operating Current (X16 Mode)	Standby	I_{SB1}	–	2.0		I/O open	
	Erase	I_{CCE}	–	75		RMS	
	Erase Suspend	I_{CCES}	–	22		CE1, CE2=V_{IH}, RMS	
Input Voltage		V_{IL}	-0.3	1.5	V		
		V_{IH}	3.5	V_{cc}+0.3			
Output Voltage During Verify		V_{OL}	–	0.4		I_{OL}= 4mA	
		V_{OH}	V_{cc}-0.5	–		I_{OH}=-2mA	

Note) Power on Vcc before power on Vcc , power off Vcc after power off Vpp. Keep Vpp
including its overshoot, below 13V. Card insertion or removal while applying
Vpp=12V may cause a loss of integrity. Do not turn on or turn off during CE="LOW".
If V_{IH} goes above Vcc+0.3V, normal operation is not assured.

11.2 AC Characteristics   (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)
Testing Conditions:
1) Input Pulse Level   : 0.8~3.5V
2) Input Rise/Fall Time   : 10ns
3) Input/Output Timing Reference Level   : 1.5V
4) Output Load   : 1TTL+C_L(100pF) (including scope and jig capacitance)

11.2.1 Erase Cycle
$\overline{WE}$ Controlled   (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time	t_{AVAV}	t_{cw}	200	–	ns
Address Setup Time	t_{AVWL}	$t_{su}(A)$	20	–	
Write Recovery Time	t_{WHAX}	$t_{rec}(WE)$	30	–	
Data Setup Time for $\overline{WE}$	t_{DVWH}	$t_{su}(D-WEH)$	60	–	
Data Hold Time	t_{WHDX}	$t_{h}(D)$	30	–	
Write Recovery Before Read	t_{WHGL}		10	–	
Card Enable Setup time for $\overline{WE}$	t_{ELWH}	$t_{su}(CE-WEH)$	140	–	
Address Setup for $\overline{WE}$	t_{AVWH}	$t_{su}(A-WEH)$	140	–	
Card Enable Hold Time	t_{WHEH}		15	–	
Write Pulse Width	t_{WLWH}	$t_{w}(WE)$	120	–	
Write Pulse Width High	t_{WHWL}	$t_{w}(WEH)$	30	–	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low	t_{WHRL}		–	150	
Duration of Erase operation Vpp=4.5~5.5V	t_{WHQV2}		0.9	–	s
Vpp=11.4~12.6V			0.3	–	
Vpp Setup to $\overline{WE}$ Going High	t_{VPWH}		100	–	
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High	t_{QVVL}		0	–	ns

C E Controlled (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL		MIN	MAX	UNIT
		SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time		t_{AVAV}	t_{cw}	200	—	n s
Address Setup Time		t_{AVEL}	$t_{su}(A)$	20	—	
Write Recovery Time		t_{EHAX}	$t_{rec}(CE)$	30	—	
Data Setup Time for $\overline{CE}$		t_{DVEH}	$t_{su}(D-CEH)$	60	—	
Data Hold Time		t_{EHDX}	$t_{h}(D)$	30	—	
Write Recovery Before Read		t_{EHGL}		10	—	
Write Enable Setup time for CE		t_{WLEH}	$t_{su}(WE-CEH)$	140	—	
Address Setup for $\overline{CE}$		t_{AVEH}	$t_{su}(A-CEH)$	140	—	
Write Enable Hold Time		t_{EHWH}		0	—	
Write Pulse Width		t_{ELEH}	$t_{w}(CE)$	120	—	
Write Pulse Width High		t_{EHEL}	$t_{w}(CEH)$	30	—	
$\overline{WE}$ High to RDY/BSY Going Low		t_{EHRL}		—	150	
Duration of Erase operation	Vpp=4.5~5.5V	t_{EHQV2}		0.9	—	s
	Vpp=11.4~12.6V			0.3	—	
Vpp Setup to $\overline{WE}$ Going High		t_{VPEH}		100	—	n s
Vpp Hold from Valid SRD, RDY/BSY High		t_{QVVL}		0	—	

1. Set $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when Vpp changes from PPr to PPH or vice versa.

○ ERASE CYCLE($\overline{WE}$ Controlled)

Note) While the data signal is in output mode, do not apply an
opposite phase signal.

○ ERASE CYCLE (C̄Ē Controlled)

Column headings:
- V_cc POWER UP & STANDBY
- WRITE BYTE WRITE OR ERASE SETUP COMMAND
- WRITE VALID ADDRESS & DATA(BYTE WRITE) OR ERASE CONFIRM COMMAND
- AUTOMATED BYTE WRITE OR ERASE DELAY
- READ STATUS REGISTER COMMAND
- WRITE READ ARRAY COMMAND

Signals: Address, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, DATA, RDY/$\overline{BSY}$, V_{PP}

Levels: V_{IH}, V_{IL}, V_{OH}, V_{OL}, V_{PPH}, V_{PPL}

A_{IN}, D_{IN}, VALID SRD, HI-IMPEDANCE

Timing parameters: $t_{su}(A)$, t_{cw}, $t_{w}(A\text{-}CEH)$, $t_{rec}(CE)$, $t_{su}(WE\text{-}CEH)$, $t_{w}(CEH)$, $t_{su}(D\text{-}CEH)$, $t_{w}(CE)$, $t_{h}(D)$, t_{WHWH}, t_{WHGL}, t_{WHQV2}, t_{WHRL}, t_{VPEH}, t_{QVVL}

Note) While the data signals is in output mode, do not apply an opposit phase signal.

12. Block Erase and Data Write Characteristics
(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		MIN	TYP	MAX	UNIT
Block Pair Erase Time	Vpp=4.5~5.5V	–	1.1	10	s
	Vpp=11.4~12.6V	–	1.0	10	
Block Pair Write Time	Vpp=4.5~5.5V	–	0.5	2.1	
	Vpp=11.4~12.6V	–	0.4	2.1	

13. Voltage Timing (Ta = 25℃)

$3.5V < V_{IH} < Vcc + 0.3$
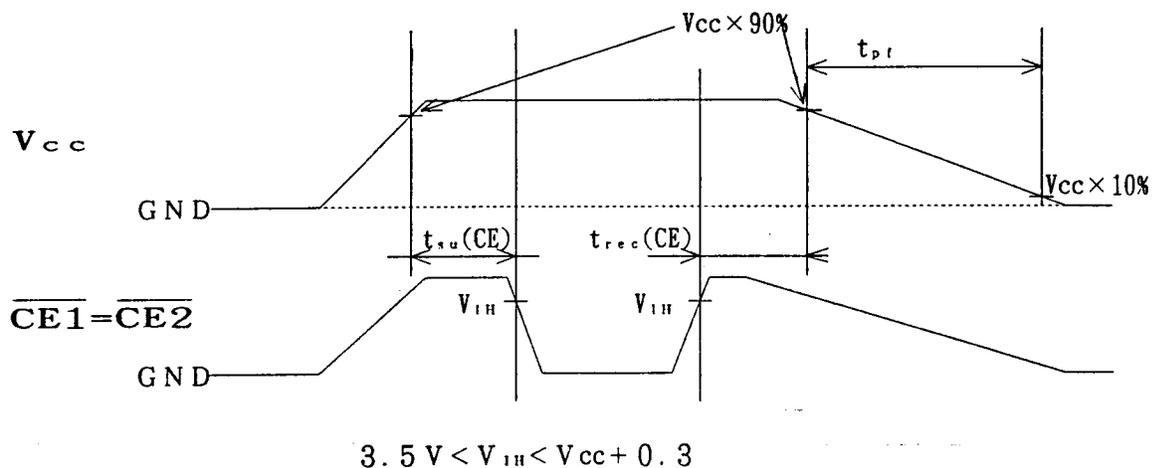
PARAMETER	SYMBOL	MIN	MAX	UNIT
$\overline{CE}$ Setup Time	$t_{su}(CE)$	4.0	–	ms
$\overline{CE}$ Recovery Time	$t_{rec}(CE)$	1.0	–	μs
Vcc Falling Time	t_{pf}	3.0	300	ms

Note)
1. When Vcc(4.5~5.5V) is applied to the memory card and you are inserting or removing the card, $\overline{CE1}$, $\overline{CE2}$ should both be high-impedance. At such a time, other signal line should also be hi-impedance. After inserting the memory card, do not access it during the $\overline{CE}$ setup time(minimum of 4ms).
(During this time, neither $\overline{CE1}$ nor $\overline{CE2}$=“LOW”.)

2. When Vcc is turn on, if the condition(for example, Vcc rising time. etc) is not sufficient to as specified, it is possible that device's Status Register is not cleared or device not becomes to Read Array Mode. To prevent these, it is recommmended that using software command, reset the Status Register or set the device to Read Array Mode.
    ex.
    Reset the Status Register   50H(5050H)
    Set to Read Array Mode   FFH(FFFFH)

14. Attribute Memory

The attribute memory holds the attribute informations of the card such as
the type of card, bit configuration, speed and so on.
EEPROM Model
    Card has 2k bytes of EEPROM attribute memory. To read the attribute memory, set
    $\overline{REG}$="LOW" and perform a read with the same access timming as common memory read.
    For this operation, access time is 300ns maximum. To allow 2k bytes of attribute
    memory, even addresses from 0 to 4096 are reserved. Since only the even-numbered
    bytes are used, reading odd-numbered bytes will result in invalid data.
Note)We have another type of attribute memory as follows,
    No EEPROM Model. (Model no. ID244G02: 5 bytes device informations in even address
    0 to 8, read only in card's control circuit, with the same access timming as common
    memory read)

14.1 Attribute Memory Read/Write Function Chart

C E 1	C E 2	A 0	W E	O E	R E G	MODE	$D_0 \sim D_7$	$D_8 \sim D_{15}$	S T A T U S
H	H	X	X	X	X		High-Z	High-Z	Standby
L	H	L	H	L	L	Read (×8)	D_0(even byte)	High-Z	Byte Access
L	H	H	H	L	L		High-Z	High-Z	Standby
L	L	X	H	L	L	Read (×8)	D_0(even byte)	High-Z	Byte Access
H	L	X	H	L	L		High-Z	High-Z	Standby
L	H	L	L	H	L	Write (×8)	D_i(even byte)	xxx	Byte Access
L	H	H	L	H	L		xxx	xxx	Standby
L	L	X	L	H	L	Write (×8)	D_i(even byte)	xxx	Byte Access
H	L	X	L	H	L		xxx	xxx	Standby
L	X	X	H	L	L	Attribute Memory Address 0~8	D_0	High-Z	Byte Access

H : High		D_i :	Input Data
L : Low		D_0 :	Output Data
X : High/Low not applicable		High-Z :	High Impedance
		xxx :	Don't Care

Notes:
1) When the write protect switch is in protect-mode, the WP output signal is "HIGH" and
   write operations (including attribute memory) are not allowed.
2) A0-A11 are attribute memory addresses. Addresses after A12 are not decoded, so care
   should be taken.

14.2 AC Characteristics (VCC=4.5V~5.5V, Ta=0~60℃)

Testing Conditions
    1)Input Pulse Level   : 0.8~3.5V
    2)Input Rise/Fall Time   : 10n s
    3)Input/Output Timing Reference Level : 1.5V
    4)Output Load Capacitance   : 1TTL+C_L (100pF)
                                              (including scope and jig capacitance)

14.3 Attribute Memory Read Cycle

(Vcc = 4.5~5.5V, Ta = 0~60℃)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Read Cycle Time	t_{CR}	t_{cR}	300	—	ns
Address Access Time	t_{ACC}	$t_a(A)$	—	300	
Card Enable Access Time	t_{CE}	$t_a(CE)$	—	300	
Output Enable Access Time	t_{OE}	$t_a(OE)$	—	150	
Output Disable Time from $\overline{CE}$		$t_{dis}(CE)$	—	100	
Output Disable Time from $\overline{OE}$	t_{DF}	$t_{dis}(OE)$	—	100	
Output Enable Time from $\overline{CE}$		$t_{en}(CE)$	5	—	
Output Enable Time from $\overline{OE}$		$t_{en}(OE)$	5	—	
Data Valid from Add Change	t_{OH}	$t_v(A)$	0	—	

○ Attribute Memory Read Cycle
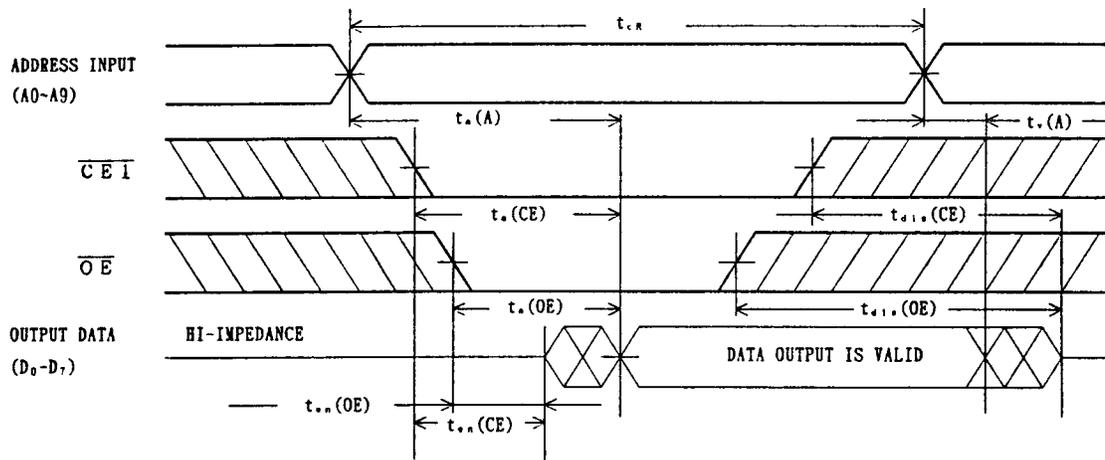
Note: 1. To read attribute memory, $\overline{REG}$="LOW", $\overline{WE}$="HIGH" and either $\overline{CE2}$="LOW" or else
   $\overline{CE2}$="HIGH" and A0="LOW".
   2. The output data becomes valid when last interval, ta(A), ta(CE) or
   ta(OE) have concluded.

14.4 Attribute Memory Write Cycle

$\overline{WE}$ Controlled   (Vcc = 4.5V ~ 5.5V, Ta = 0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time	twc	tcw	10	—	m s
Write Pulse Width	twP	tw(WE)	180	—	n s
Address Setup Time	tAS	tsu(A)	10	—	
Data Setup Time for $\overline{WE}$	tDS	tsu(D-WEH)	100	—	
Crad Enable Setup Time	tcES	tsu(CE)	0	—	
Output Enable Setup Time	toES	tsu(OE-WE)	45	—	
Address Hold Time	tAH		260	—	
Write Hold Time	tcH		0	—	
Output Enable Hold Time	toEH		70	—	
$\overline{WE}$ HIGH Hold Time	twEH		9.9	—	m s
Data Hold Time	tDH	th(D)	80	—	n s

$\overline{CE}$ Controlled   (Vcc = 4.5V ~ 5.5V, Ta = 0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time	twc	tcw	10	—	m s
Write Pulse Width	twP	tw(CE)	210	—	n s
Address Setup Time	tAS	tsu(A)	10	—	
Data Setup Time for $\overline{CE}$	tDS	tsu(D-CEH)	100	—	
Write Enable Setup Time	twES	tsu(WE)	0	—	
Output Enable Setup Time	toES	tsu(OE-CE)	45	—	
Address Hold Time	tAH		260	—	
Write Hold Time	twH		0	—	
Output Enable Hold Time	toEH		70	—	
$\overline{CE}$ HIGH Hold Time	tcEH		9.9	—	m s
Data Hold Time	tDH	th(D)	80	—	n s

○ Attribute Memory Write Cycle (WE Controlled)

○ Attribute Memory Write Cycle (CE Controlled)
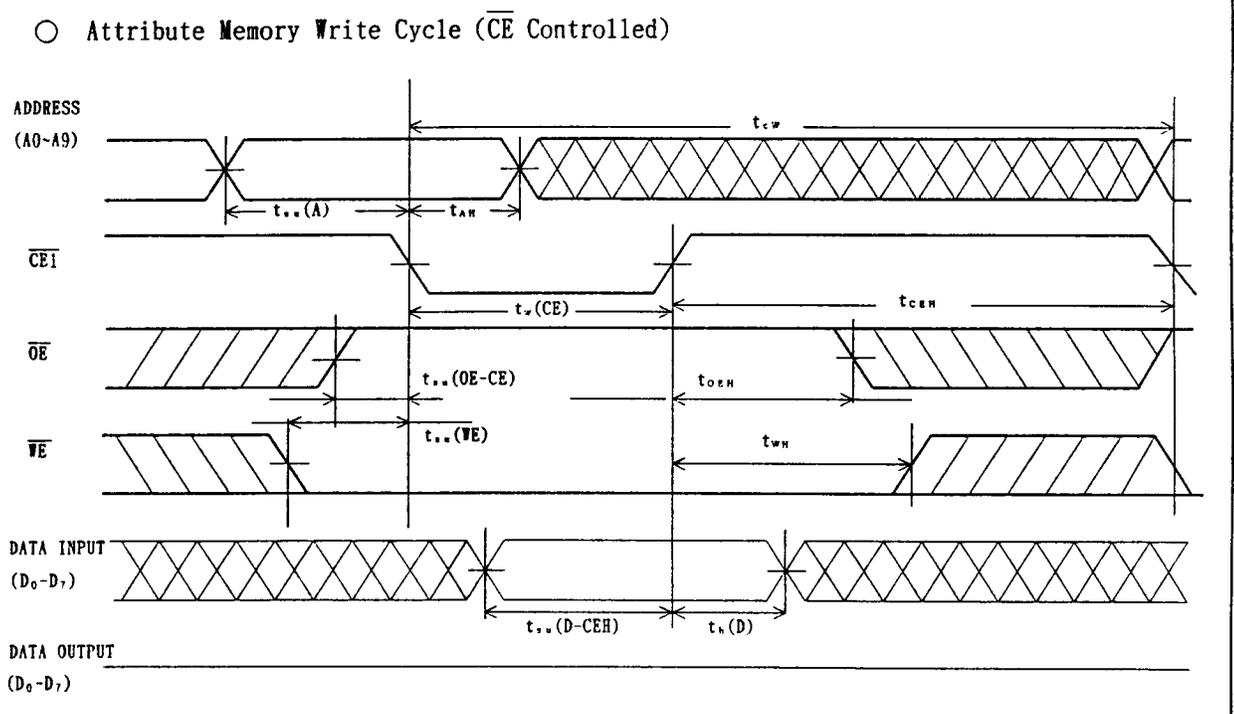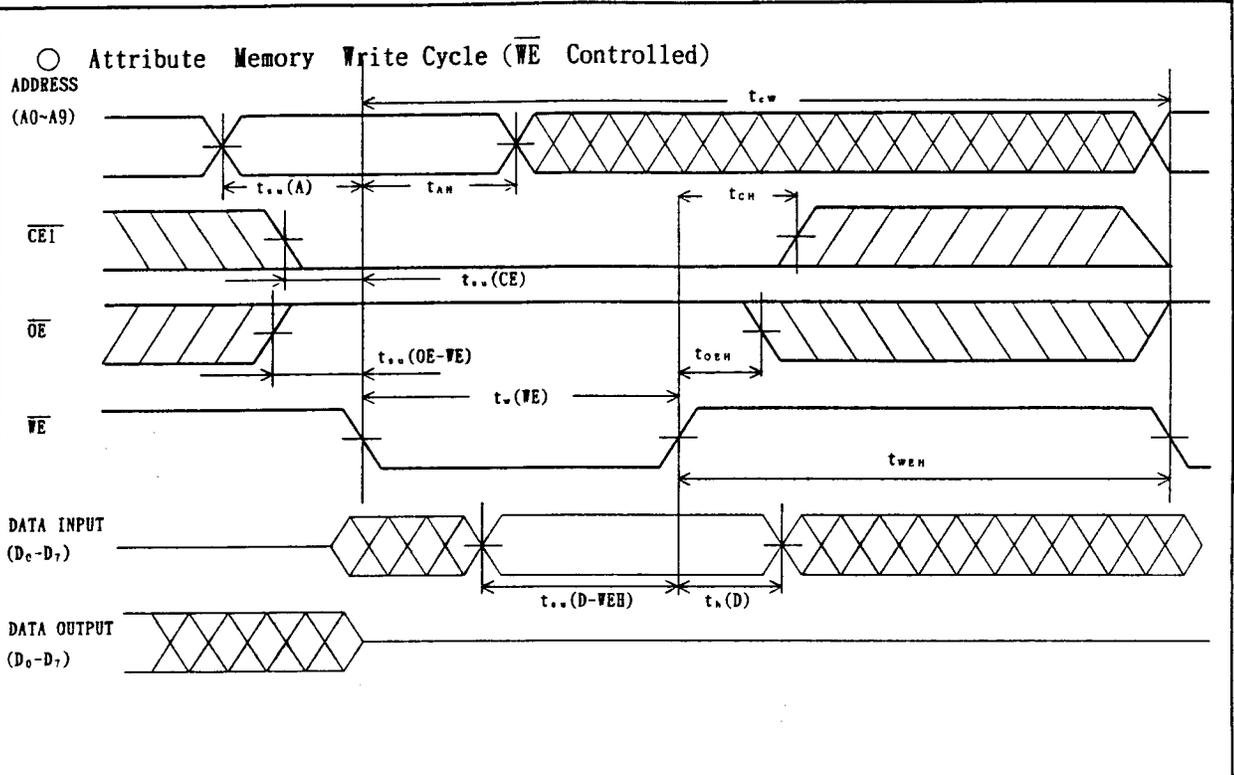
Note: To write attribute memory, REG="LOW" and either CE2="LOW" or else CE2="HIGH" and A0="LOW".

15. Specification Changes
    Specifications may be changed upon discussion and agreement between both parties.

16. Othes Precautions
    - Permanent damage occures if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
    - Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
    - Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
    - Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
    - Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
    - When the memory card is not being used, return it to its protective case.
    - Do not allow the memory card to come in contact with fire.

SHARP

(A) ENLARGEMENT OF THE

WRITE-PROTECT SWITCH

17. External Diagrams

Protected
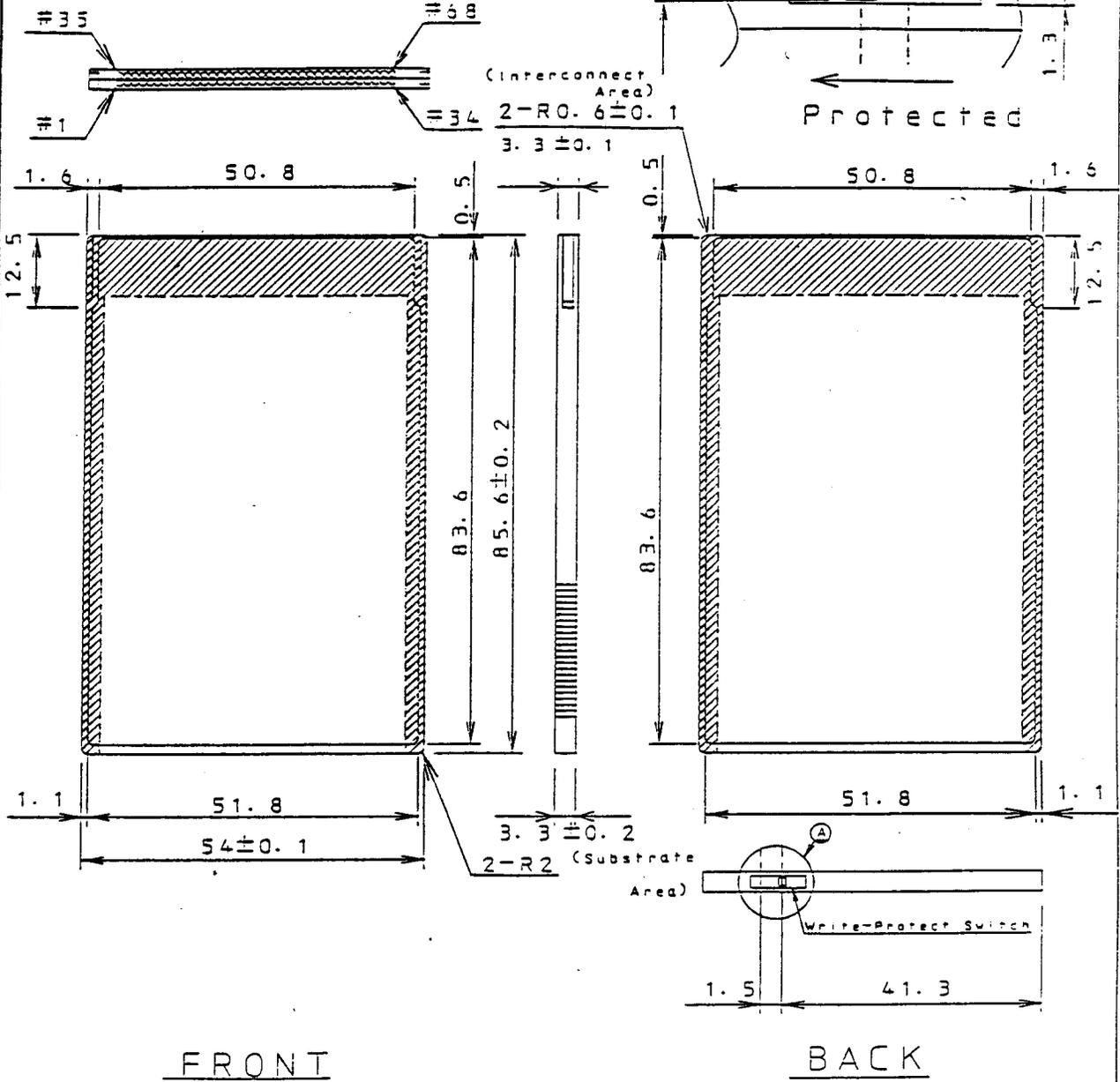
FRONT

BACK

APPLICABLE			SCALE	UNIT	(A)			
MODEL			1/1	mm	(A)	CH. DATE	REVISE	CHARGE
THICKNESS		MATERIAL		FINISH		NAME	MEMORY. CARD	
							EXTERNAL DIAGRAM	
DATE	1994. 11. 16						PCMCIA Rel. 2. 0 TYPE	
DESIGN	DRAW	TRACE	CHECK	APPROVE	Memory Card Business Project Team			
			TENRI IC GROUP					
			SHARP CORPORATION			DRAWING NO.	IMC001-A102	

19. EXTERNAL APPEARANCES

CONNECTOR SIDE

▲MEMORY CARD

FLASH MEMORY

8MB

SHARP

FRONT PANEL

Note

1 端子に、手をふれないで下さい。
   Do not touch the terminals.

2 カードを曲げたり、落としたり、衝撃を
   与えないで下さい。
   This card should not be subject to
   flexing or expose to impact.

3 熱、湿気、直射日光をさけて下さい。
   Avoid heat, moisture and direct sunlight.

MEMO

NO.

WRITE PROTECT

PC Card
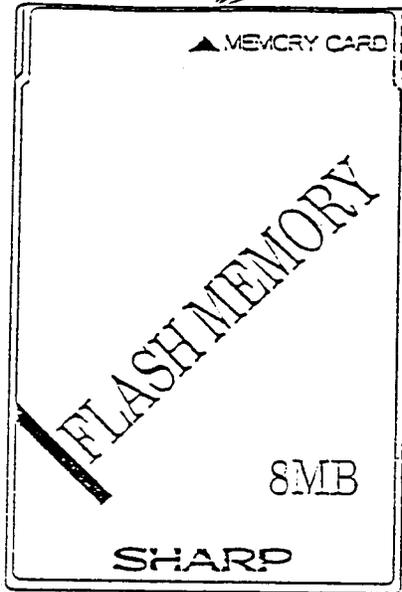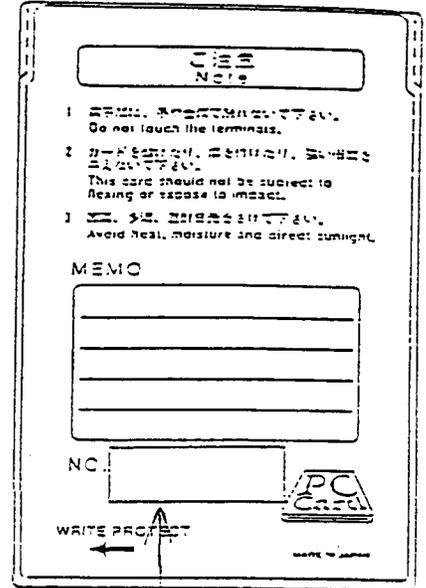
LABELING POSITION

BACK PANEL

LABEL SIZE AND DENOTATIONS

20

8

ID244G01

YWWUUSSSS

Model No.

Serial No.

User Code

Week of the year

Lowest number of AC
(199Y years WW the week)
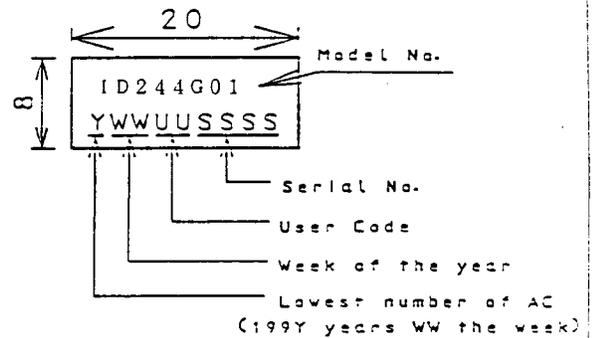
APPLICABLE MODEL	ID244G01		SCALE	UNIT	Ⓐ			
				mm	Ⓐ			
					CH. DATE	REVISE	CHARGE
THICKNESS	DEFFERENCE	MATERIAL	FINISH		NAME			
DATE	1995. 10. 10							
			MEMORY CARD BUSINESS PROJECT TEAM					
			INTEGRATED CIRCUITS GROUP		DRAWING NO.			
			SHARP CORPORATION					

18. PACKING SPECIFICATION

ID24XXXX

Connector Side

Connector Side

IC Memory Card

Back Panel

Label the Model No. and Manufacturing No.

Note 4

Front Panel

IC Memory Card

Flexible Plastic Case

x25

Ⓑ Inner Carton
(25 pieces contained)

x4

Ⓒ Outer Carton
(100 pieces contained)

x4

Ⓓ Outer Case
(400 pieces contained)
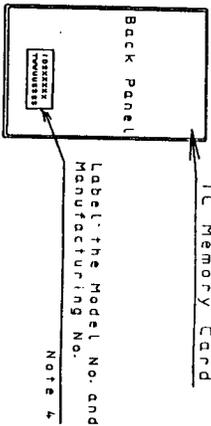
Parts List

	Parts Name
A	Flexible Plastic Case
B	Inner Carton (25 pieces contained)
C	Outer Carton (100 pieces contained)
D	Outer Case (400 pieces contained)
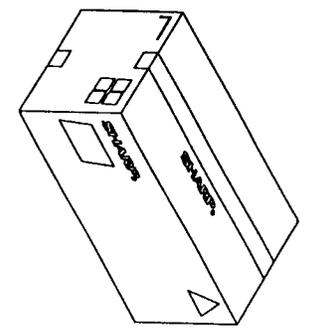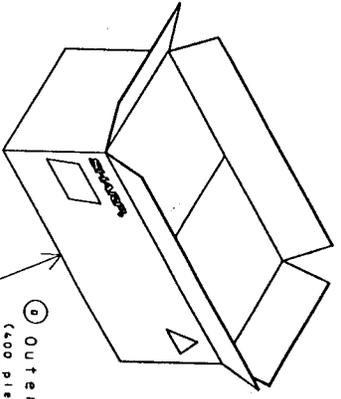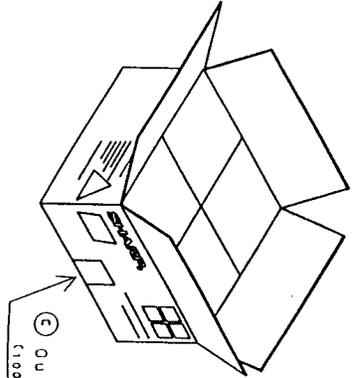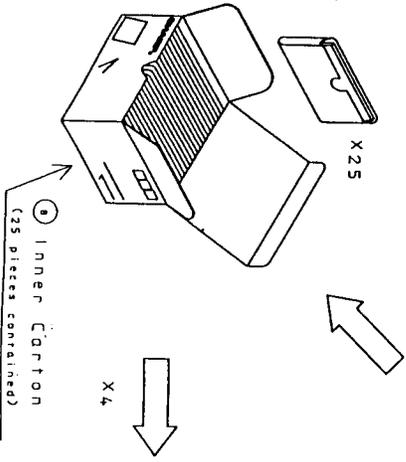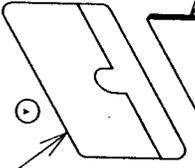
Packing Specification

1. Label the Model No. and Manufacturing No. on the back panel of the card.

2. Each Memory Card is contained in the flexible plastic case. (The front side of the card comes to the place where the card is released and the connector side is placed against this point, so that the connector is not touched by finger, as shown in the figure.)

3. The inner carton contains 25 pieces of the card with the case. (Note 1.)

4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is then attached on inner carton.

5. The outer carton contains 4 inner cartons. (Note 2.)

6. The product name, Lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is then attached on the outer carton.

7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)

8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is then attached on the case.

Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.

3. The other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.

4. Size of label and denotations are following. (unit:mm)

├─ 8 ─┤

ID2XXXXX
YWWUUSSSS

20

Serial No.
User Code
Week of the Year
Lowest number of AC
(1994 years WW the week)
Model No.
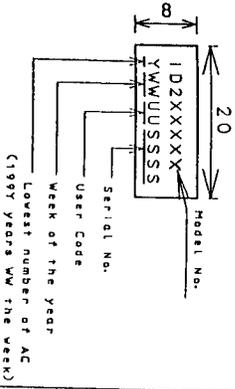
	APPLICABLE MODEL	THICKNESS	DIFFERENCE	MATERIAL	FINISH		
	ID2XXXXX						

DATE 1995. 10. 0

SCALE | UNIT | A
mm | CH.DATE | REVISE | CHARGE

INTEGRATED CIRCUITS GROUP
MEMORY IC&B BUSINESS PROJECT TEAM

NAME ID2XXXXX Packing Specification

SHARP CORPORATION

DRAWING No. IMC02S-J300

32

Flash cards, 8 MByte Memory, PCMCIA linear, ID244G01