Integrated Device Technology, Inc.

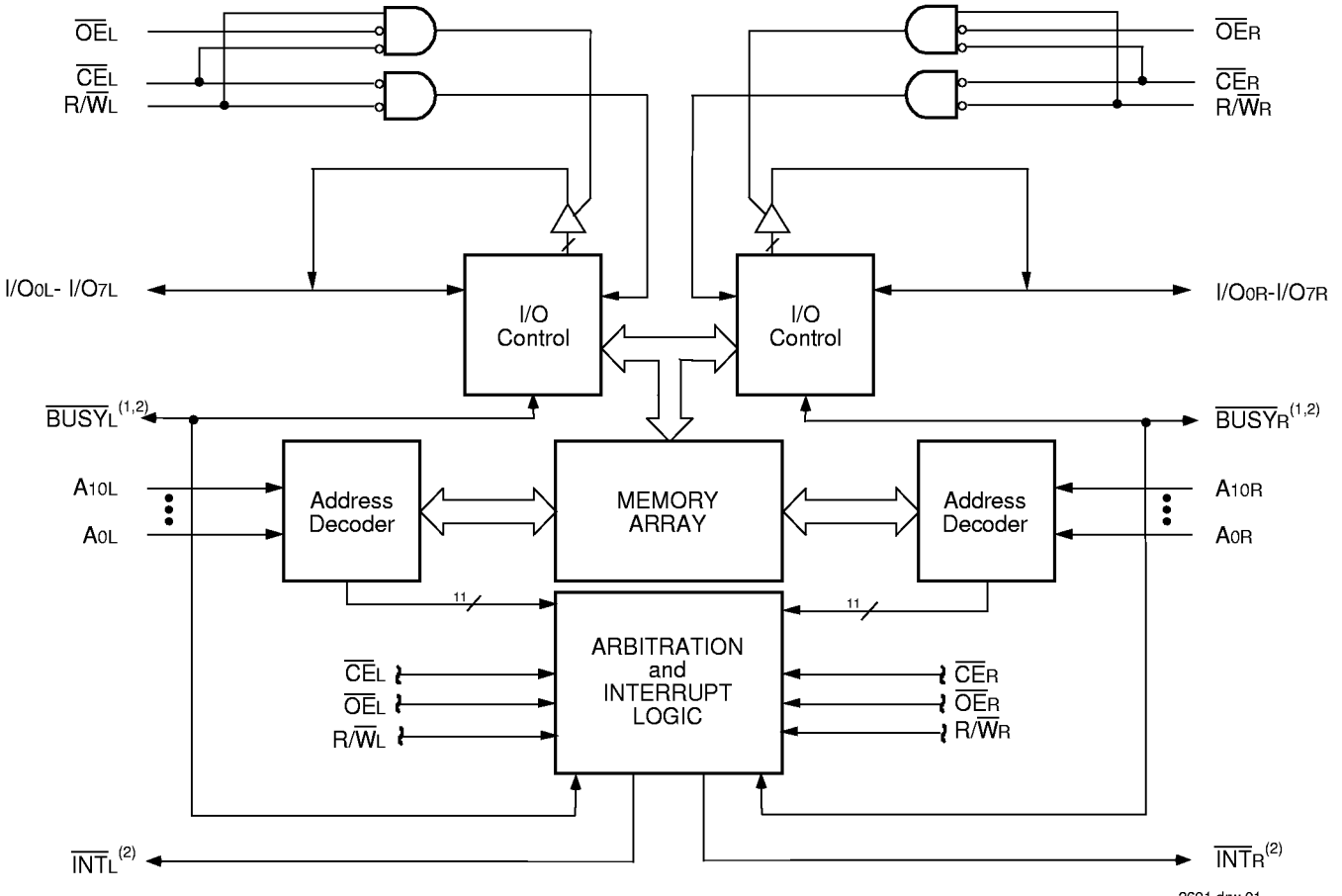
HIGH SPEED 2K X 8 DUAL-PORT STATIC RAM WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  - —Commercial: 20/25/35/55ns (max.)
  - —Industrial: 55ns (max.)
- Low-power operation
  - —IDT71321/IDT71421SA
    - Active: 550mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT71321/421LA
    - Active: 550mW (typ.)
    - Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation –2V data retention (LA only)
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Industrial temperature range (–40°C to +85°C) is available for selected speeds

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT71321 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor of 270Ω.
   IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor of 270Ω.

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DESCRIPTION:

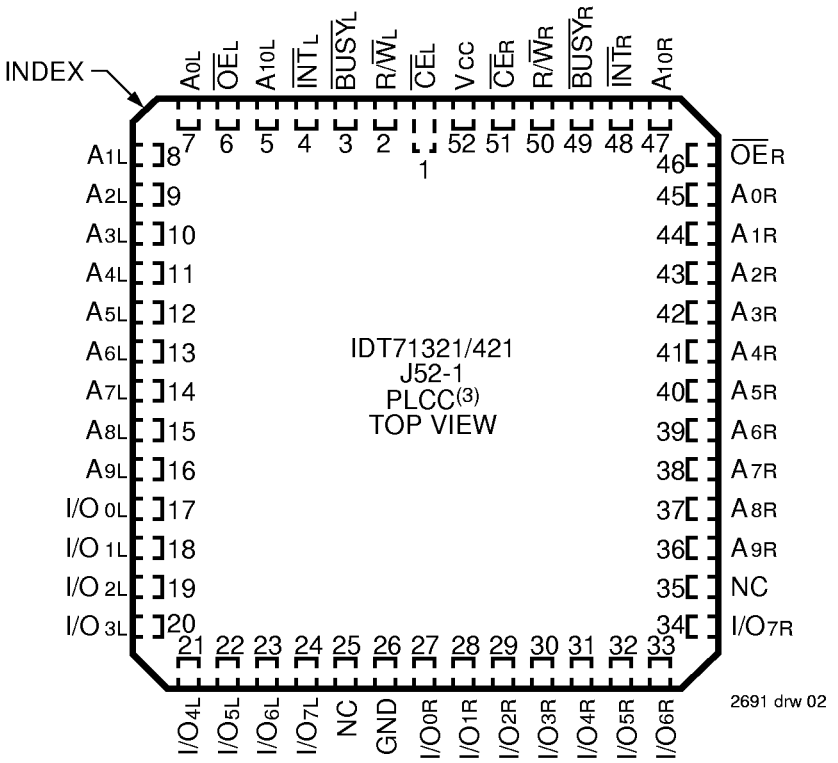
The IDT71321/IDT71421 are high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit Dual-Port Static RAM or as a "MASTER" Dual-Port Static RAM together with the IDT71421 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port Static RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin PLCCs, 64-pin TQFPs, and 64-pin STQFPs.

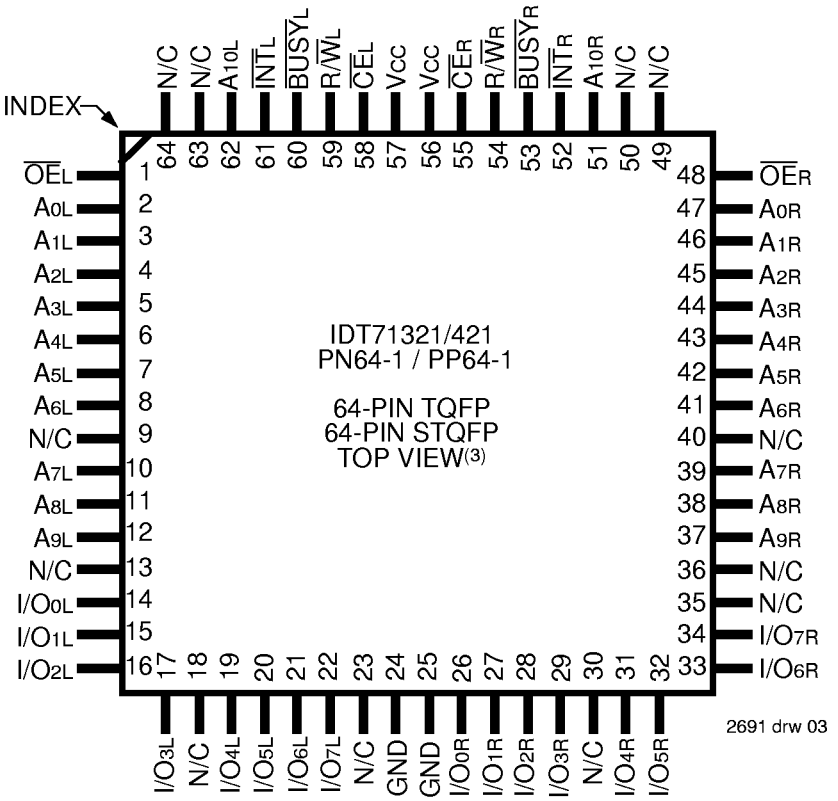
PIN CONFIGURATIONS[1,2]



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS[1,2] (CON'T.)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial & Industrial	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

2691 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2691 tbl 02

NOTES:
1. This is the parameter TA.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

2691 tbl 03

NOTES:
1. VIL (min.) = -3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 10%.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,5,7] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		71321X20[2] 71421X20[2] Com'l Only Typ.	71321X20[2] 71421X20[2] Com'l Only Max.	71321X25 71421X25 Com'l Only Typ.	71321X25 71421X25 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Open f = f_{MAX}[3]	COM'L	S	110	250	110	220	mA
				L	110	200	110	170	
			IND	S	—	—	110	280	
				L	—	—	110	220	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[3]	COM'L	S	30	65	30	65	mA
				L	30	45	30	45	
			IND	S	—	—	30	80	
				L	—	—	30	60	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[6] Active Port Outputs Open, f=f_{MAX}[3]	COM'L	S	65	165	65	150	mA
				L	65	125	65	115	
			IND	S	—	—	65	160	
				L	—	—	65	125	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
			IND	S	—	—	1.0	30	
				L	—	—	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[6] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	60	155	60	145	mA
				L	60	115	60	105	
			IND	S	—	—	60	155	
				L	—	—	60	115	

2691 tbl 04a

Symbol	Parameter	Test Condition	Version		71321X35 71421X35 Com'l & Ind Typ.	71321X35 71421X35 Com'l & Ind Max.	71321X55 71421X55 Com'l & Ind Typ.	71321X55 71421X55 Com'l & Ind Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Open f = f_{MAX}[3]	COM'L	S	80	165	65	155	mA
				L	80	120	65	110	
			IND	S	80	230	65	190	
				L	80	170	65	140	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[3]	COM'L	S	25	65	20	65	mA
				L	25	45	20	35	
			IND	S	25	80	20	65	
				L	25	60	20	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[6] Active Port Outputs Open, f=f_{MAX}[3]	COM'L	S	50	125	40	110	mA
				L	50	90	40	75	
			IND	S	50	150	40	125	
				L	50	115	40	90	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L	S	1.0	15	1.0	15	mA
				L	0.2	4	0.2	4	
			IND	S	1.0	30	1.0	30	
				L	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[6] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	45	110	40	100	mA
				L	45	85	40	70	
			IND	S	45	145	40	110	
				L	45	105	40	85	

2691 tbl 04b

NOTES:
1. 'X' in part numbers indicates power rating (SA or LA).
2. PLCC package only.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. Vcc = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\,DC}$ = 100mA (Typ)
6. Port "A" may be either left or right port. Port "B" is opposite from port "A".
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	71321SA 71421SA		71321LA 71421LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[1]	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} - 5.5V	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$/$\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2691 tbl 05

NOTE:
1. At Vcc ≤ 2.0V leakages are undefined.

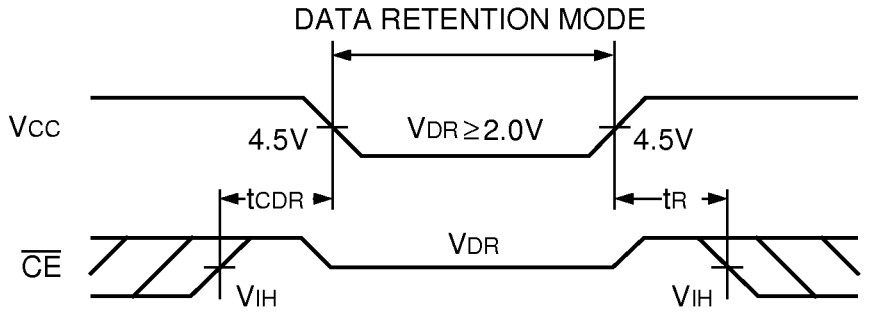
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	0	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE}$ ≥ V_{CC} - 0.2V	COM'L	—	100	1500	µA
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	IND	—	100	4000	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2691 tbl 06

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

DATA RETENTION WAVEFORM



2691 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

2691 tbl 07

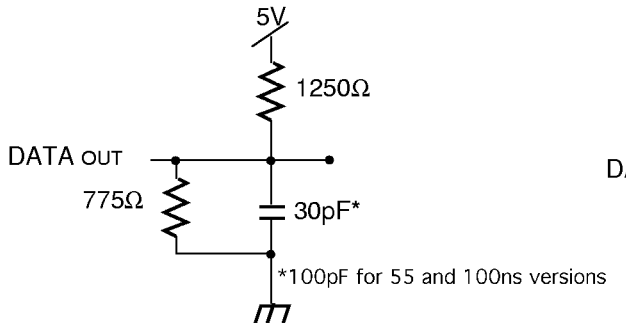


Figure 1. AC Output Test Load

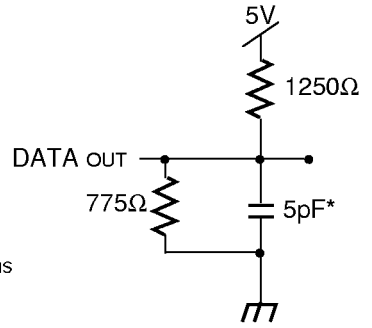
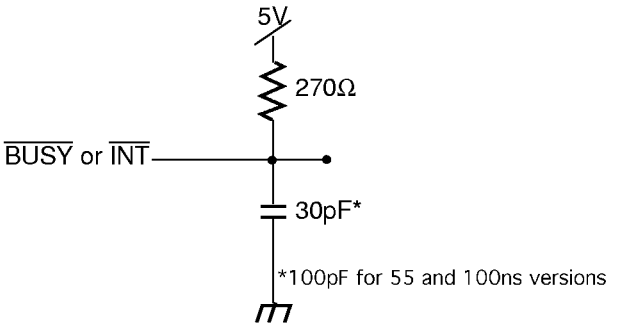


Figure 2. Output Test Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})
* Including scope and jig.



2691 drw 05

Figure 3. $\overline{BUSY}$ and $\overline{INT}$
AC Output Test Load

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2,4]

Symbol	Parameter	71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	11	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,3]	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,3]	—	10	—	10	ns
t_{PU}	Chip Enable to Power Up Time[3]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[3]	—	20	—	25	ns

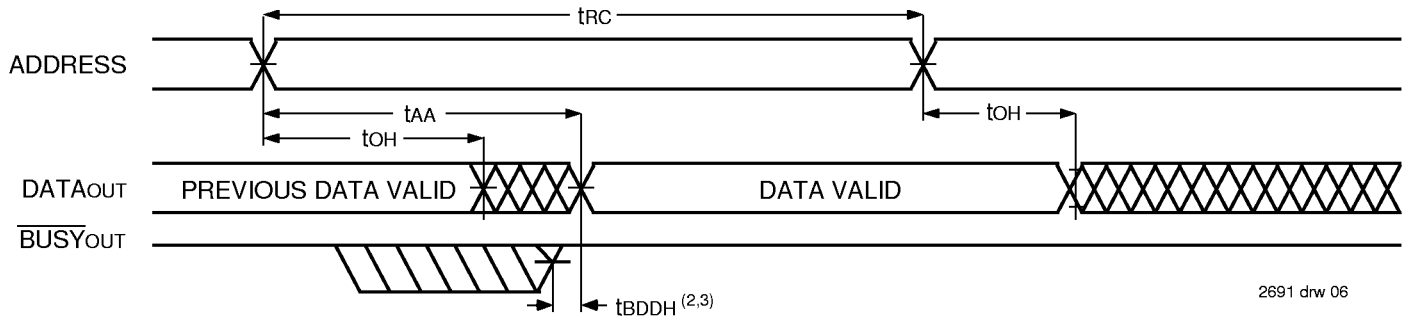
2691 tbl 08a

Symbol	Parameter	71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,3]	0	—	5	—	ns
t_{HZ}	Output High-Z Time[1,3]	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time[3]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[3]	—	35	—	50	ns

2691 tbl 08b

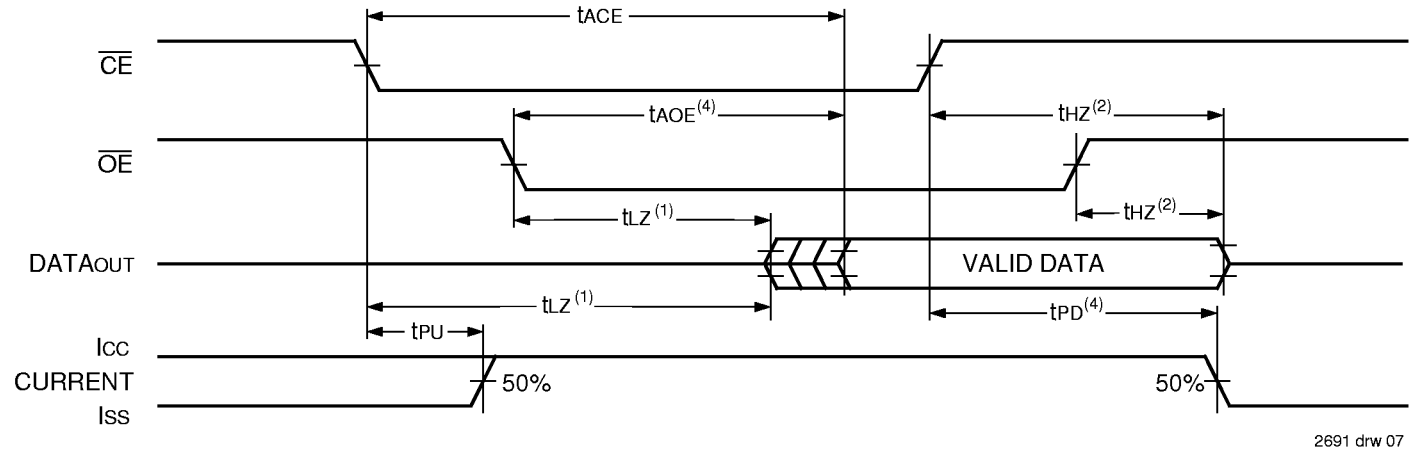
NOTES:
1. Transition is measured ±500mV from Low or High-impedance voltage Output Test Load (Figure 2).
2. "X" in part numbers indicates power rating (SA or LA).
3. This parameter is guaranteed by device characterization, but is not production tested.
4. Industrial temperature: for other speeds, packages and powers contact your sales office.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1)



NOTES:
1. R/$\overline{W}$ = V_{IH}, $\overline{CE}$ = V_{IL}, and is $\overline{OE}$ = V_{IL}. Address is valid prior to the coincidental with $\overline{CE}$ transition LOW.
2. t_{BDD} delay is required only in the case where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA}, and t_{BDD}.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deaserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH} and $\overline{OE}$ = V_{IL}, and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA}, and t_{BDD}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4,6]

Symbol	Parameter	71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time[2]	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	15	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	12	—	ns
t_{HZ}	Output High-Z Time[1]	—	10	—	10	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	10	—	10	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	ns

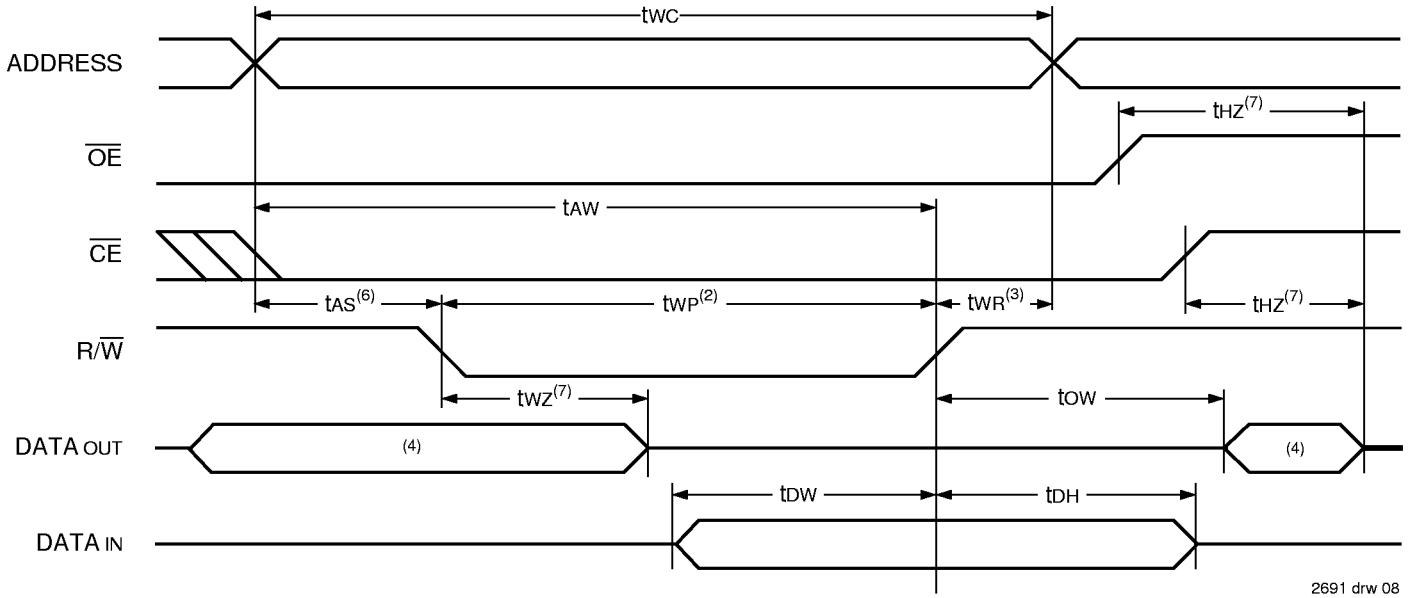
2691 tbl 09a

Symbol	Parameter	71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time [2]	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1]	—	15	—	25	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	ns

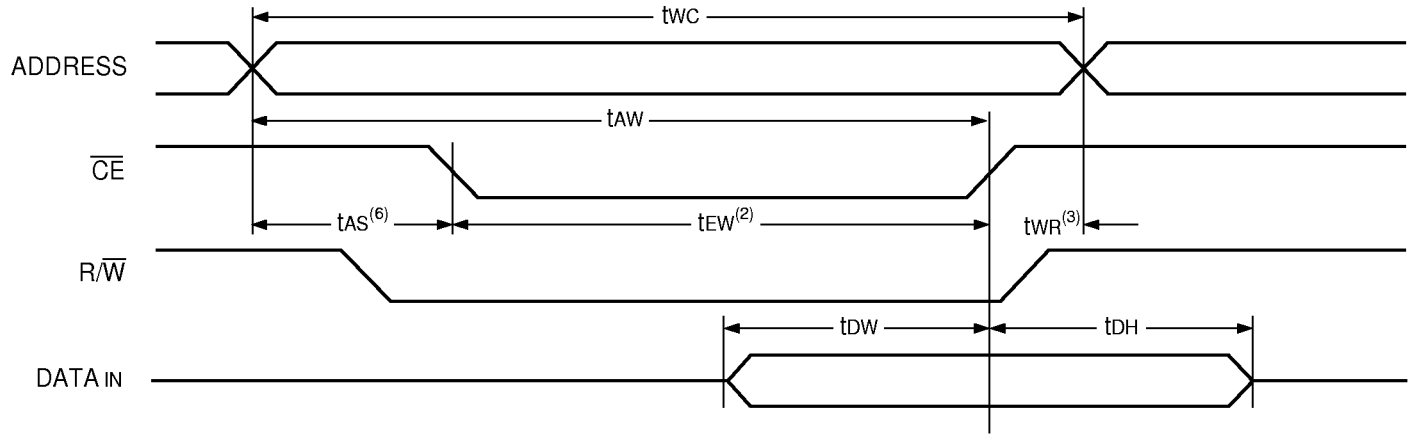
2691 tbl 09b

NOTES:
1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. For Master/Slave combination, $t_{WC} = t_{BAA} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after t_{BAA} .
3. If $\overline{OE}$ is LOW during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{DW})$ to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
4. "X" in part numbers indicates power rating (SA or LA).
5. Industrial temperature: for other speeds, packages and powers contact your sales office.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,5,8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,5)



NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of $\overline{CE}$ = V_{IL} and R/$\overline{W}$= V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured ±500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6,7)

Symbol	Parameter	71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (For MASTER 71321)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	25	—	35	ns
BUSY INPUT TIMING (For SLAVE 71421)						
t_{WB}	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	40	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	30	—	35	ns

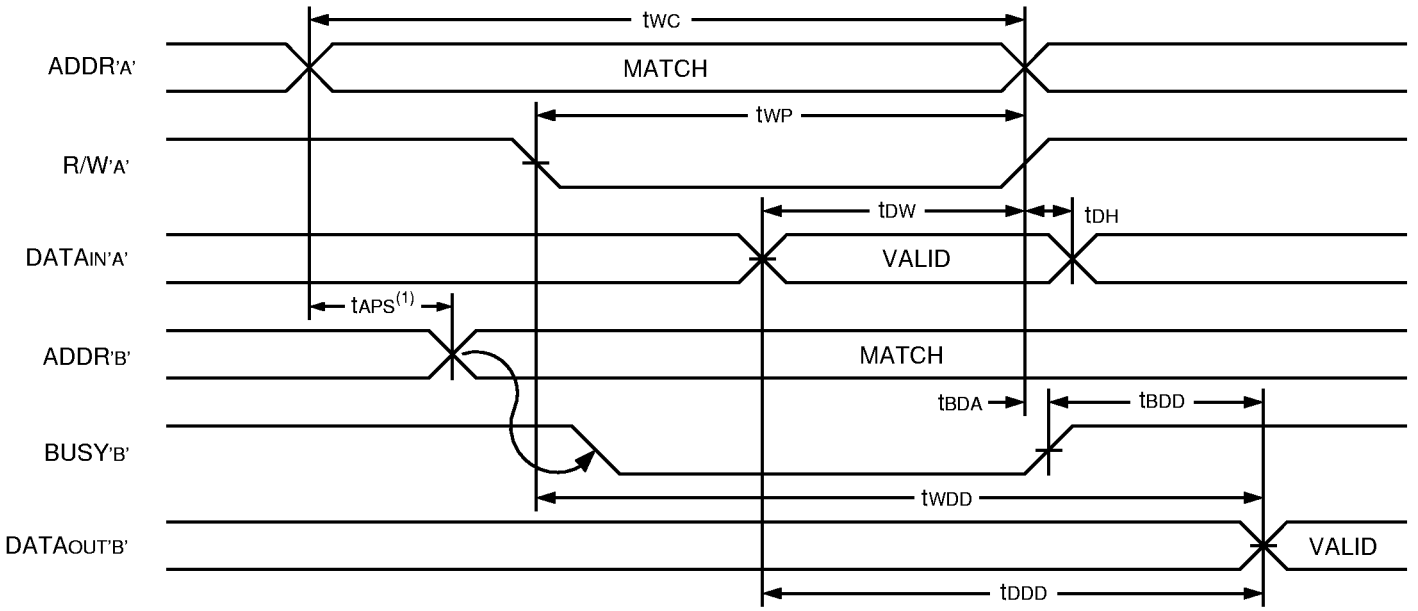
2691 tbl 10a

Symbol	Parameter	71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (For MASTER 71321)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	30	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	55	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	35	—	50	ns
BUSY INPUT TIMING (For SLAVE 71421)						
t_{WB}	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	55	ns

2691 tbl 10b

NOTES:
1. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$."
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that a write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

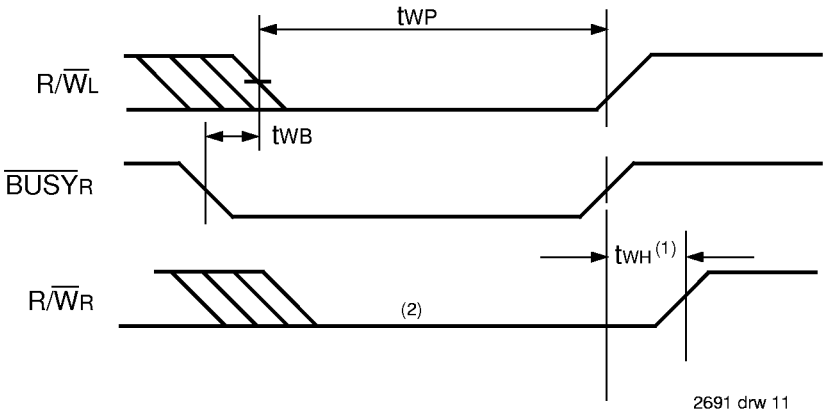
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$(2,3,4)



2691 drw 10

NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for Slave (71421).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

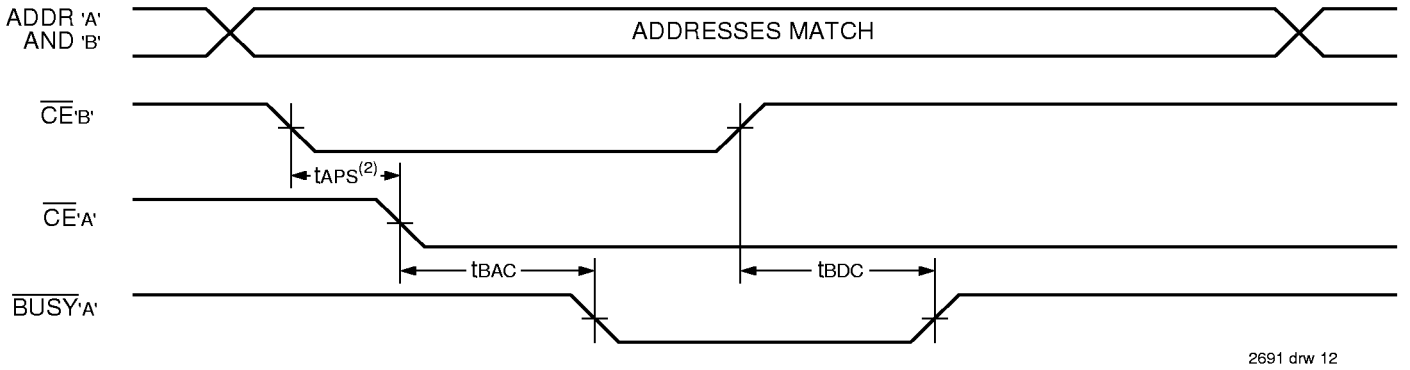
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$(3)



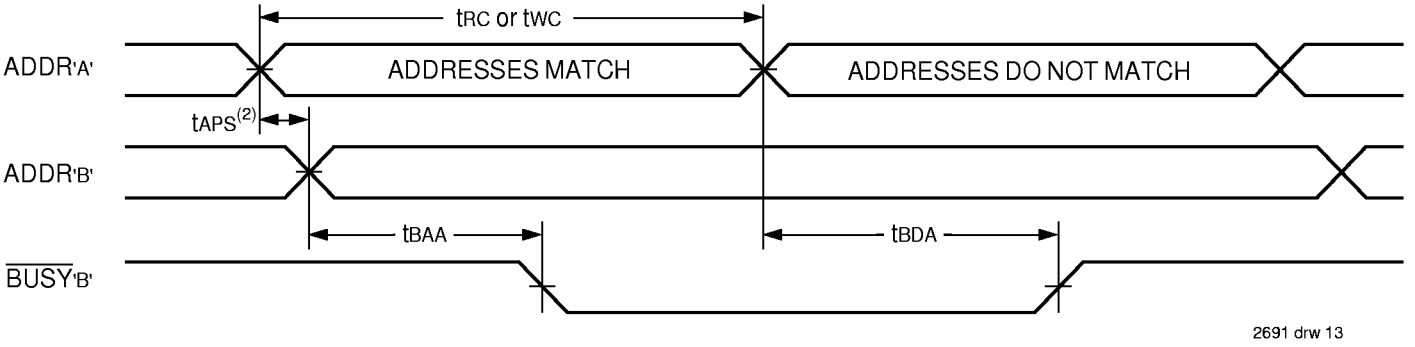
2691 drw 11

NOTES:
1. t_{WH} must be met for both $\overline{BUSY}$ Input (71421, slave) or Output (71321 master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking $R/\overline{W}_{B'}$, until $\overline{BUSY}_{B'}$ goes HIGH.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (1)



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING (1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (71321 only).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1,2)

		71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l Only		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	ns
tINR	Interrupt Reset Time	—	20	—	25	ns

2691 tbl 11a

NOTES:
1. "X" in part numbers indicates power rating (SA or LA).
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1,2)

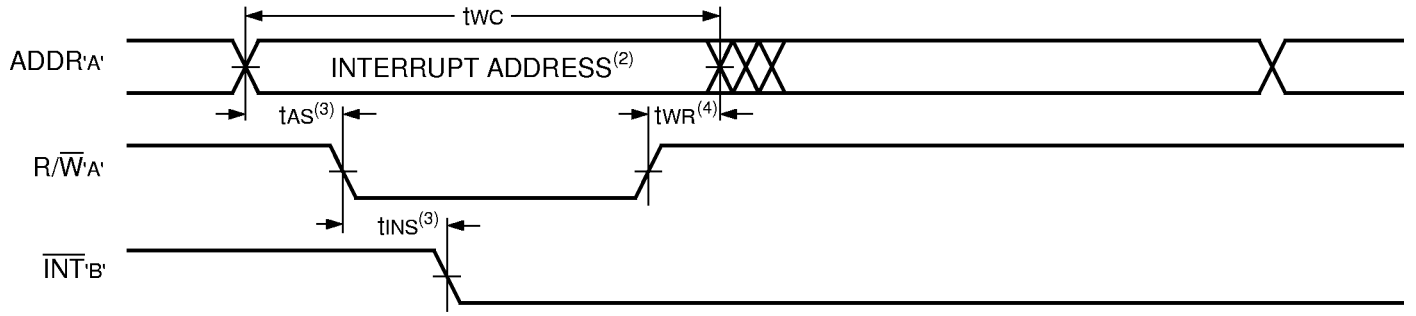
		71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	45	ns
t_{INR}	Interrupt Reset Time	—	25	—	45	ns

2691 tbl 11b

NOTES:
1. "X" in part numbers indicates power rating (SA or LA).
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

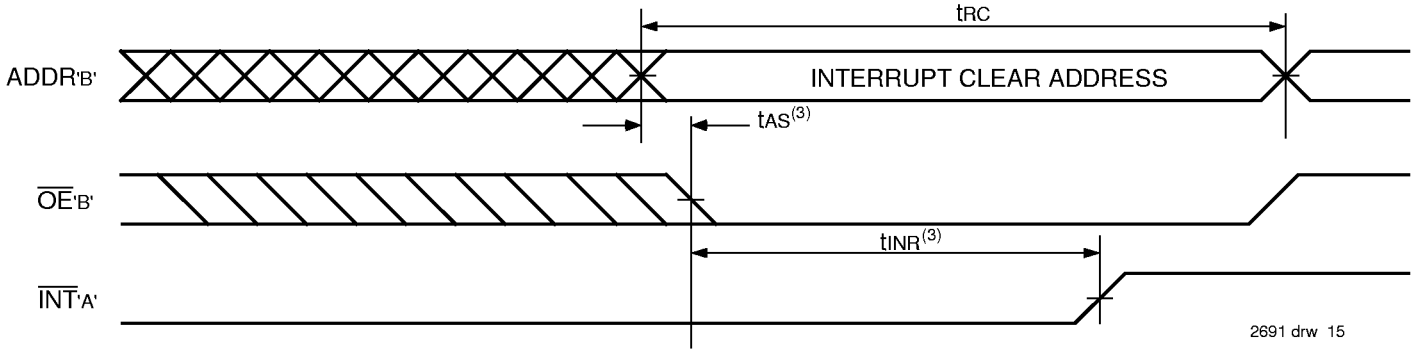
TIMING WAVEFORM OF INTERRUPT MODE

SET $\overline{INT}$



2691 drw 14

CLEAR $\overline{INT}$



2691 drw 15

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I. NON-CONTENTION READ/WRITE CONTROL(4)

Left or Right Port(1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2691 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TRUTH TABLE II. INTERRUPT FLAG(1,4)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{10L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{10R}-A_{0R}	$\overline{INT}_R$	
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2691 tbl 13

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TRUTH TABLE III — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2691 tbl 14

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for 71321 (master). Both are inputs for 71421 (slave). $\overline{BUSY}_X$ outputs on the 71321 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

FUNCTIONAL DESCRIPTION

The IDT71321/IDT71421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71321/IDT71421 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per Truth Table II. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table V for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT71321 (Master) are open drain type outputs and require open drain resistors to operate. If these SRAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array does not require the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an SRAM array in width while using busy logic, one master part is used to decide which side of the SRAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT71321/IDT71421 SRAMs the $\overline{BUSY}$ pin is an output if the part is Master (IDT7132), and the $\overline{BUSY}$ pin is an input if the part is a Slave (IDT7142) as shown in Figure 3.

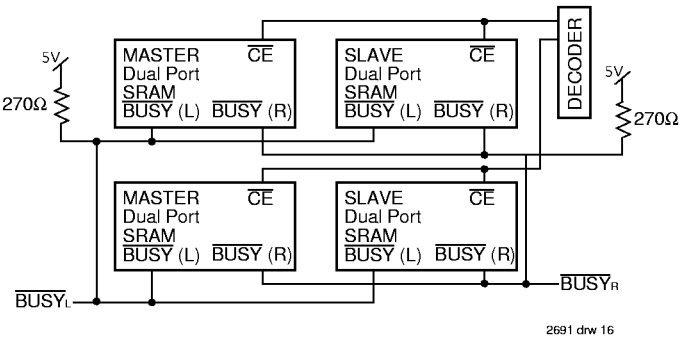
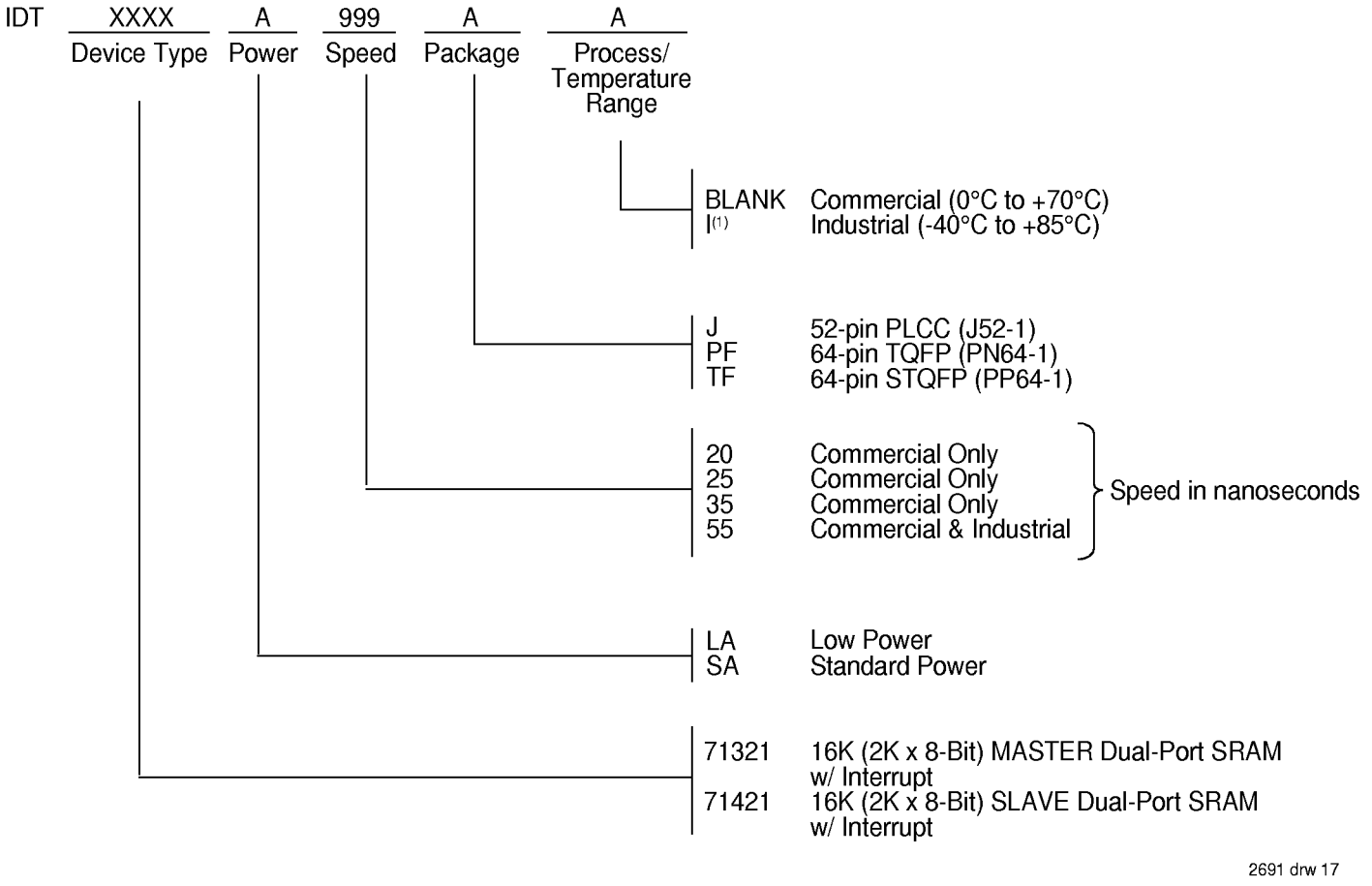


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT71321 (Master) and (Slave) IDT71421 RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

ORDERING INFORMATION



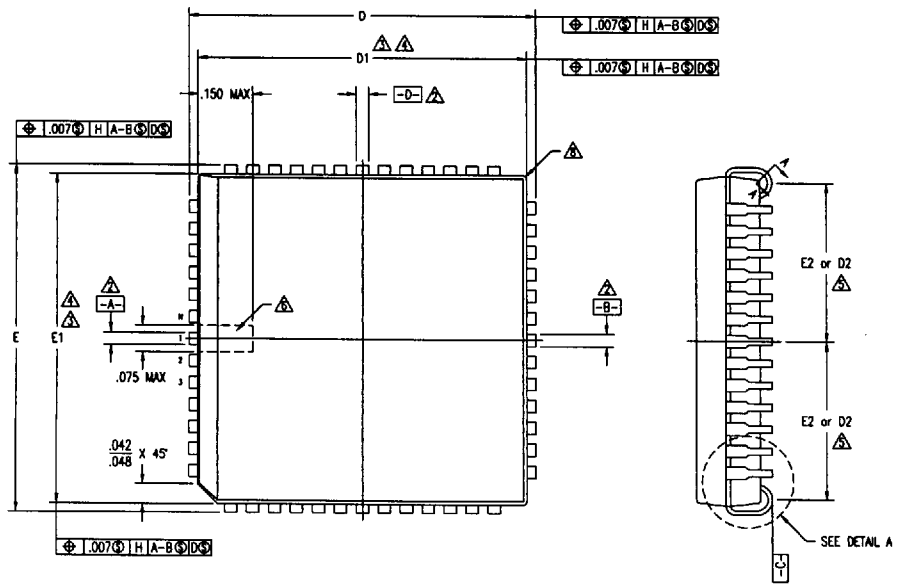
2691 drw 17

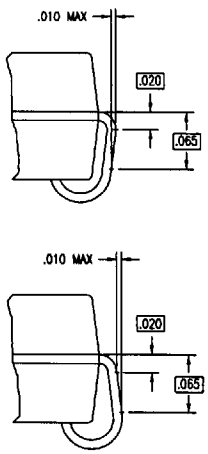
NOTES:

1. Industrial temperature range is available in selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office.

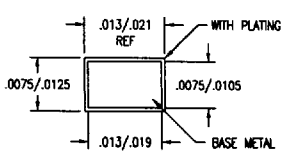
PLCC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	





DETAIL A ⚠



SECTION A-A ⚠

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL ANGULAR XX± ± XXX± XXXX±		
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/88	
CHECKED		SIZE C DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING

4825771 0021952 2TT

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.165	.172	.180	
A1	.095	.105	.115	
A2	.062	–	.083	
D	.485	.490	.495	
D1	.450	.453	.456	3,4
D2	.195	.205	.215	5
E	.485	.490	.495	
E1	.450	.453	.456	3,4
E2	.191	.205	.219	5
N	28			

DWG #	J44-1			
JEDEC VARIATION AC				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.685	.690	.695		
.650	.653	.656	3,4	
.295	.305	.315	5	
.685	.690	.695		
.650	.653	.656	3,4	
.291	.305	.319	5	
44				

DWG #	J52-1			
JEDEC VARIATION AD				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.785	.790	.795		
.750	.753	.756	3,4	
.345	.355	.365	5	
.785	.790	.795		
.750	.753	.756	3,4	
.341	.355	.369	5	
52				

DWG #	J68-1			
JEDEC VARIATION AE				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.985	.990	.995		
.950	.953	.956	3,4	
.445	.455	.465	5	
.985	.990	.995		
.950	.953	.956	3,4	
.441	.455	.469	5	
68				

DWG #	J84-1			
JEDEC VARIATION AF				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.059	–	.080		
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.545	.555	.565	5	
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.541	.555	.569	5	
84				

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	06/15/95
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

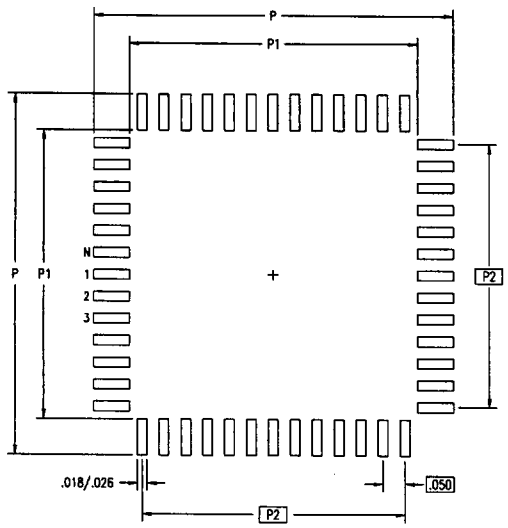
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	08	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



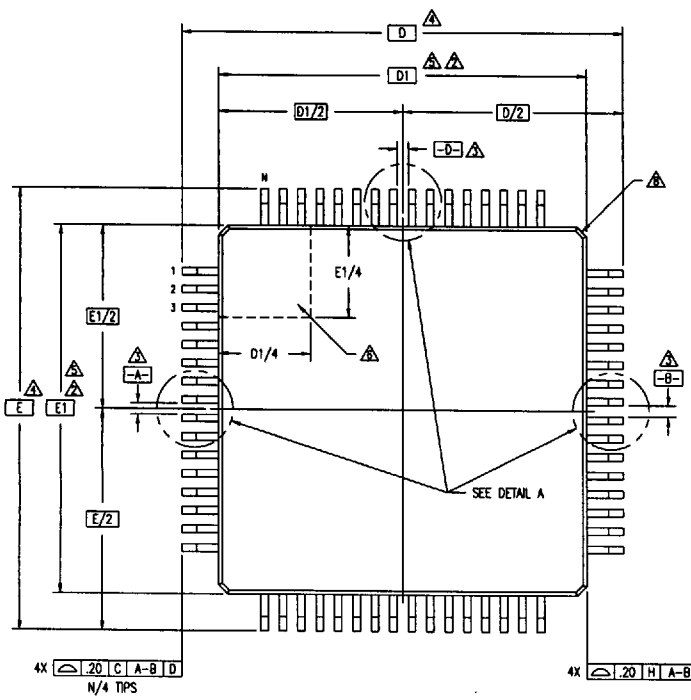
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

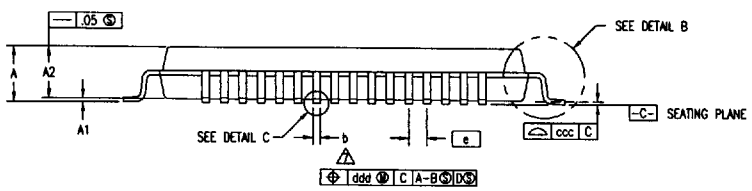
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH	
DRAWN dd	08/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	

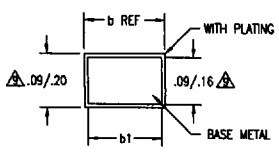
PACKAGE DIAGRAM OUTLINES

TQFP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	

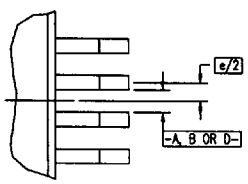




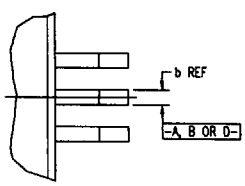


DETAIL C

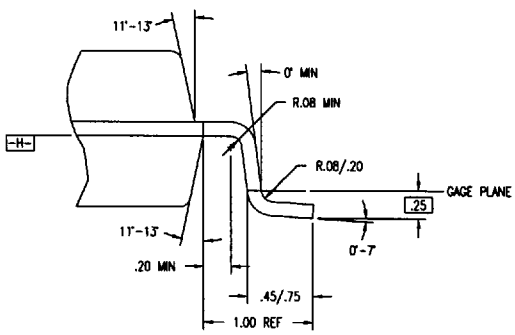
EVEN LEAD SIDES



ODD LEAD SIDES



DETAIL A



DETAIL B

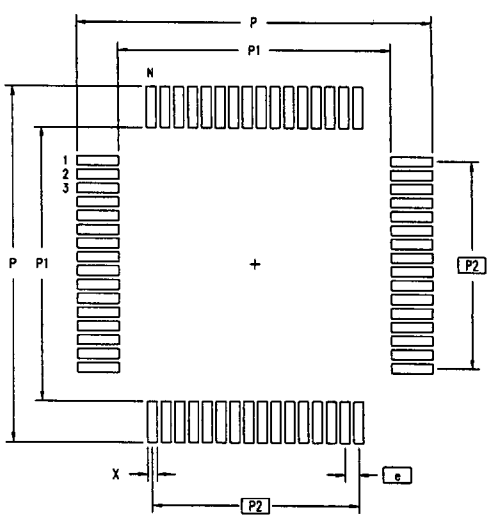
TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS / DRAWN AA 03/12/92 / CHECKED	TITLE: PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM	
	SIZE C	DRAWING No. PSC-4036 REV 03
	DO NOT SCALE DRAWING	

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

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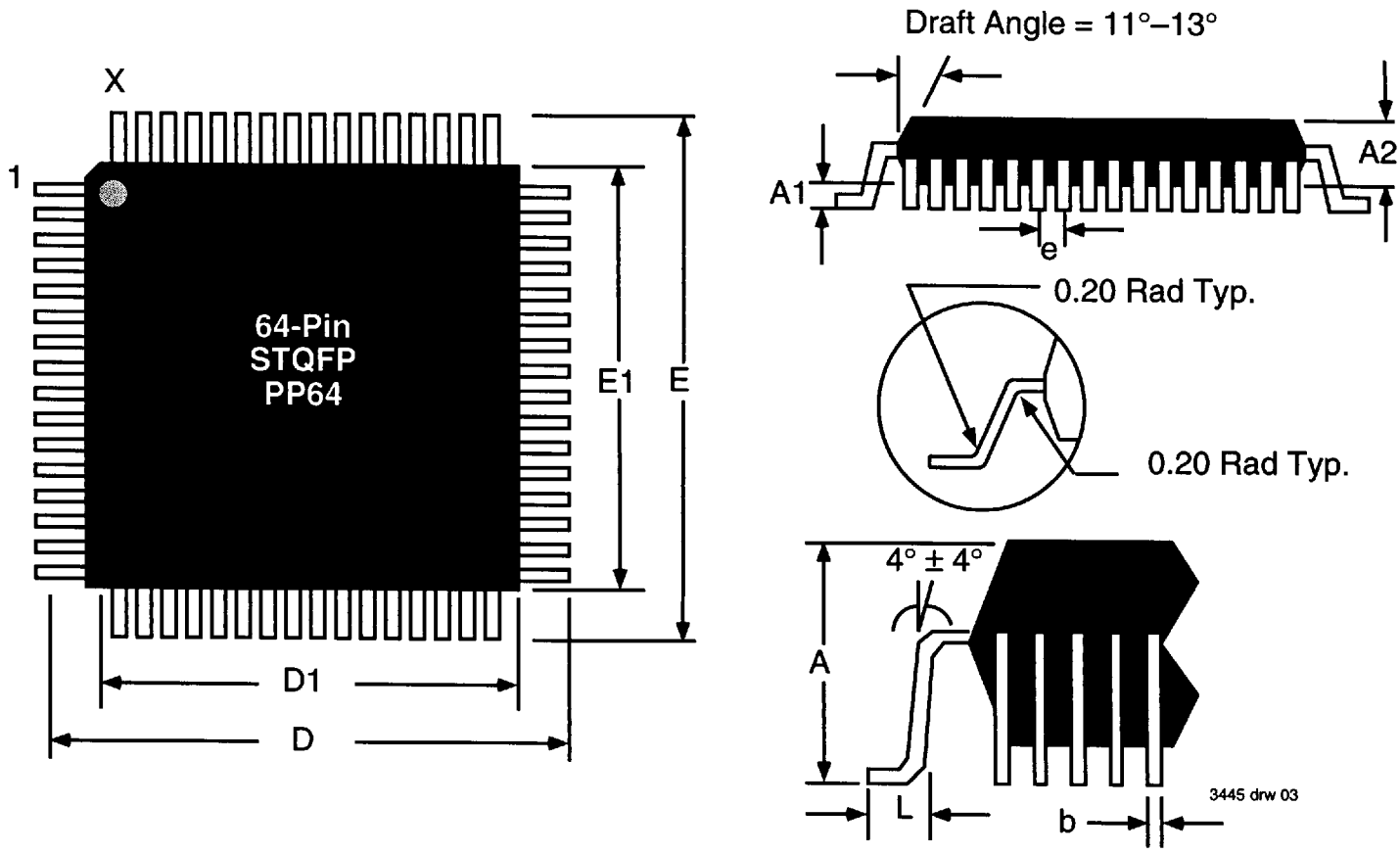
APPROVALS	DATE
DRAWN AA	03/12/92
CHECKED	

TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C | DRAWING No. PSC-4036 | REV 03

DO NOT SCALE DRAWING

PACKAGE DIMENSIONS



DIMENSIONS

64-PIN STQFP WITH 10MM BODY

DImension Letter	Tolerance (mm)	Dimension (mm)
A	Max.	1.60
A1	±.05	0.10
A2	±.05	1.45
D	±.10	12.00
D1	±.10	10.00
E	±.10	12.00
E1	±.10	10.00
L	±15	0.60
e	Basic	0.50
b	.05	0.22

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