INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8208M

Extended PCI Arbiter

Preliminary Specification V0.3

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Revision History

Section	Revision	Page No.
6	• The MAX. value of V_{IL} in section 6 DC Characteristics was revised to ‘VCC x **0.3**’. • The MAX. value of V_{IH} has been removed.	11

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1. Features

- **Extended PCI Arbiter**
  - Supports 1 PCI arbiter to extend 1 set of SYSGNT# and SYSREQ#, which can be utilized to support 3 PCI Masters
- **Input PCI Clock**
  - Supports input clock frequency from 25MHz to 66MHz
- **16-pin SOP**

2. General Description

The IT8208M incorporates an extended PCI arbiter to support more PCI master bus request.

The extended PCI arbiter utilizes one set of SYSGNT# and SYSREQ# to support 3 PCI Masters, so that two more PCI Masters can be supported for the system. PCISTOP# input signal is useful to facilitate the fairness arbitration. The algorithm of this arbiter uses a rotation arbitration priority that is illustrated in Figure 2-1**.**

The PCI bus clock can support frequency from 25 MHz to 66 MHz. The IT8208M is available in 16 SOP package.

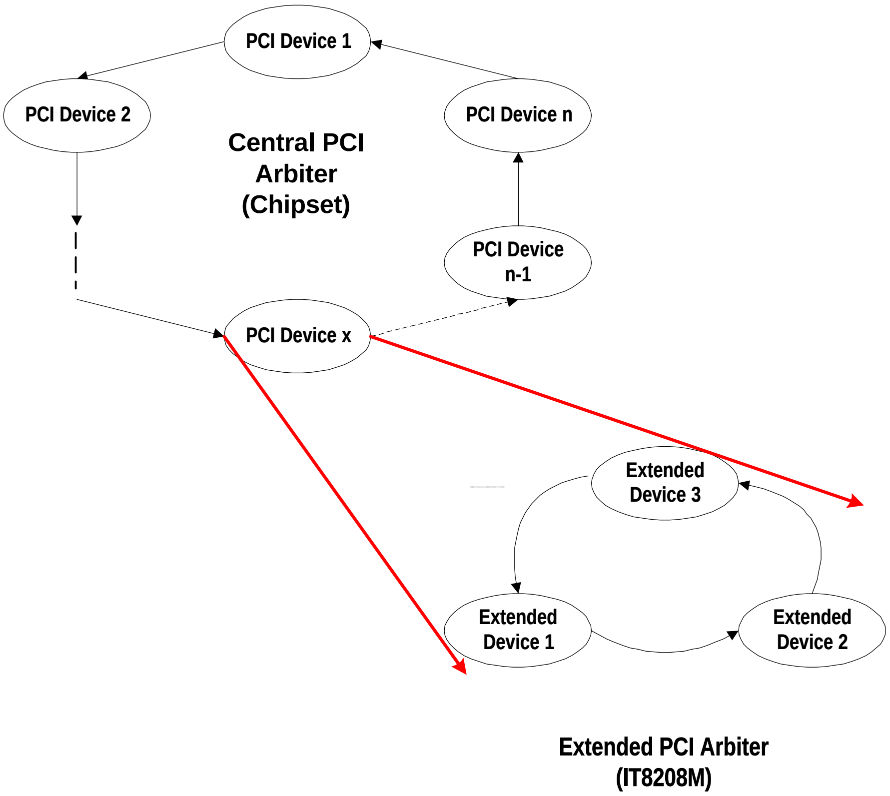


Figure 2-1. Arbitration Scheme of IT8208M

3. Block Diagram

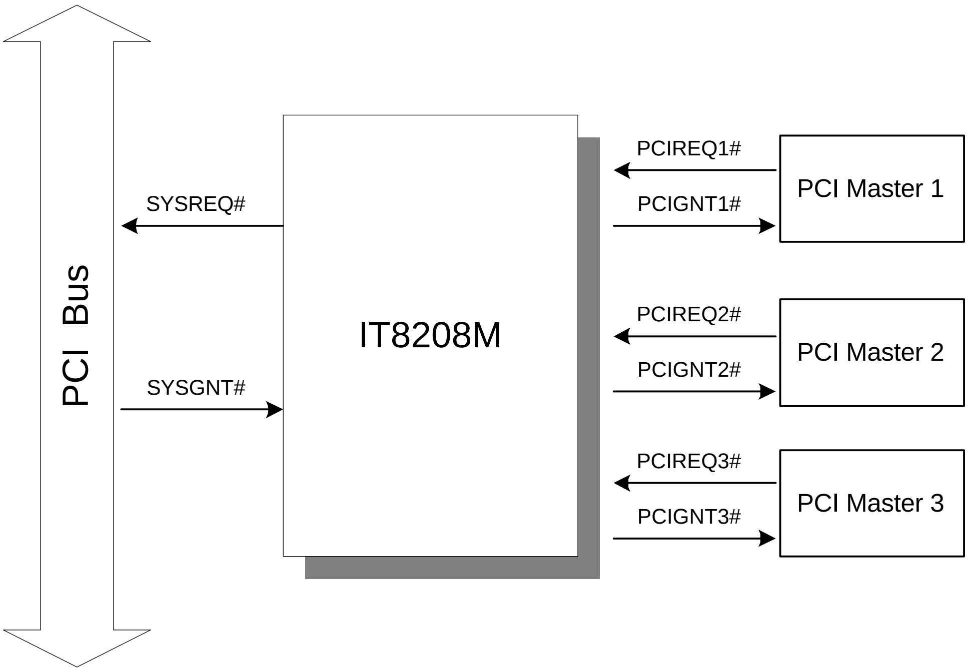
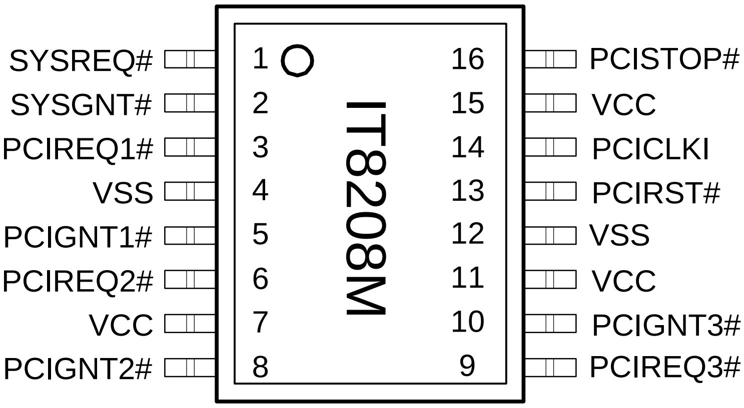


Figure 3-1. Extended PCI Arbiter Scheme

4. Pin Configuration



Pin	Signal	Pin	Signal
1	SYSREQ#	9	PCIREQ3#
2	SYSGNT#	10	PCIGNT3#
3	PCIREQ1#	11	VCC
4	VSS	12	VSS
5	PCIGNT1#	13	PCIRST#
6	PCIREQ2#	14	PCICLKI
7	VCC	15	VCC
8	PCIGNT2#	16	PCISTOP#

Table 4-1. Pins Listed in Numeric Order

5. IT8208M Pin Descriptions

Table 5-1. Pin Descriptions of Extended PCI Arbiter

Signal	Pin(s) No.	Attribute	Description
Extended PCI Arbiter Signals (3.3V CMOS I/F, 5V tolerant)			
PCISTOP#	**16**	PIU	***PCI Bus STOP# Signal***
SYSREQ#	**1**	O12	***PCI Bus Request***
SYSGNT#	**2**	PIU	***PCI Bus Grant***
PCIREQ1#	**3**	PIU	***Request Signal from Extended PCI Master 1***
PCIGNT1#	**5**	O12	***Grant Signal to Extended PCI Master 1***
PCIREQ2#	**6**	PIU	***Request Signal from Extended PCI Master 2***
PCIGNT2#	**8**	O12	***Grant Signal to Extended PCI Master 2***
PCIREQ3#	**9**	PIU	***Request Signal from Extended PCI Master 3***
PCIGNT3#	**10**	O12	***Grant Signal to Extended PCI Master 3***
PCIRST#	**13**	IK	***PCI Bus RST# Signal***

Table 5-2. Pin Descriptions of PCI Bus Clock

Signal	Pin(s) No.	Attribute	Description
PCI Bus Clock Signals (3.3V CMOS I/F)			
PCICLKI	**14**	I	***PCICLK Input***

Table 5-2. Pin Descriptions of Power/Ground Signals

Signal	Pin(s) No.	Attribute	Description
Power Ground Signals			
VSS	**4, 12**	I	***Ground***
VCC	**11, 15**	I	***Power Supply of 3.3V***

Notes: IO cell types are described as below:

I: Input PAD.
IK: Schmitt Trigger Input PAD.
PIU: PCI Bus Specified Input PAD (integrated a 75K ohms pull-up resistor).
O12: 12mA Output PAD.

6. DC Characteristics (VCC = 3.3V±0.3V. Ta=0°C to 70°C)

Absolute Maximum Ratings*

Applied Voltage of VCC, AVCC............-0.3V to +4.6V

Input Voltage of 3.3V Interface ......-0.3V to VCC+0.3V

Input Voltage of 5V tolerant Interface ...-0.3V to 5.25V

Tcase...0°C to +70°C

Storage Temperature .... -40°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Ta = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Conditions
V_{IL}	Input Low Voltage	- 0.3V		VCC x **0.3**	VCC=3.0 ~ 3.6V
V_{IH}	Input High Voltage	VCC x 0.7			VCC=3.0 ~ 3.6V
V_{OL}	Output Low Voltage			0.5	I_{OL}= -12mA
V_{OH}	Output High Voltage	2.4			I_{OH}= 12mA
I_{IL}	Input Low Current	-1µA		1µA	V_{IL}= V_{SS} no pull-up or pull-down
I_{IH}	Input High Current	-1µA		1µA	V_{IH}= VCC no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10µA		10µA	
Cin	Input Capacitance		3pF		
Cout	Output Capacitance		3pF		
Cbld	Bi-directional Buffer		3pF		
R_I	Input Pull-Up Resistance	40KΩ	75KΩ	170KΩ	V_{IL} =0V

7. AC Characteristics

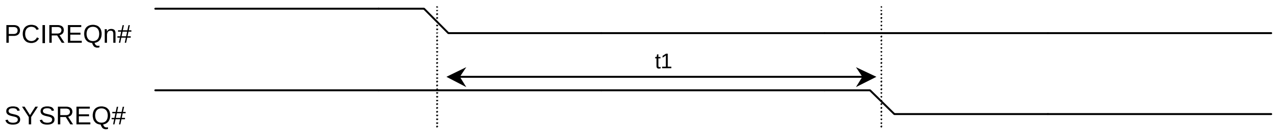


Figure 7-1. PCI Request Delay Timing

Table 7-1. PCI Request Delay Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PCIREQn# (n=1, 2, 3) to SYSREQ# asserted	0	-	7	ns

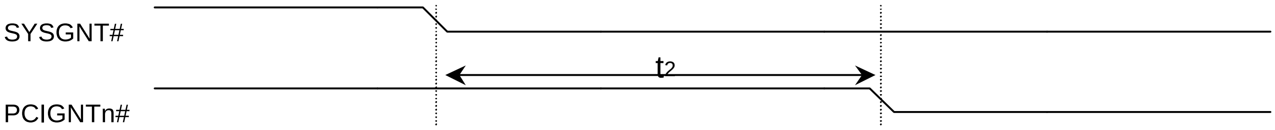


Figure 7-2. PCI Grant Delay Timing

Table 7-2. PCI Grant Delay Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_2	SYSGNT# to PCIGNTn# (n=1, 2, 3) asserted	0	-	8.5	ns

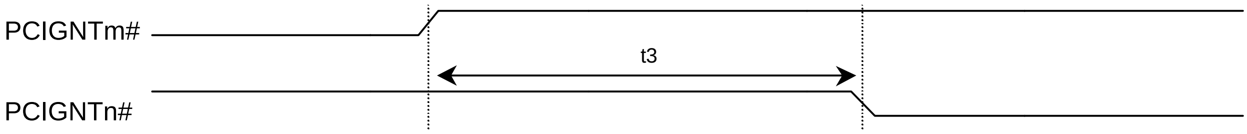


Figure 7-3. PCI Grant Separation Timing

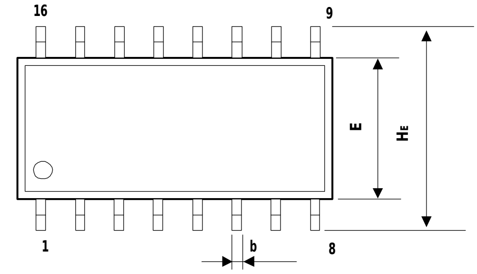
Table 7-3. PCI Grant Separation Timing Table

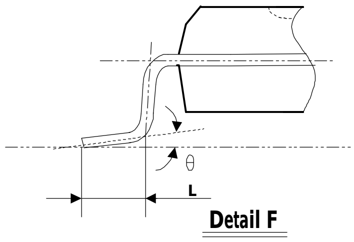
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_3	PCIGNTm# (m=1, 2, 3) deasserted to PCIGNTn# (n=1, 2, 3) asserted ($n \neq m$)	1	-	-	Clock Period

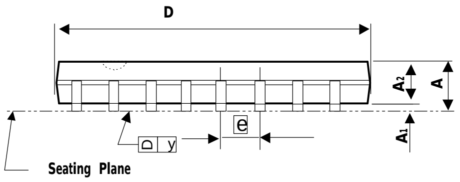
8. Package Information

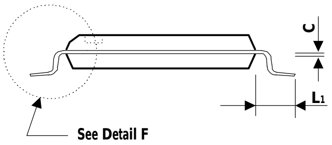
SOP16L Outline Dimensions

unit: inches/mm









Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.053	0.064	0.069	1.35	1.63	1.75
A_1	0.004	0.006	0.010	0.10	0.15	0.25
A_2	0.051	0.055	0.059	1.30	1.40	1.50
b	0.013	0.016	0.020	0.33	0.41	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.386	0.390	0.394	9.80	9.91	10.01
E	0.150	0.154	0.157	3.80	3.90	4.00
e	0.050BSC			1.27BSC		
H_E	0.228	0.236	0.244	5.80	6.00	6.20
L	0.016	0.025	0.050	0.40	0.64	1.27
L_1	0.042REF.			1.07REF.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

9. Ordering Information

Part No.	Package
IT8208M	16 SOP