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|--------------|-------------|---|
| SANYO | No. ※ 5086A | LC371000SP, SM-10/LC371000SP, SM-20LV |
| | | 1 MEG (131072 words × 8 bits) Mask ROM Internal Clocked Silicon Gate |

Preliminary

Overview

The LC371000SP, SM-10 and LC371000SP, SM-20LV are 1048576-bit Mask Programmable Read Only Memories organized as 131072 words by 8 bits.

The LC371000SP, SM-10 has a fast access time of 100 ns (t_{AA}) and 40 ns (t_{OA}) and a low standby power dissipation of 30 μ A under 5 V supply voltage. So, it is suitable for the fast 5 V operating systems.

The LC371000SP, SM-20LV has an access time of 200 ns (t_{AA}) and 80 ns (t_{OA}) and low standby power dissipation of 5 μ A under 3 V supply voltage. So, it is suitable for the low power systems such as battery used ones. Moreover, the LC371000SP, SM-20LV offers a fast access time of 150 ns (t_{AA}) and 60 ns (t_{OA}) under 3.3 V (3.0 to 3.6 V) supply voltage.

Pin configurations are 28-pin type. Pin 20 is mask programmable to CE or OE and it is possible to select either active HIGH or LOW.

Features

- 131072 words × 8 bits organization
- Power supply

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|----------------------|-----------------|
| LC371000SP, SM-10: | 5.0 V \pm 10% |
| LC371000SP, SM-20LV: | 2.7 to 3.6 V |
- Fast access time (t_{AA} , t_{CA})

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|----------------------|----------------------------|
| LC371000SP, SM-10: | 100 ns (max.) |
| LC371000SP, SM-20LV: | 200 ns (max.) |
| | 150 ns |
| | (V_{CC} = 3.0 to 3.6 V) |
- Operating current

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|----------------------|--------------|
| LC371000SP, SM-10: | 70 mA (max.) |
| LC371000SP, SM-20LV: | 20 mA (max.) |
- Standby current (selected CE/ \overline{CE})

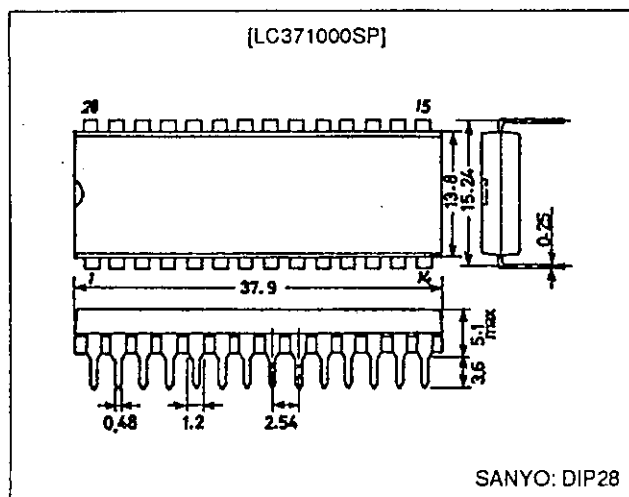
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|----------------------|-------------------|
| LC371000SP, SM-10: | 30 μ A (max.) |
| LC371000SP, SM-20LV: | 5 μ A (max.) |
- Full static operation (internal clocked type)
- Fully TTL compatible (5 V supply)
- 3 state outputs
- 28-pin type pin configuration
- Package type

| | |
|---------------------|------------------|
| LC371000SP-10/20LV: | DIP28 (600 mil) |
| LC371000SM-10/20LV: | SOP28D (450 mil) |

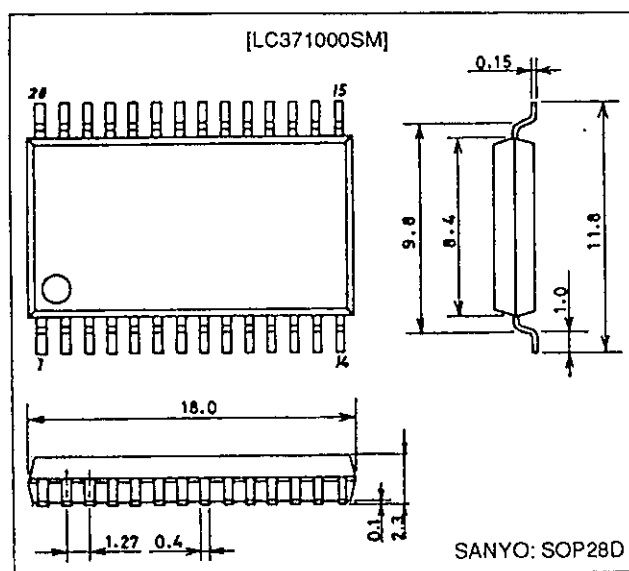
Package Dimensions

unit: mm

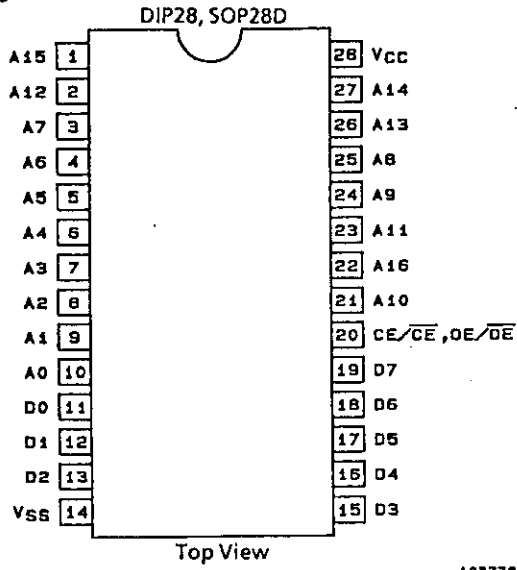
3012A-DIP28



3187-SOP28D



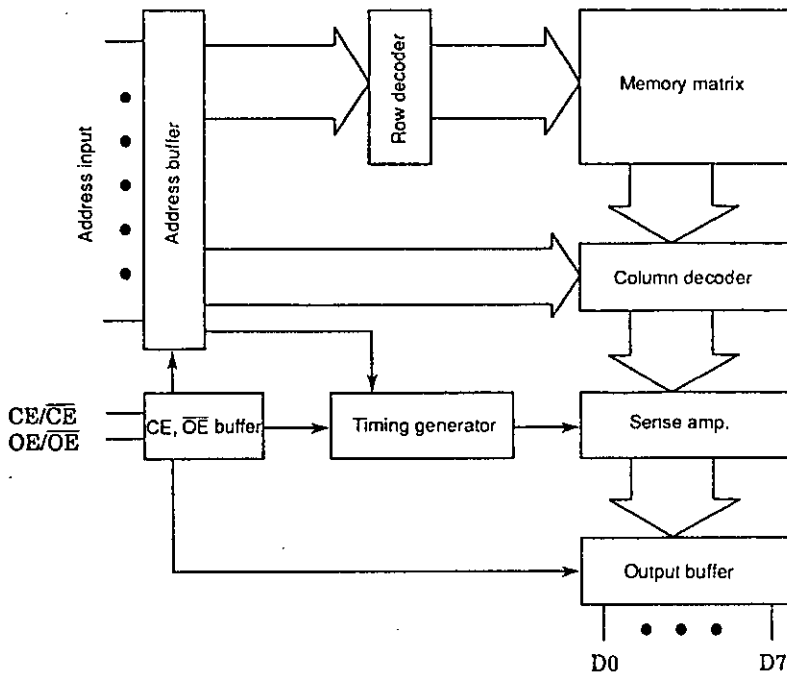
Pin Assignment



Pin Functions

| | |
|-----------------|---------------------|
| A0 to A16 | Address input |
| D0 to D7 | Data output |
| CE/CĒ | Chip enable input |
| OE/OĒ | Output enable input |
| V _{CC} | Power supply |
| V _{SS} | Ground |

Block Diagram



Truth Table

| CE/CĒ | OE/OĒ | Output | V _{CC} current |
|--------|--------|--------|-------------------------|
| L/H | -/- | High-Z | Standby mode |
| -/- | L/H | High-Z | Operating mode |
| H/L | -/- | DOUT | Operating mode |
| -/- | H/L | DOUT | Operating mode |

Note: It is mask programmable to select CE/CĒ/OE/OĒ's active level.

Specifications

Absolute Maximum Ratings*1

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|---------------|---|--------------------------|------------------|
| Maximum power supply voltage | $V_{CC\ max}$ | | -0.3 to +7.0 | V |
| Supply input voltage | V_{IN} | | -0.3*2 to $V_{CC} + 0.3$ | V |
| Supply output voltage | V_{OUT} | | -0.3 to $V_{CC} + 0.3$ | V |
| Allowable power dissipation | $Pd\ max$ | $T_a = 25^\circ\text{C}$; Reference values for the SANYO DIP package | 1.0 | W |
| Operating temperature | T_{opr} | | 0 to +70 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.

2. V_{IN} (min) = -3.0 V (pulse width ≤ 30 ns)

Input/Output Capacitance* at $T_a = 25^\circ\text{C}$, $f = 1.0$ MHz

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------|-----------|---|-----|-----|-----|------|
| Input capacitance | C_{IN} | $V_{IN} = 0$ V; Reference values for the SANYO DIP package | | | 8 | pF |
| Output capacitance | C_{OUT} | $V_{OUT} = 0$ V; Reference values for the SANYO DIP package | | | 10 | pF |

Note: * This parameter is periodically sampled and not 100% tested.

3 V Operation

DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ\text{C}$

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------------|---------------|------------|--------------|-----|----------------|------|
| Supply voltage | $V_{CC\ max}$ | | 2.7 | 3.0 | 3.6 | V |
| Input high level voltage | V_{IH} | | $0.8 V_{CC}$ | | $V_{CC} + 0.3$ | V |
| Input low level voltage | V_{IL} | | -0.3 | | +0.4 | V |

DC Electrical Characteristics at $T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|------------|--|----------------|-----|-----------|---------------|
| Operating supply current | I_{CCA1} | $\overline{CE} = 0.2$ V ($CE = V_{CC} - 0.2$ V), $V_I = V_{CC} - 0.2$ V/0.2 V | | | 15 | mA |
| | I_{CCA2} | $\overline{CE} = V_{IL}$ ($CE = V_{IH}$), $I_O = 0$ mA, $V_I = V_{IH}/V_{IL}$, $f = 5$ MHz | | | 20 | mA |
| Standby supply current*2 | I_{CCS1} | $\overline{CE} = V_{CC} - 0.2$ V ($CE = 0.2$ V) | | | 5 (0.5*1) | μA |
| | I_{CCS2} | $\overline{CE} = V_{IH}$ ($CE = V_{IL}$) | | | 50 (10*1) | μA |
| Input leakage current | I_{LI} | $V_{IN} = 0$ to V_{CC} | -1.0 | | +1.0 | μA |
| Output leakage current | I_{LO} | \overline{CE} or $\overline{OE} = V_{IH}$ (CE or $OE = V_{IL}$), $V_{OUT} = 0$ to V_{CC} | -1.0 | | +1.0 | μA |
| Output high level voltage | V_{OH} | $I_{OH} = -0.5$ mA | $V_{CC} - 0.2$ | | | V |
| Output low level voltage | V_{OL} | $I_{OL} = 0.5$ mA | | | 0.2 | V |

Note: 1. Guaranteed at $T_a = 25^\circ\text{C}$

2. When OE/OE is programmed, this system cannot be in standby mode.

AC Characteristics at $T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|-----------|------------|-------------|-----|-------------|------|
| Cycle time | t_{CYC} | | 200 (150*2) | | | ns |
| Address access time | t_{AA} | | | | 200 (150*2) | ns |
| Chip enable access time | t_{CA} | | | | 200 (150*2) | ns |
| Output enable access time | t_{OA} | | | | 80 (60*2) | ns |
| Output hold time | t_{OH} | | 25 | | | ns |
| Output disable time*1 | t_{OD} | | | | 50 | ns |

Note: 1. t_{OD} is measured from the earlier edge of the \overline{CE} (CE) or \overline{OE} (OE)'s going high (low). This parameter is periodically sampled and not 100% tested.

2. Guaranteed at $V_{CC} = 3.0$ to 3.6 V

5 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------------|---------------------|------------|------|-----|-----------------------|------|
| Supply voltage | V _{CC} max | | 4.5 | 5.0 | 5.5 | V |
| Input high level voltage | V _{IH} | | 2.2 | | V _{CC} + 0.3 | V |
| Input low level voltage | V _{IL} | | -0.3 | | +0.8 | V |

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|-------------------|---|------|-----|-------------|---------|
| Operating supply current | I _{CCA1} | $\overline{CE} = 0.2\text{ V}$ (CE = V _{CC} - 0.2 V), V _I = V _{CC} - 0.2 V/0.2 V | | | 30 | mA |
| | I _{CCA2} | $\overline{CE} = V_{IL}$ (CE = V _{IH}), I _O = 0 mA, V _I = V _{IH} /V _{IL} , f = 10 MHz | | | 70 | mA |
| Standby supply current*2 | I _{CCS1} | $\overline{CE} = V_{CC} - 0.2\text{ V}$ (CE = 0.2 V) | | | 30 (1.0*1) | µA |
| | I _{CCS2} | $\overline{CE} = V_{IH}$ (CE = V _{IL}) | | | 1.0 (300*1) | mA (µA) |
| Input leakage current | I _{LI} | V _{IN} = 0 to V _{CC} | -1.0 | | +1.0 | µA |
| Output leakage current | I _{LO} | \overline{CE} or $\overline{OE} = V_{IH}$ (CE or OE = V _{IL}), V _{OUT} = 0 to V _{CC} | -1.0 | | +1.0 | µA |
| Output high level voltage | V _{OH} | I _{OH} = -1.0 mA | 2.4 | | | V |
| Output low level voltage | V _{OL} | I _{OL} = 2.0 mA | | | 0.4 | V |

Note: 1. Guaranteed at Ta = 25°C
 2. When \overline{OE}/OE is programmed, this system cannot be in standby mode.

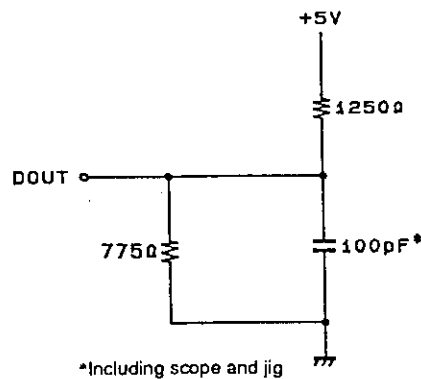
AC Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|------------------|------------|-----|-----|-----|------|
| Cycle time | t _{CYC} | | 100 | | | ns |
| Address access time | t _{AA} | | | | 100 | ns |
| Chip enable access time | t _{CA} | | | | 100 | ns |
| Output enable access time | t _{OA} | | | | 40 | ns |
| Output hold time | t _{OH} | | 20 | | | ns |
| Output disable time* | t _{OD} | | | | 30 | ns |

Note: * t_{OD} is measured from the earlier edge of the \overline{CE} (CE) or \overline{OE} (OE)'s going high (low).
 This parameter is periodically sampled and not 100% tested.

AC Test Conditions

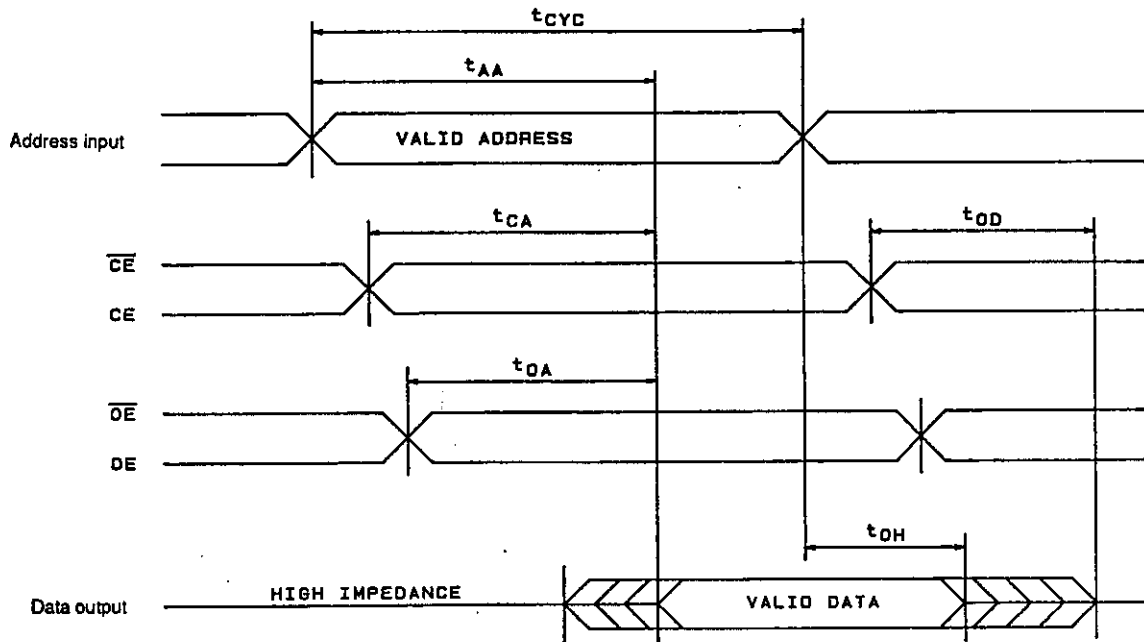
| | |
|----------------------|---|
| Input pulse levels | 0.4 V to 0.8 V _{CC} (3 V measurement), 0.6 V to 2.4 V (5 V measurement) |
| Input rise/fall time | 5 ns |
| Input timing level | 1.5 V |
| Output timing level | 1.5 V |
| Output load | 70 pF (3 V measurement) See Figure (5 V measurement) |



A03779

Output Load (5 V measurement)

Timing Chart



A03780

Usage Notes

For the reasons of using ATD (Address Transition Detector) circuit, the output data of this LSI directly after supplying voltage are invalid.

The valid data would be offered after the transition of at least one of CE or address signals under the stable supply voltage.

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