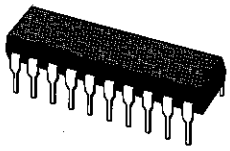
SGS-THOMSON MICROELECTRONICS

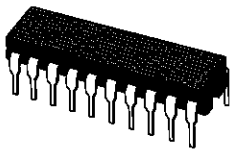
M54/74HC690/691
M54/74HC692/693

HC690/692 DECADE COUNTER/REGISTER (3-STATE)
HC691/693 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (for Q_A to Q_D)
  10 LSTTL LOADS (for RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) (for Q_A to Q_D)
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) (for RCO)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS690/691



B1R
(Plastic Package)



F1R
(Ceramic Package)

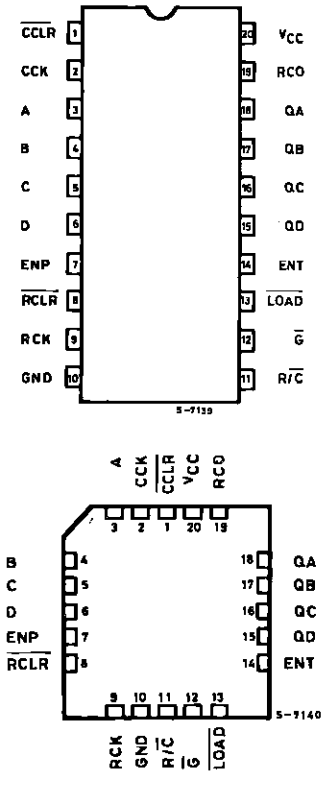
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R	M74HCXXXM1R
M74HCXXXB1R	M74HCXXXC1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The HC690/691/692/693 are high speed CMOS COUNTER/REGISTER fabricated in silicon gate C^2MOS technology.

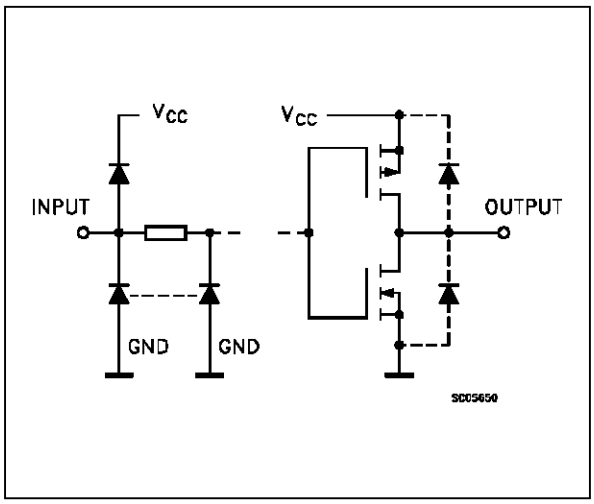
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output. These devices incorporate a synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.

If the LOAD input ($\overline{LOAD}$) is held "L" DATA input (A-D) are loaded in to the internal counter at positive edge of counter clock input ($\overline{CCK}$). In the counter mode, internal counter counts up at the positive of the counter clock. If the counter clear input ($\overline{CCLR}$) is held "L", the internal counter is cleared (synchronously to the counter clock for HC692/HC693, and asynchronously for HC690/HC691). The internal

counter's outputs are stored in the output register at the positive edge of the register clock (RCK). If the register clear input (RCLR) is held "L" the register is cleared (synchronously to register clock for HC692/HC693 and asynchronously for HC690/HC691). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

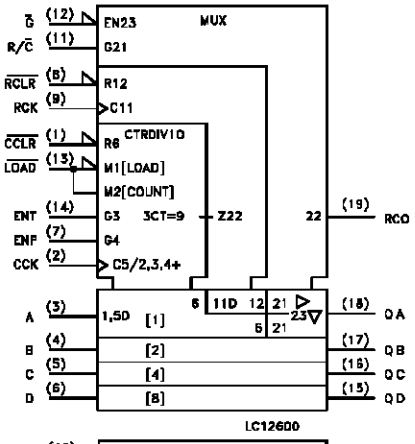


PIN DESCRIPTION

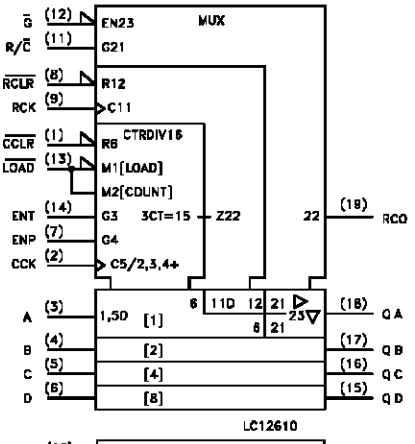
PIN No	SYMBOL	NAME AND FUNCTION
3 to 6	A to D	Data Inputs
7, 14	ENT, ENP	Enable Inputs
15 to 18	QA to QD	Data Outputs
1	$\overline{CCLR}$	Counter Clear (Active LOW)
2	CCK	Counter Clock
11	R/$\overline{C}$	Counter/ Register Select
8	$\overline{RCLR}$	Register Clear (Active LOW)
9	RCK	Register Clock
19	RCO	Ripple Counter Output
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

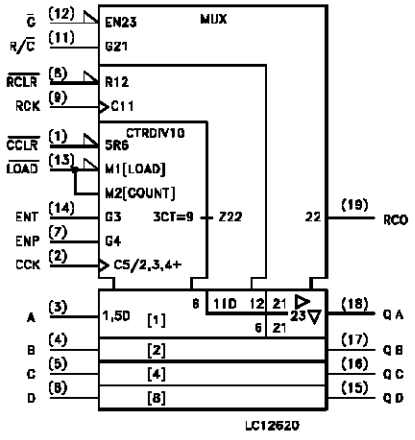
HC690



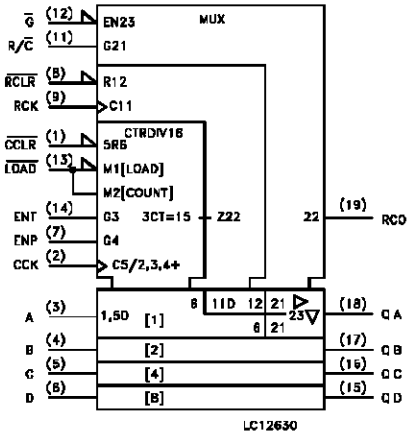
HC691



HC692



HC693

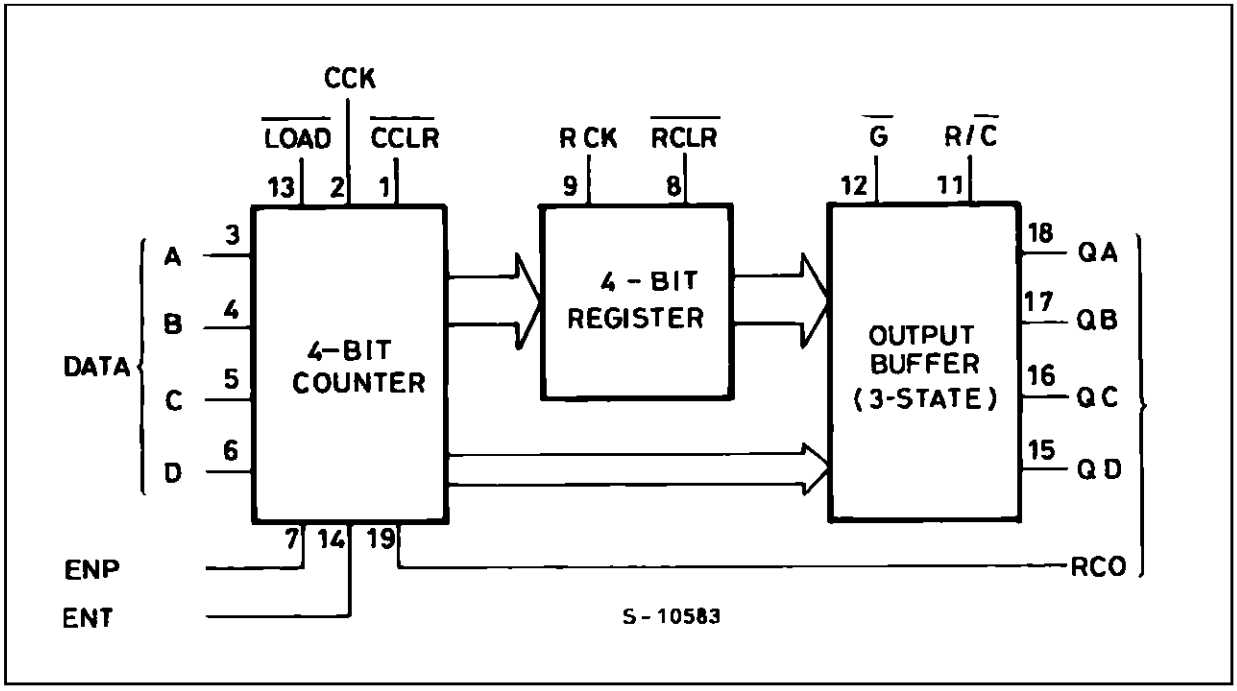


TRUTH TABLE

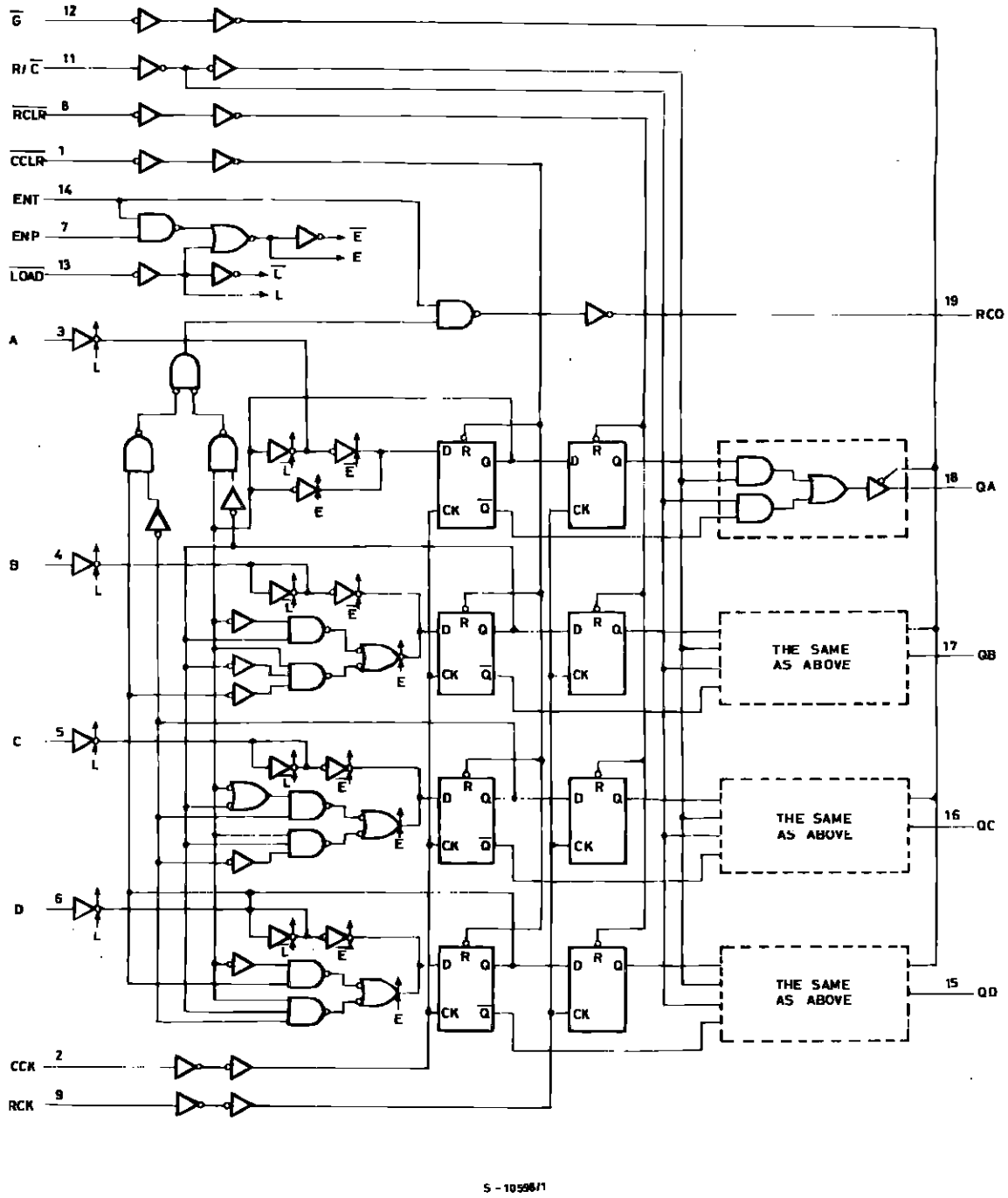
INPUTS									OUTPUS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	(*)	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	⎍	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	⎍	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	⎍	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	⎍	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	⎎	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	(*)	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	⎍	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H	⎎	H	L	NO CHANGE				NO LOAD

(*) : X for HC690/691 ⎍ for HC692/693
X : DON'T CARE
Z : HIGH IMPEDANCE
a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGHT D RESPECTIVELY.
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS a' through qd' respectively
HC690/692 RCO = QA • QD • ENT
HC691/693 RCO = QA • QB • QC • QD • ENT

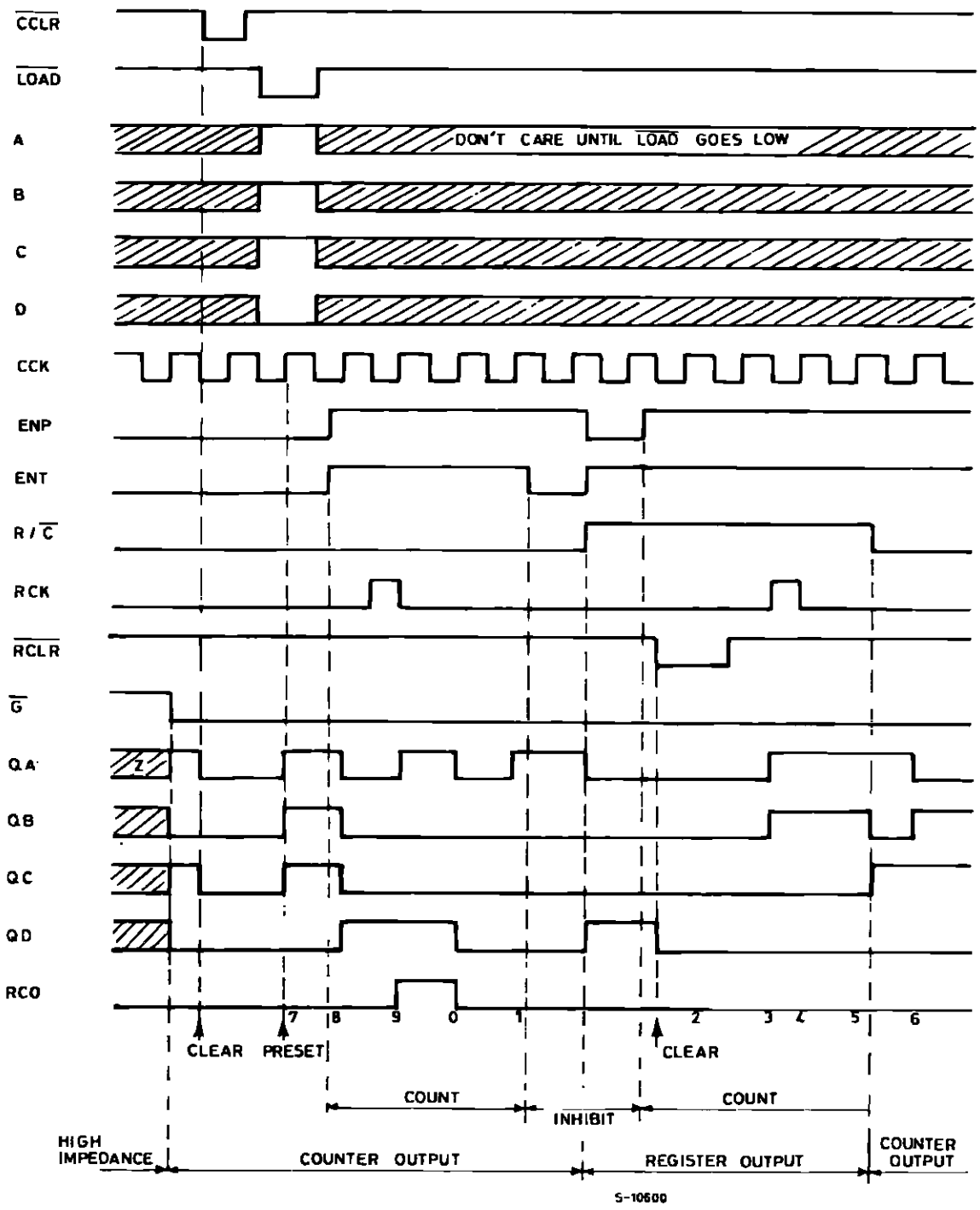
BLOCK DIAGRAM



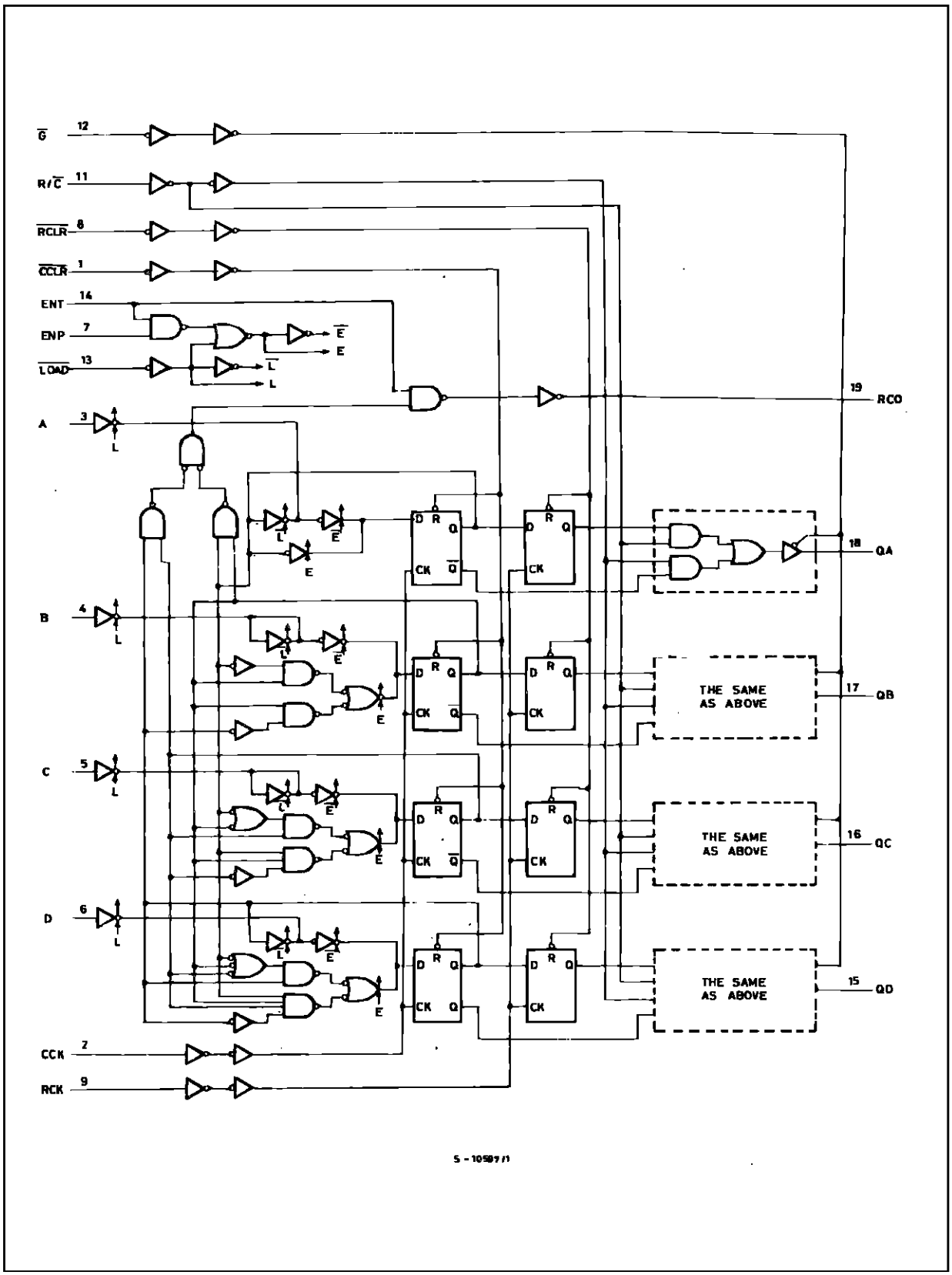
LOGIC DIAGRAM (HC690)



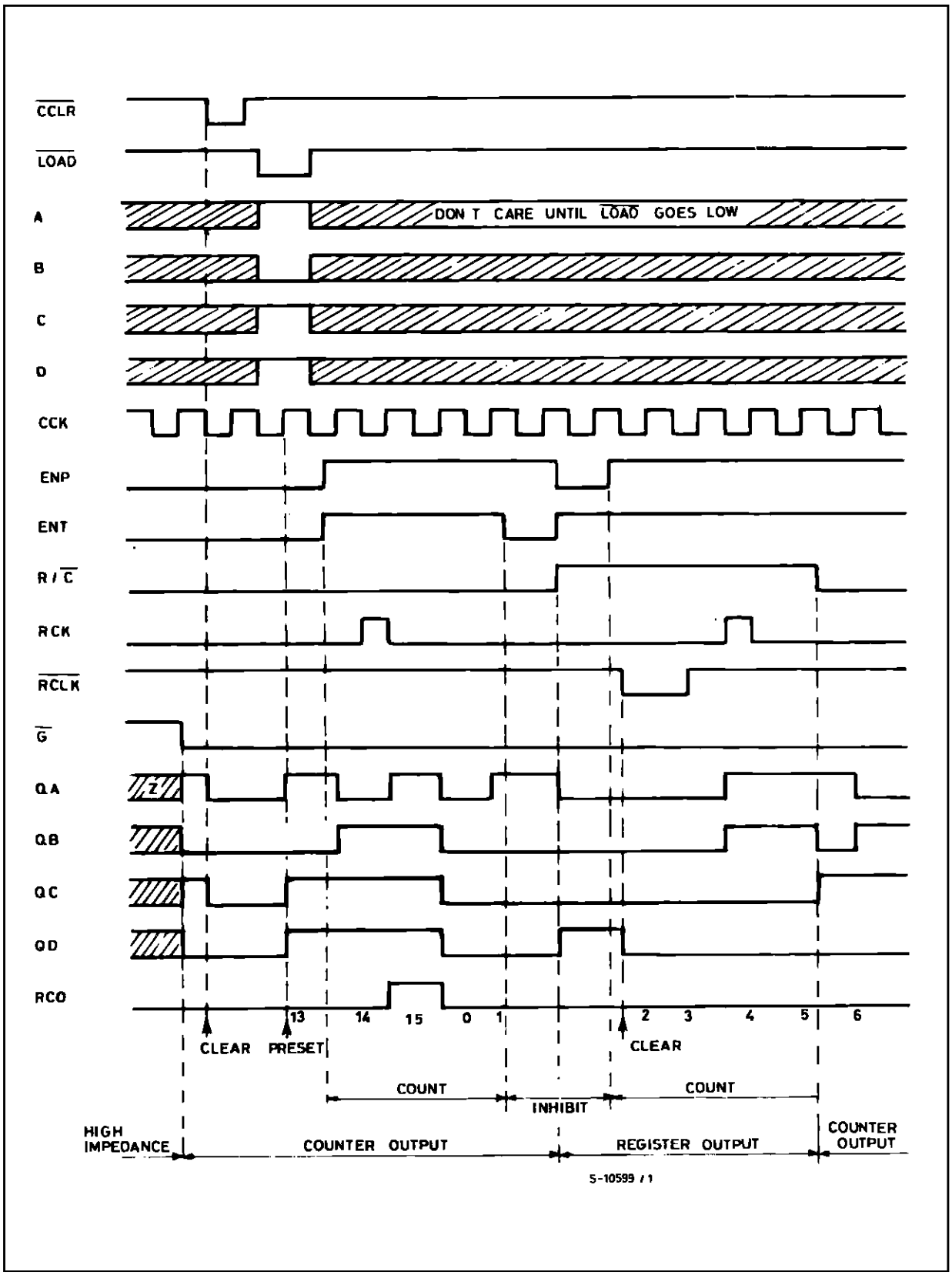
TIMING CHART (HC690)



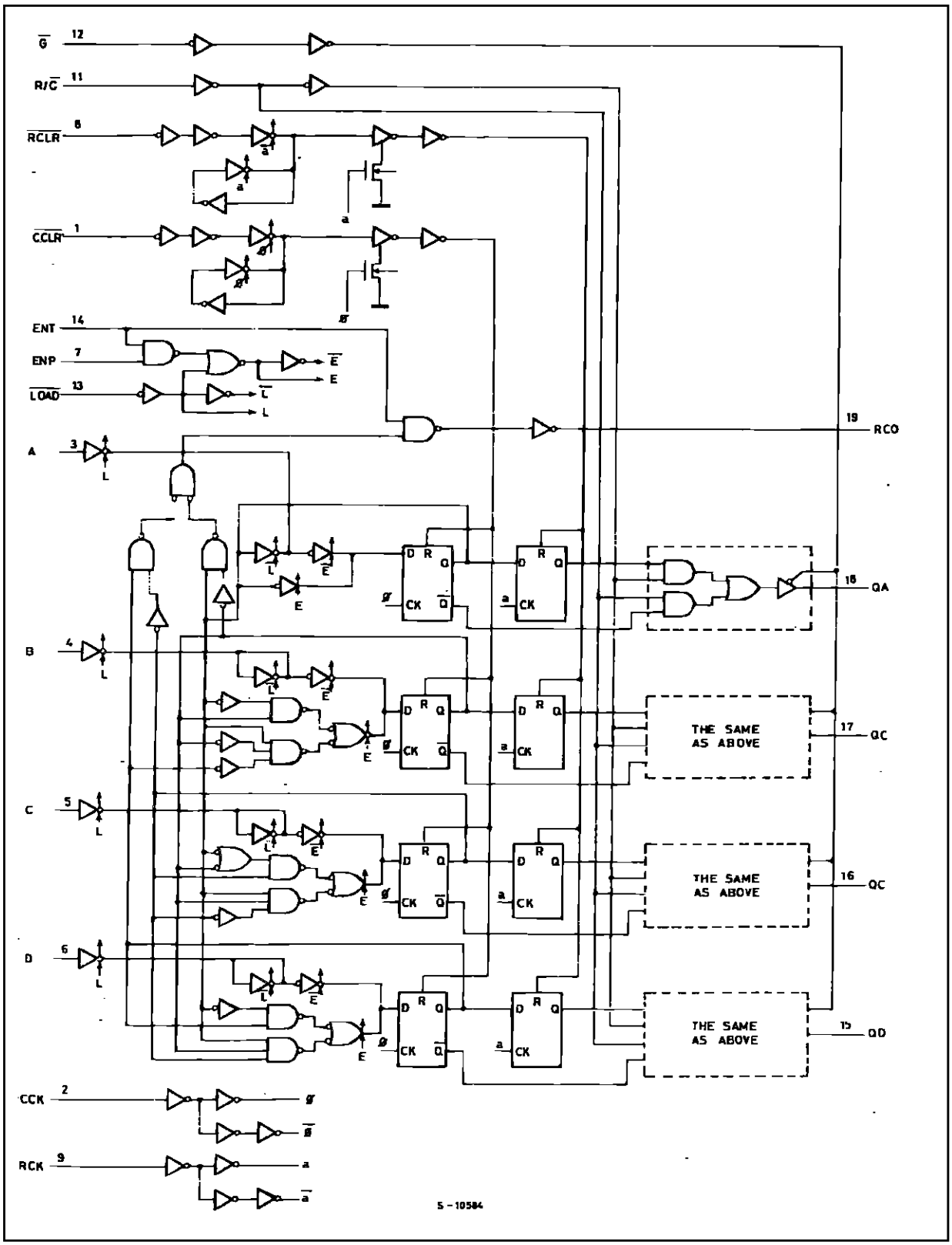
LOGIC DIAGRAM (HC691)



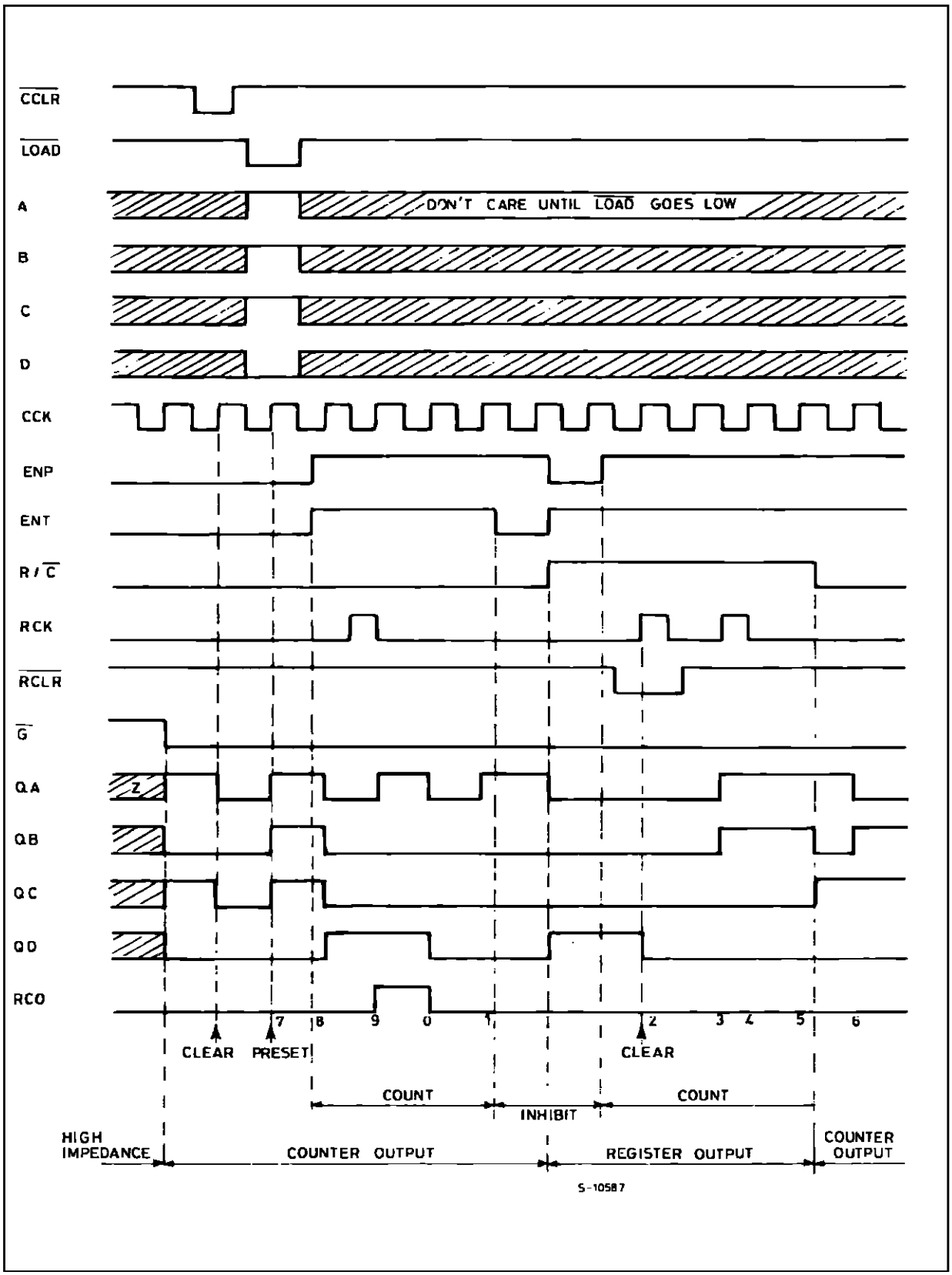
TIMING CHART (HC691)



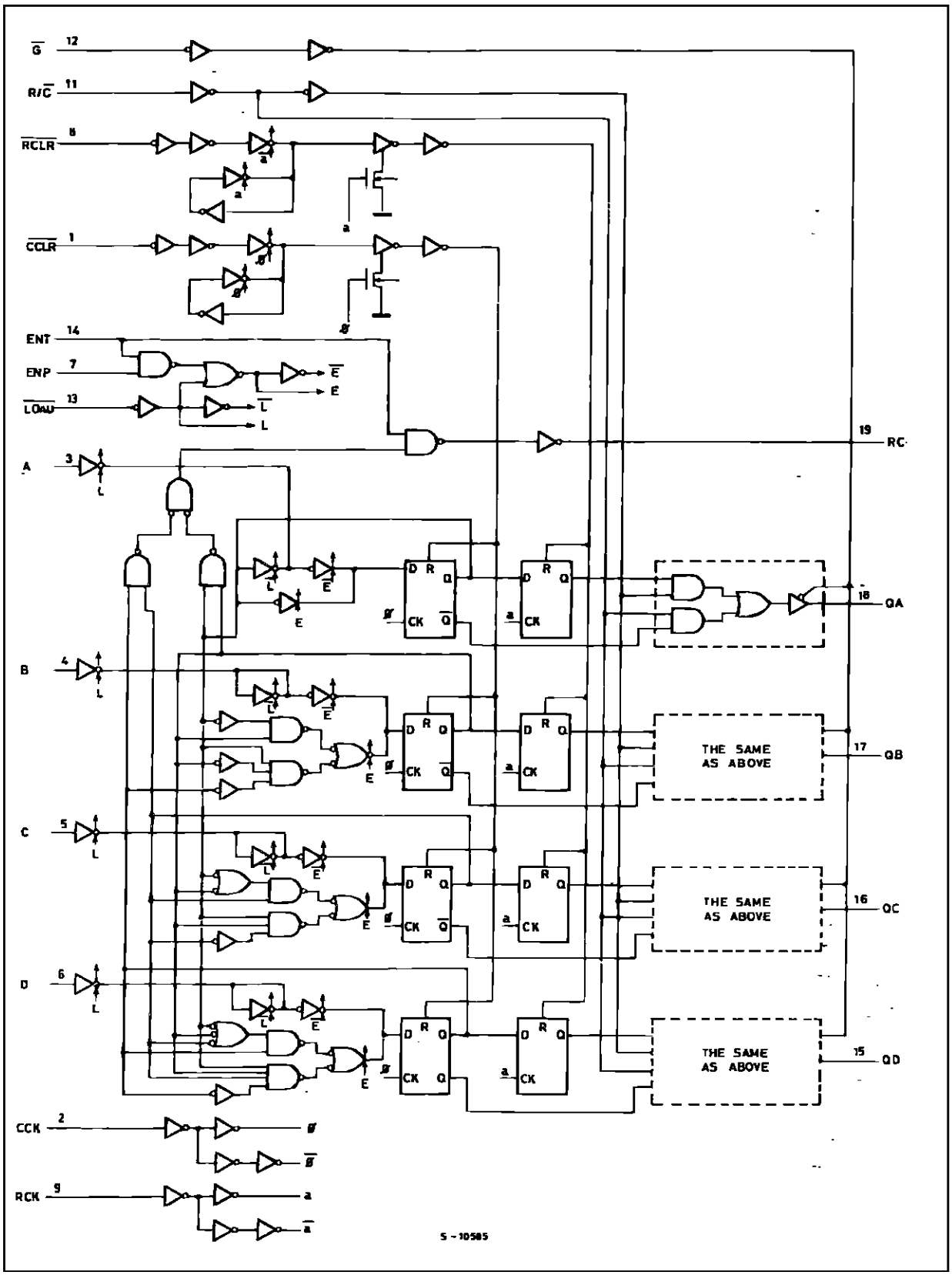
LOGIC DIAGRAM (HC692)



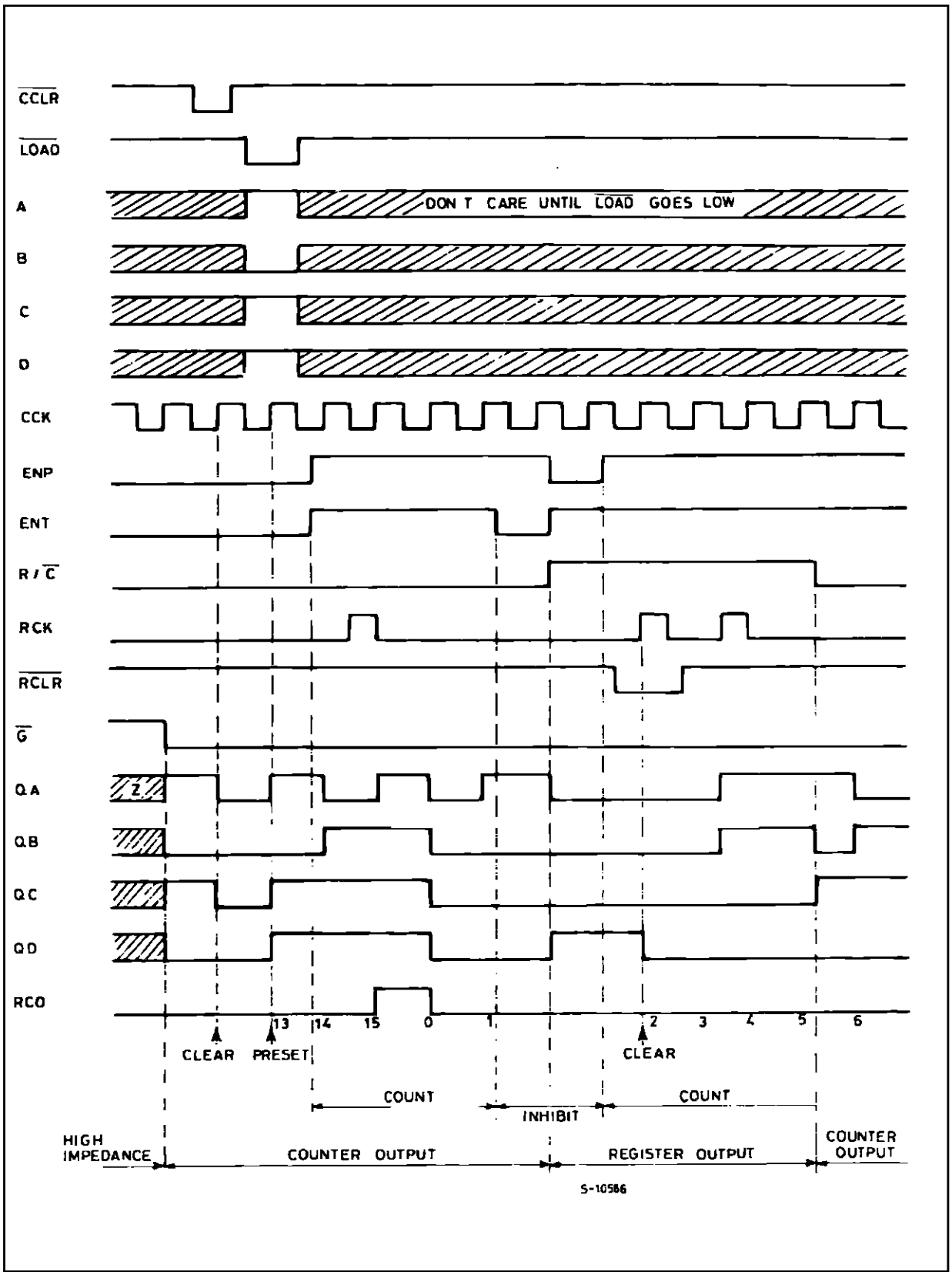
TIMING CHART (HC692)



LOGIC DIAGRAM (HC693)



TIMING CHART (HC693)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		-0.5 to +7	V
V_I	DC Input Voltage		-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	RCO	± 25	mA
		QA to QD	± 35	
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		± 70	mA
P_D	Power Dissipation		500 (*)	mW
T_{stg}	Storage Temperature		-65 to +150	°C
T_L	Lead Temperature (10 sec)		300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37		0.40	
V_{OL}	Low Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

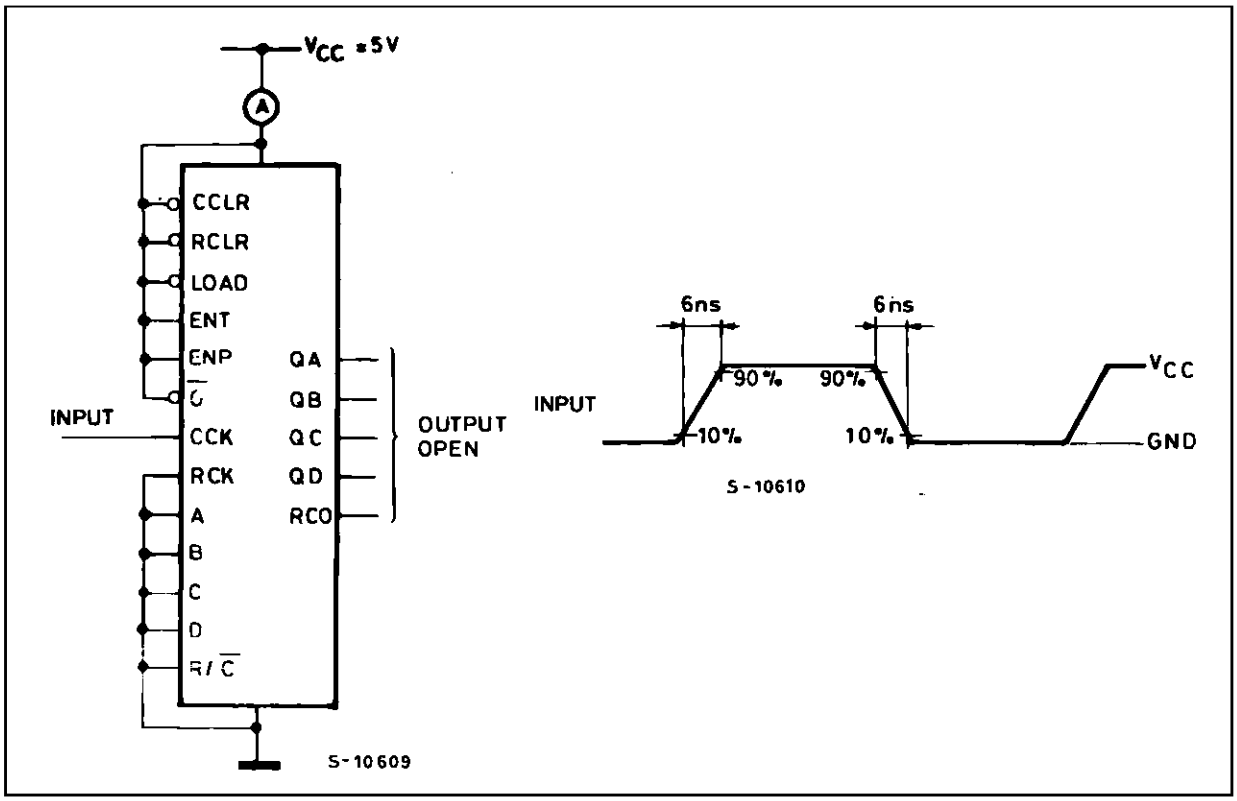
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		19	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - Q)	2.0	50			82	205		255		310	ns
		4.5				26	41		51		62	
		6.0				22	35		43		53	
		2.0	150			95	235		295		255	ns
		4.5				30	47		59		71	
		6.0				26	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			86	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			99	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - RCO)	2.0	50			65	165		205		250	ns
		4.5				21	33		41		50	
		6.0				18	28		35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (R/C - Q)	2.0	50			59	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
		2.0	150			72	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT - RCO)	2.0	50			36	100		125		150	ns
		4.5				12	20		25		30	
		6.0				10	17		21		26	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - Q) (for HC690/691)	2.0	50			91	225		280		340	ns
		4.5				29	45		56		68	
		6.0				25	38		48		58	
		2.0	150			104	255		320		385	ns
		4.5				33	51		64		77	
		6.0				28	43		54		65	
t_{PHL}	Propagation Delay Time ($\overline{RCLR}$ - Q) (for HC690/691)	2.0	50			86	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			100	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - RCO) (for HC690/691)	2.0	50			70	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0	50		4.4	12		3.6		3		MHz
		4.5			22	45		18		15		
		6.0			26	53		21		18		
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		48	120		150		180	ns
		4.5				15	24		30		36	
		6.0				13	20		26		31	
		2.0	150	R_L = 1 KΩ		61	150		190		225	ns
		4.5				19	30		38		45	
		6.0				17	26		32		38	
t_{PLH} t_{PHL}	Output Disable Time	2.0	50	R_L = 1 KΩ		32	145		180		220	ns
		4.5				15	29		36		44	
		6.0				13	25		31		37	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK - RCK)	2.0	50			28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CCLR}$ - $\overline{RCLR}$ (for HC690/691)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			68	150		190		220	ns
		4.5				17	30		38		44	
		6.0				14	26		32		37	
t_s	Minimum Set-up Time (A, B, C, D)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_s	Minimum Set-up Time $\overline{CCLR}$, $\overline{RCLR}$ (for HC692/693)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_s	Minimum Set-up Time (CCK, RCK)	2.0	50			48	125		155		180	ns
		4.5				12	25		31		36	
		6.0				10	21		26		31	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Removal Time (for HC690/691)	2.0	50				25		30		40	ns
		4.5					5		6		8	
		6.0					5		5		7	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC690/691 for HC692/693			70 80						pF

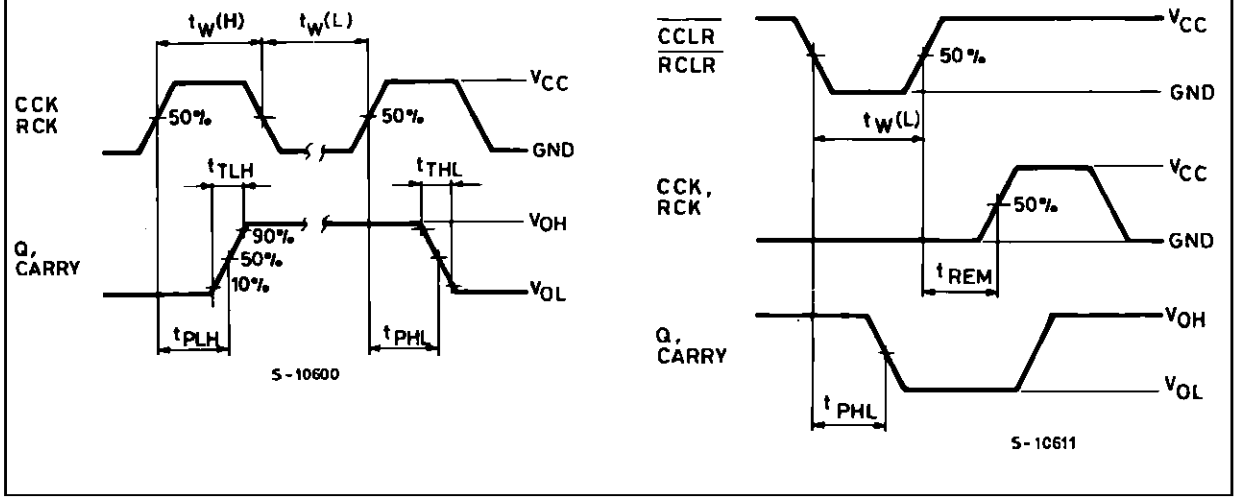
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



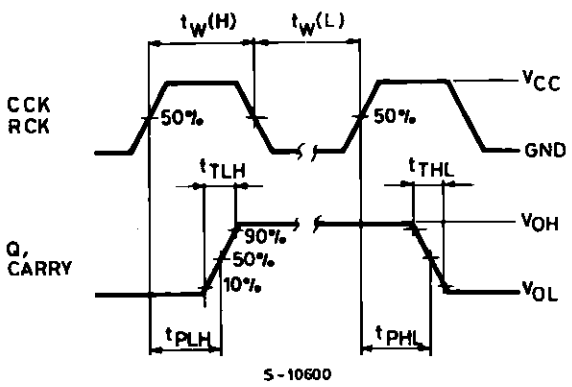
SWITCHING CHARACTERISTICS TEST WAVEFORM

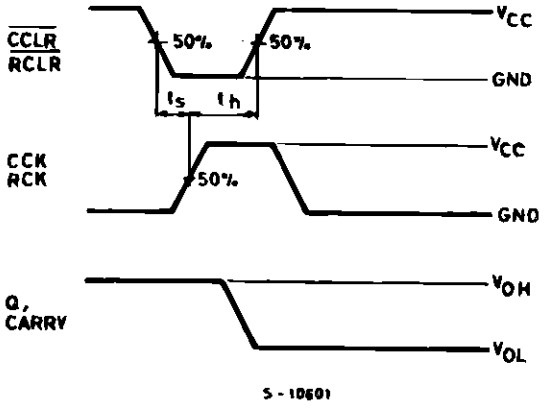
for HC690/691



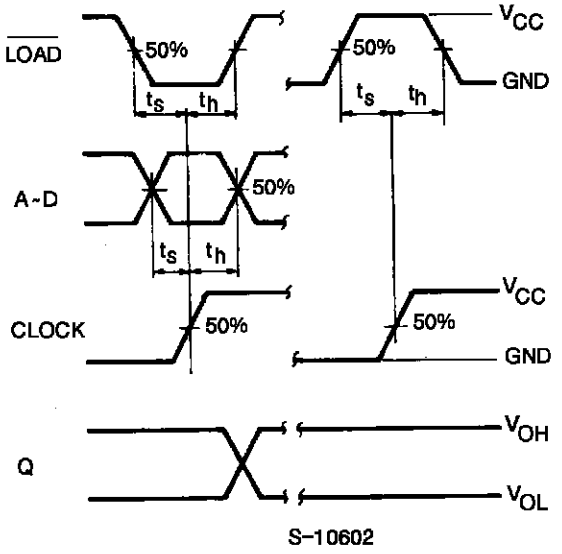
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

for HC692/693

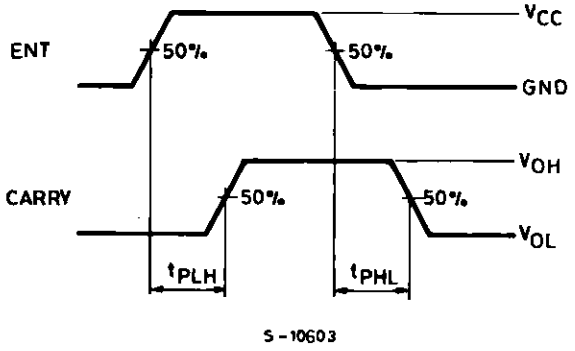


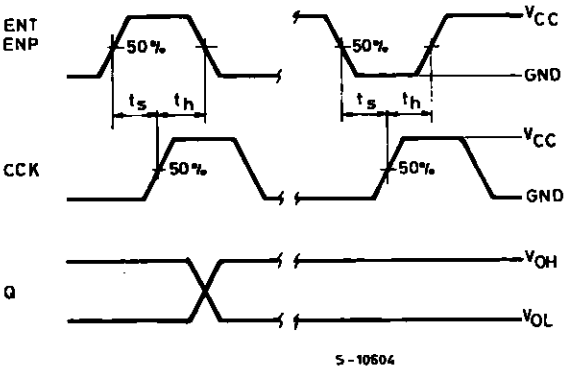


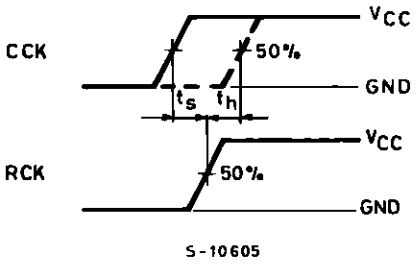
for ALL TYPES



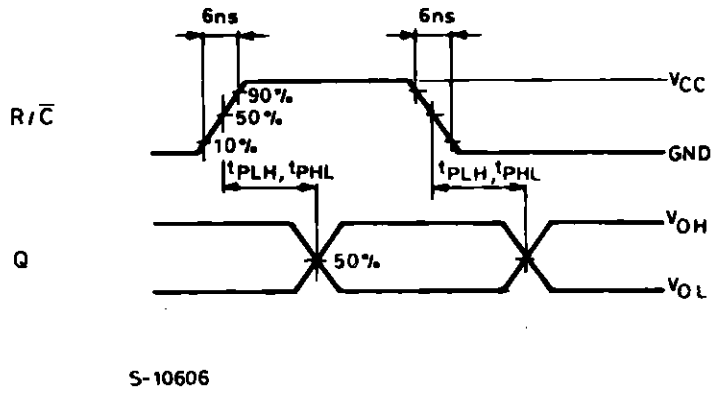
(Fix Maximum Count)







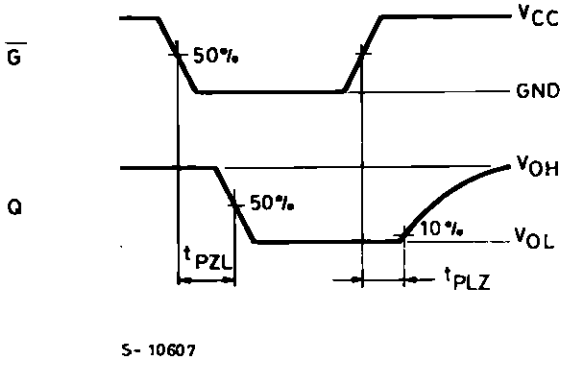
SWITCHING CHARACTERISTICS (continued)



S-10606

t_{PLZ}, t_{PZL}

The 1 kΩ load resistors should be connected between outputs and V_{CC} line and the 50 pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

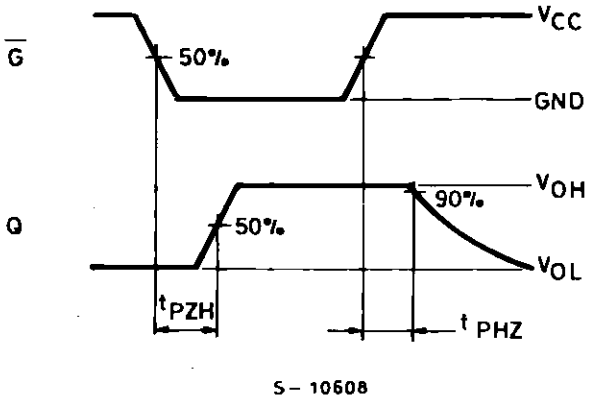


S- 10607

t_{PHZ}, t_{PZH}

The 1 kΩ load resistors and the 50 pF load capacitors should be connected between each output and GND line.

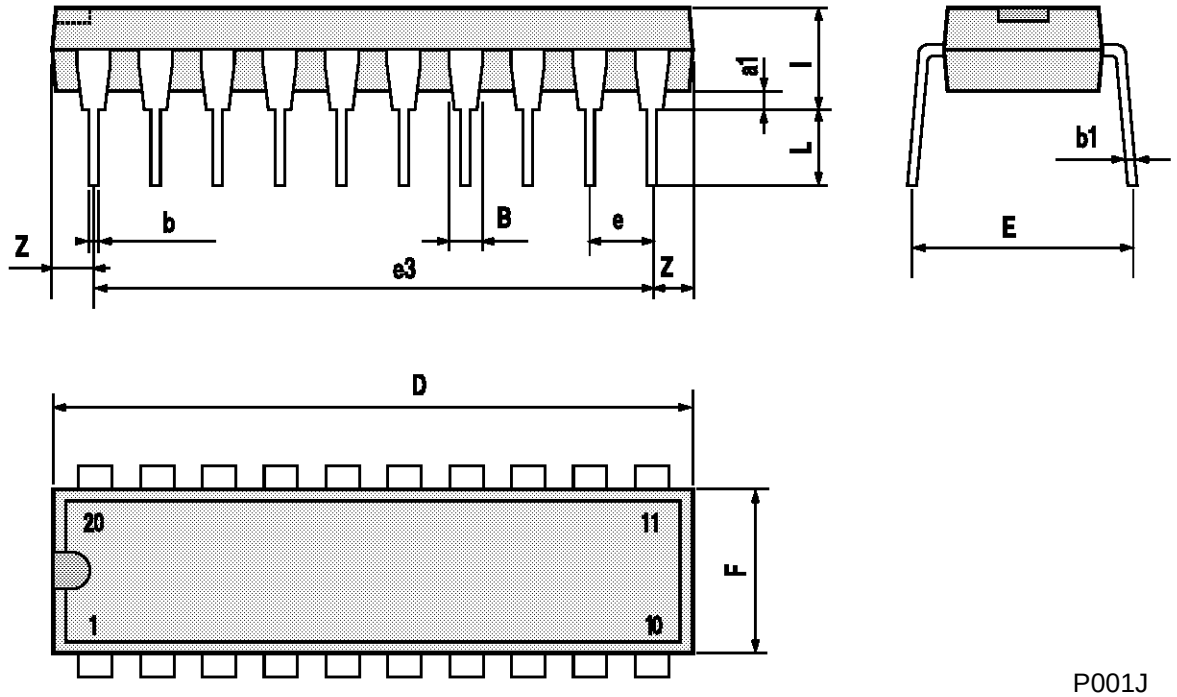
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.



S – 10608

Plastic DIP20 (0.25) MECHANICAL DATA

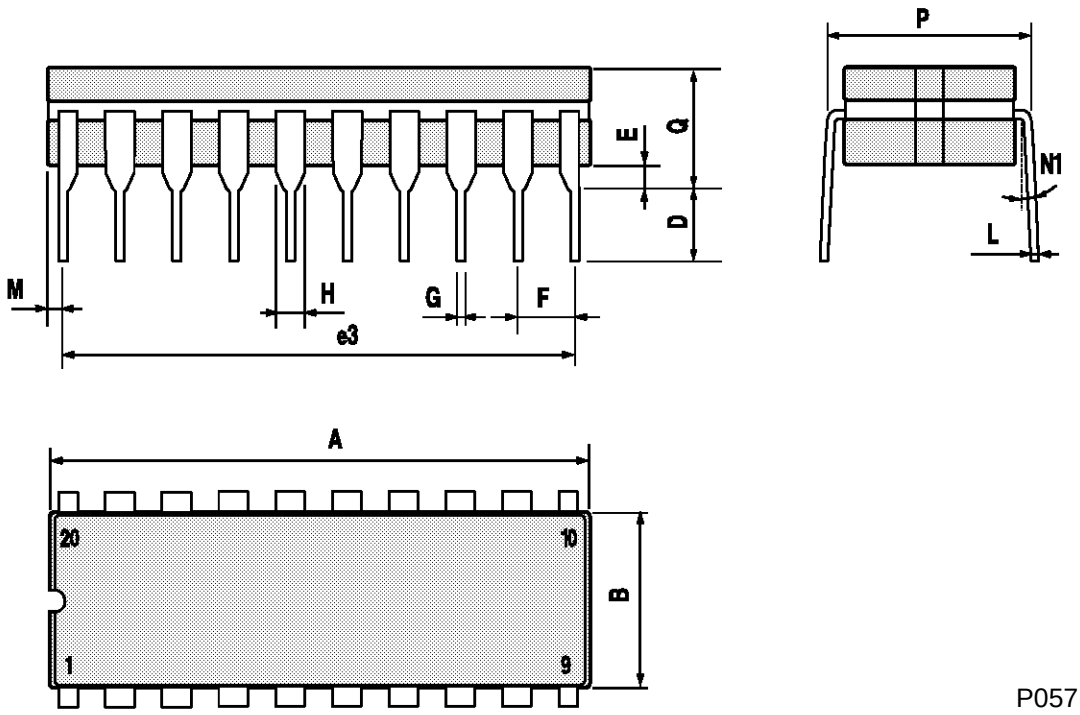
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

Ceramic DIP20 MECHANICAL DATA

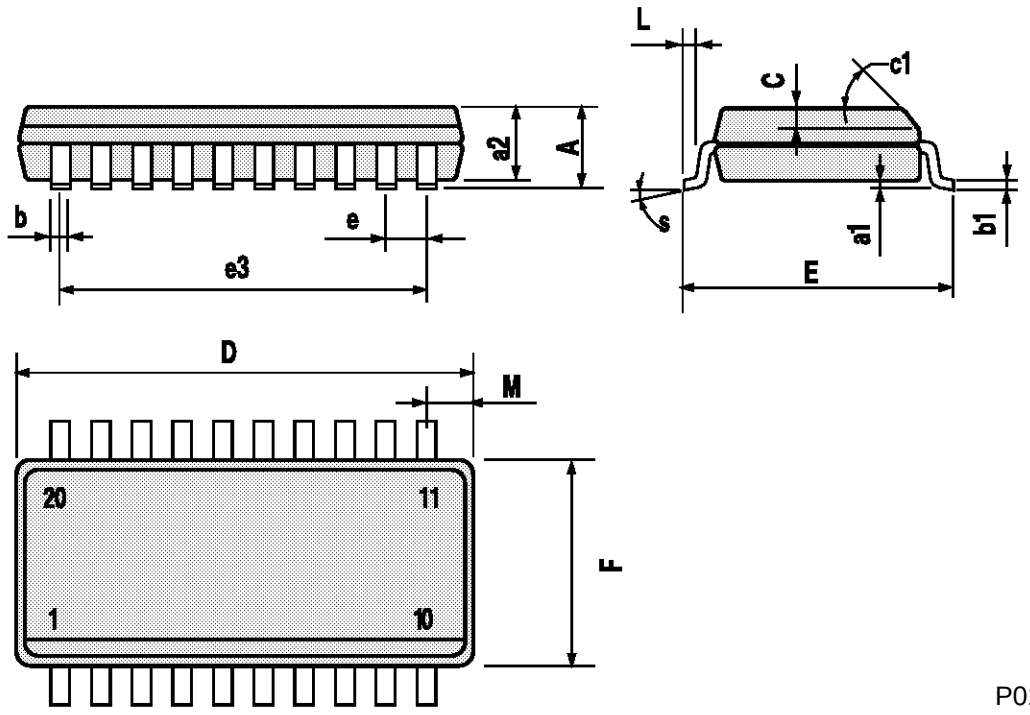
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



P057H

SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045