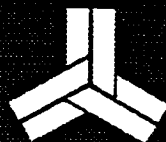


High-Performance 128 KByte Asynchronous Cache Module



AS7M32D128

PRELIMINARY 128 KByte Asynchronous Cache Module

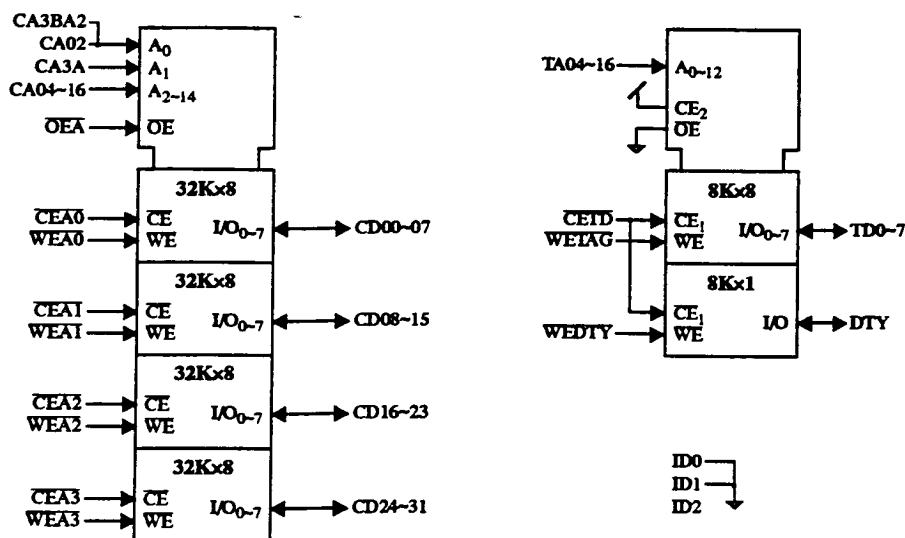
FEATURES

- 128 KByte secondary cache module
 - Data: 32,768 words × 32 bits
 - Tag: 8,192 words × 8 bits
 - Dirty: 8,192 words × 1 bit
- High speed
 - 15/20 ns cache address access time
 - 12/15 ns tag address access time
 - 50/33 MHz cycle frequency
- Low power
 - Active: 3.85W max (15 ns cycle)
 - Standby: 82.5 mW max
- 64 pin dual-readout SIMM
 - Same pinout for 128/256KB
 - No motherboard jumpers required
 - Small footprint: less than 1.2 in²
- Supports major PC cache controllers
 - Per-byte $\overline{CE}$ and $\overline{WE}$ controls
 - Per-bank $\overline{OE}$ control
 - Separate tag and dirty $\overline{WE}$
- TTL-compatible, three-state I/O
- High-quality 4-layer PCB

PIN ARRANGEMENT

ID0	1	65	ID1
ID2	2	66	GND
CD00	3	67	CD01
CD02	4	68	CD03
CD04	5	69	V _{cc}
CD06	6	70	CD05
CD08	7	71	CD07
GND	8	72	CD09
CD10	9	73	CD11
CD12	10	74	CD13
CD14	11	75	CD15
CD16	12	76	CD17
CD18	13	77	CD19
CD20	14	78	CD21
GND	15	79	GND
CD22	16	80	CD23
CD24	17	81	CD25
V _{cc}	18	82	V _{cc}
CD26	19	83	CD27
CD28	20	84	CD29
CD30	21	85	CD31
NC	22	86	NC
NC	23	87	NC
GND	24	88	GND
CEA0	25	89	NC
CEA1	26	90	NC
CEA2	27	91	V _{cc}
CEA3	28	92	NC
GND	29	93	NC
OEA	30	94	NC
WEA0	31	95	NC
WEA1	32	96	NC
WEA2	33	97	NC
WEA3	34	98	NC
WETAG	35	99	WEDTY
CE1D	36	100	V _{cc}
NC	37	101	NC
NC	38	102	NC
CA3A	39	103	CA3BA2
CA02	40	104	CA3B
GND	41	105	GND
CA04	42	106	CA05
CA06	43	107	CA07
CA08	44	108	CA09
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	NC
NC	49	113	NC
GND	50	114	GND
TA04	51	115	TA05
TA06	52	116	TA07
TA08	53	117	TA09
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	NC
NC	58	122	NC
GND	59	123	GND
TD0	60	124	TD1
TD2	61	125	TD3
TD4	62	126	TD5
TD6	63	127	TD7
DTY	64	128	V _{cc}

LOGIC BLOCK DIAGRAM



SELECTION GUIDE

	7M32D128-15	7M32D128-20
Maximum cache address access time	15 ns	20 ns
Maximum tag address access time	12 ns	15 ns
Maximum operating current	700 mA	650 mA
Maximum standby current	15 mA	15 mA

ALLIANCE SEMICONDUCTOR



FUNCTIONAL DESCRIPTION

The AS7M32D128 is a high performance secondary cache module for 486 and other advanced computer systems. The Alliance 32D family provides a plug-and-play upgradeable cache solution for motherboards based on all popular personal computer chipsets.

The 32D128 includes 128 KBytes of secondary cache, organized as one bank of 32K words by 32 bits. The module includes 8K words by 8 bits of tag storage and 8K "dirty" bits, for cacheable main memory up to 32 MBytes. Separate write-enable controls for tag and dirty RAMs offer maximum system flexibility.

The 32D128 is available in popular personal computer speed grades. The -15 version offers 15 ns address access time for cache data and 12 ns address access time for tag/dirty bits, to support 50 MHz system designs. The -20 version offers 20 ns address access time for cache data and 15 ns address

access time for tag/dirty bits, to support 33 MHz system designs.

Alliance's industry-leading low power CMOS fast static RAM gives the 32D128 excellent power characteristics. The module dissipates less than 82.5 mW in standby mode, and less than 3.85W in operation at 50 MHz. Inputs and outputs are fully TTL-compatible.

The 32D128 plugs into a 64 dual readout SIMM connector which occupies less than 1.2 square inches of board space. Identification pins ID0~ID2 distinguish different members of the 32D family and eliminate the need for motherboard cache configuration jumpers.

The module is fully static and requires no clocks for refresh or operation. It uses a single 5V power supply.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	—	6.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	°C
Temperature Under Bias	T_{bias}	-10	+85	°C
DC Output Current	I_{out}	—	20	mA

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby (I_{SB} , I_{SB1})
L	H	H	High-Z	Output Disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

**RECOMMENDED OPERATING CONDITIONS** $(T_a = 0 \text{ to } +70^\circ\text{C})$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5*	—	0.8	V

* $V_{IL, \text{min}} = -3.0\text{V}$ for pulse width less than 10 ns.**DC OPERATING CHARACTERISTICS** $(V_{CC} = 5\text{V} \pm 10\%, \text{GND} = 0\text{V}, T_a = 0 \text{ to } +70^\circ\text{C})$

Parameter	Symbol	Test Conditions	-15		-20		Unit
			Min	Max	Min	Max	
Input Leakage Current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{in} = \text{GND to } V_{CC}$	—	10	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{CE} = V_{IH}, V_{CC} = \text{Max}, V_{out} = \text{GND to } V_{CC}$	—	10	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CE} = V_{IL}, I_{out} = 0 \text{ mA}, f = f_{\text{max}}$	—	700	—	650	mA
Standby Power Supply Current	I_{SB}	$\overline{CE} = V_{IH}, f = f_{\text{max}}$	—	60	—	60	mA
	I_{SB1}	$\overline{CE} > V_{CC} - 0.2\text{V}, f = 0, V_{in} \leq 0.2\text{V or } V_{in} \geq V_{CC} - 0.2\text{V}$	—	15	—	15	mA
Output Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	—	0.4	—	0.4	V
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	—	2.4	—	V

CAPACITANCE $(f = 1 \text{ MHz}, T_a = \text{Room Temperature}, V_{CC} = 5\text{V})$

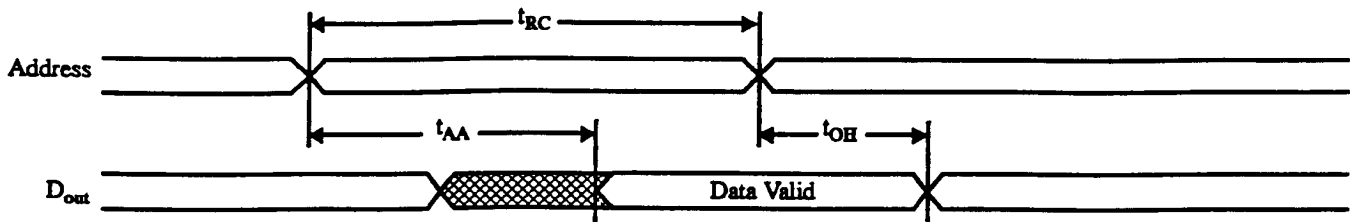
Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance: cache address	C_{IN4}	CA, $\overline{OEA}$	$V_{in} = 0\text{V}$	35	pF
Input capacitance: tag address	C_{IN2}	TA, $\overline{CETD}$	$V_{in} = 0\text{V}$	17.5	pF
Input capacitance: control	C_{IN1}	$\overline{WE}, \overline{CE}$ (except $\overline{CETD}$)	$V_{in} = 0\text{V}$	10	pF
Data I/O capacitance	C_{IO}	CD, TD, DTY	$V_{in} = V_{out} = 0\text{V}$	12	pF

**READ CYCLE**^{3, 11}(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

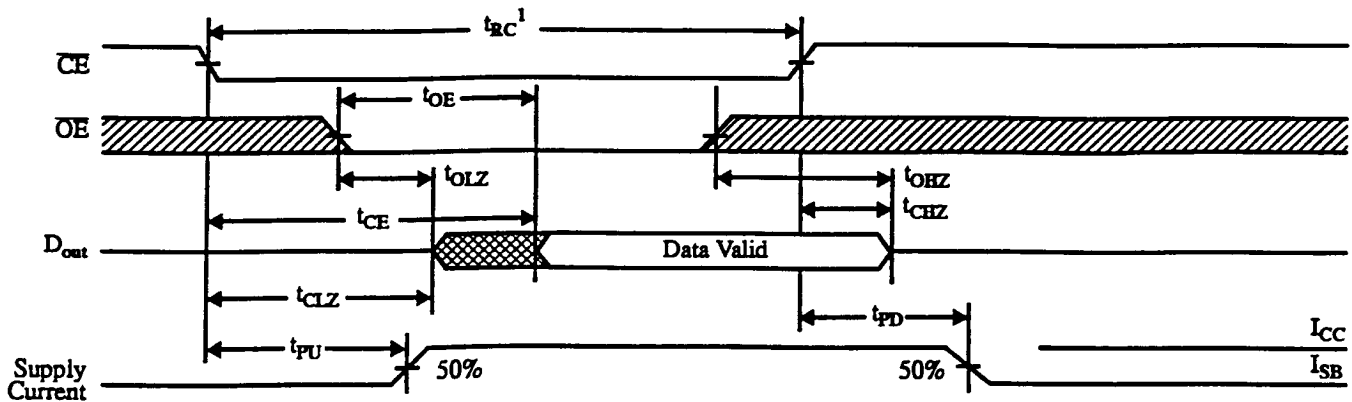
Parameter	Sym	-15				-20				Units	Notes
		Cache		Tag		Cache		Tag			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{RC}	15	—	12	—	20	—	15	—	ns	
Address Access Time	t _{AA}	—	15	—	12	—	20	—	15	ns	3
Chip Enable (CE) Access Time	t _{CE}	—	15	—	12	—	20	—	15	ns	
Output Enable (OE) Access Time	t _{OE}	—	4	—	—	—	5	—	—	ns	
Output Hold from Address Change	t _{OH}	3	—	3	—	3	—	3	—	ns	5
Chip Enable to Output in Low Z	t _{CLZ}	3	—	3	—	3	—	3	—	ns	4, 5
Chip Disable to Output in High Z	t _{CHZ}	—	4	—	4	—	5	—	4	ns	4, 5
Output Enable to Output in Low Z	t _{OLZ}	0	—	—	—	0	—	—	—	ns	4, 5
Output Disable to Output in High Z	t _{OHZ}	—	4	—	—	—	5	—	—	ns	4, 5
Chip Enable to Power Up Time	t _{PU}	0	—	0	—	0	—	0	—	ns	4, 5
Chip Disable to Power Down Time	t _{PD}	—	15	—	12	—	20	—	15	ns	4, 5

TIMING WAVEFORM OF READ CYCLE 1^{3, 6, 7, 11}

(Address controlled)

**TIMING WAVEFORM OF READ CYCLE 2**^{3, 6, 8, 11}

(CE controlled)

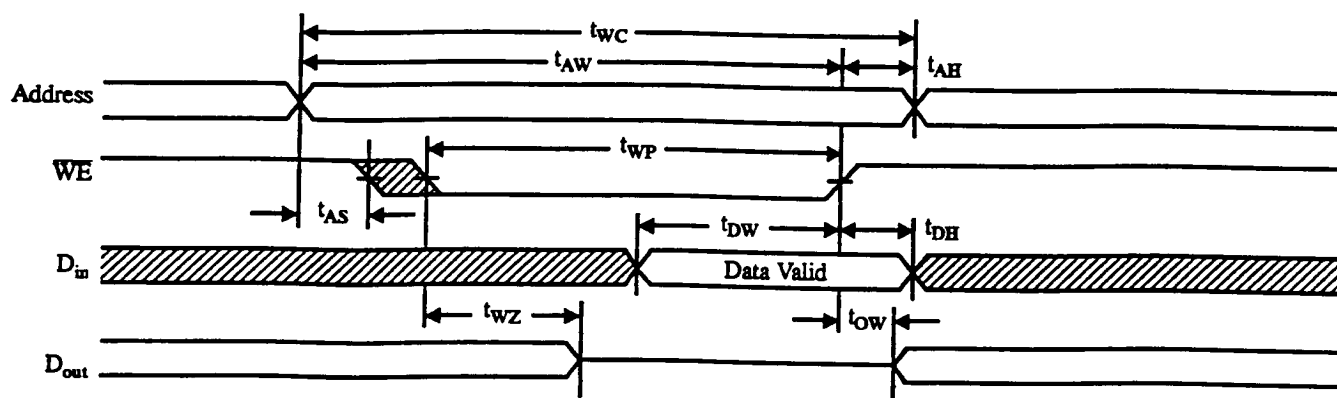


**WRITE CYCLE** ^{3, 10} $(V_{CC} = 5V \pm 10\%, GND = 0V, T_a = 0 \text{ to } +70^\circ C)$

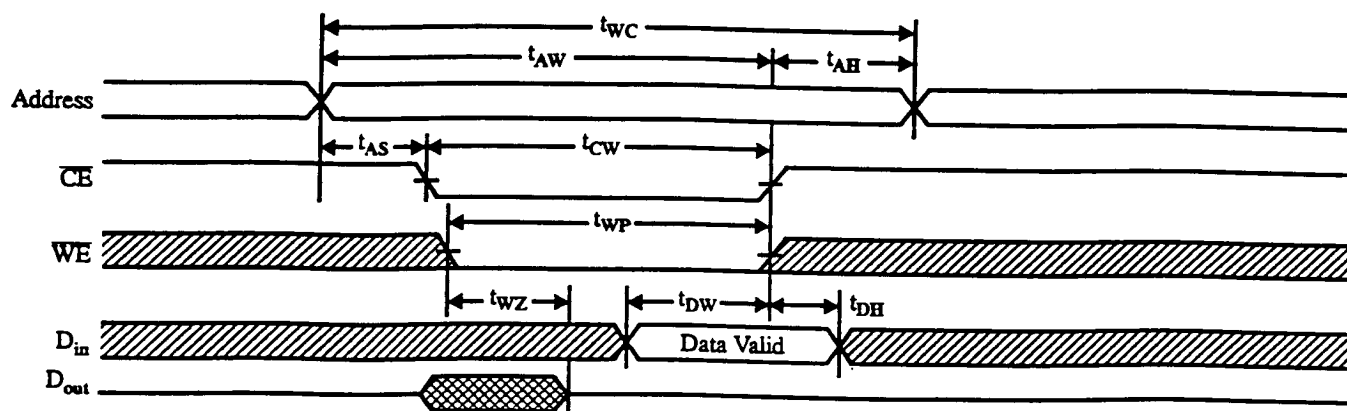
Parameter	Sym	-15				-20				Units	Notes
		Cache		Tag		Cache		Tag			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t _{WC}	15	—	12	—	20	—	15	—	ns	
Chip Enable to Write End	t _{CW}	10	—	9	—	12	—	10	—	ns	
Address Set-up to Write End	t _{AW}	10	—	9	—	12	—	10	—	ns	
Address Set-up Time	t _{AS}	0	—	0	—	0	—	0	—	ns	
Write Pulse Width	t _{WP}	9	—	8	—	12	—	9	—	ns	
Address Hold From End of Write	t _{AH}	0	—	0	—	0	—	0	—	ns	
Data Valid to Write End	t _{DW}	9	—	8	—	12	—	9	—	ns	
Data Hold Time	t _{DH}	0	—	0	—	0	—	0	—	ns	4, 5
Write Enable to Output in High Z	t _{WZ}	—	5	—	5	—	5	—	5	ns	4, 5
Output Active from Write End	t _{OW}	3	—	3	—	3	—	3	—	ns	4, 5

TIMING WAVEFORM OF WRITE CYCLE 1 ⁹

(WE controlled)

**TIMING WAVEFORM OF WRITE CYCLE 2** ⁹

(CE controlled)





AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

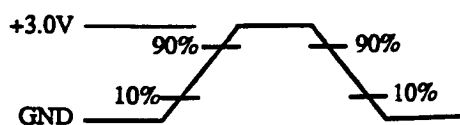


Figure A. Input Waveform

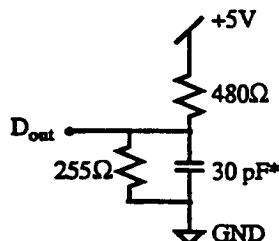
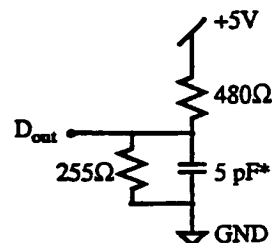
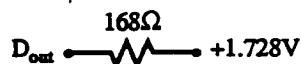


Figure B. Output Load

Thevenin equivalent:

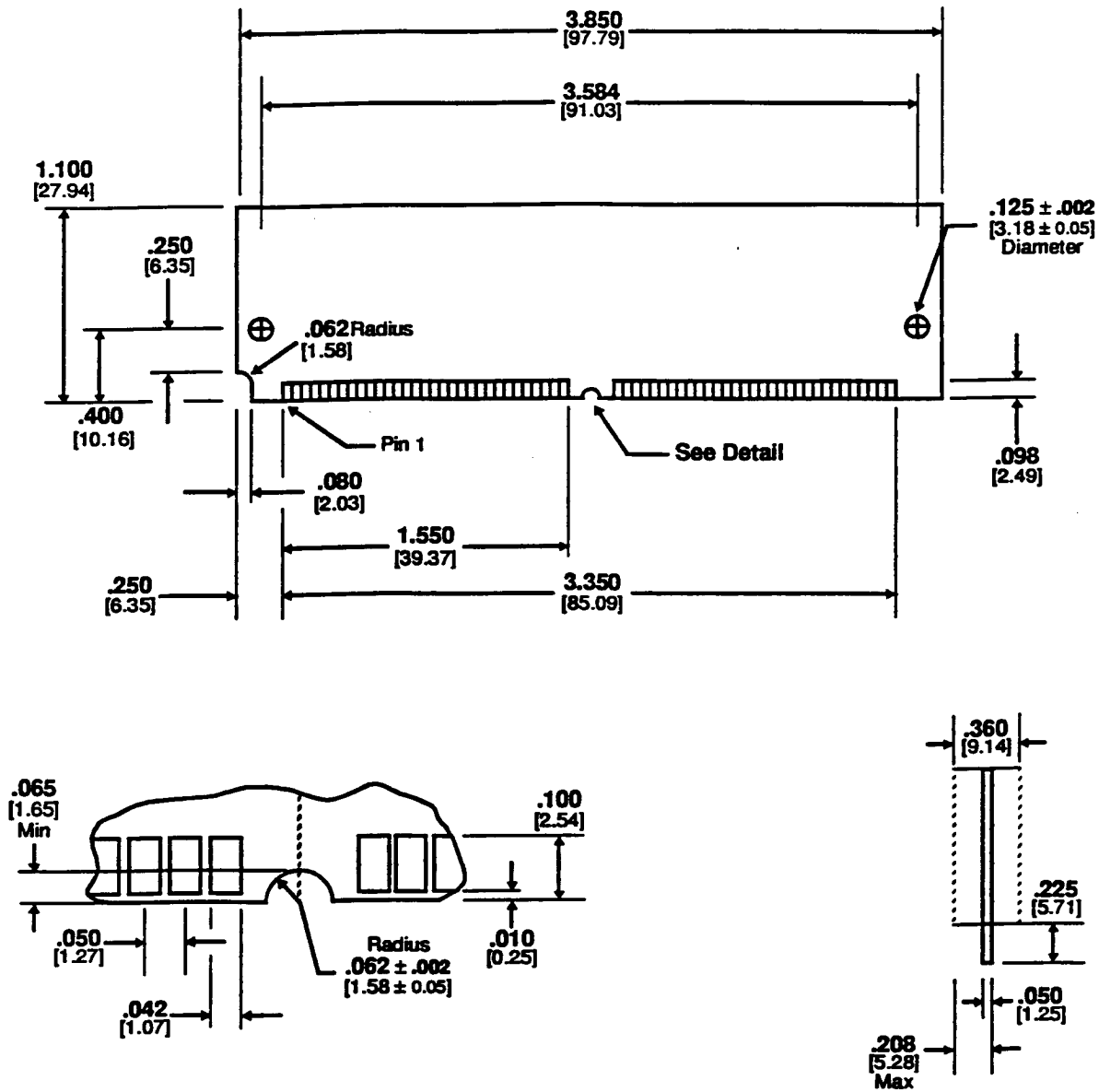
Figure C. Output Load for t_{CLZ} , t_{CHZ}

*including scope and jig capacitance

NOTES

1. During V_{cc} power-up, a pull-up resistor to V_{cc} on $\overline{CE}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see AC Test Loads and Waveforms, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with $CL = 5\text{ pF}$ as in Figure C. Transition is measured 500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is high for read cycle
7. $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
10. All write cycle timings are referenced from the last valid address to the first transitioning address.
11. All read cycle timings are referenced from the last valid address to the first transitioning address.

PHYSICAL DIMENSIONS



Dimensions in inches (millimeters).



ORDERING INFORMATION

Package	Cache Address Access Time	
	15 ns	20 ns
64 dual readout SIMM	AS7M32D128-15C	AS7M32D128-20C

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