

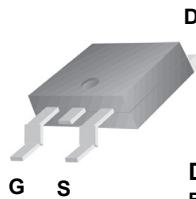
**FCD7N60 / FCU7N60**  
**600V N-Channel MOSFET**

**Features**

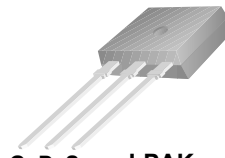
- 650V @ $T_J = 150^\circ\text{C}$
- Typ.  $R_{ds(on)} = 0.53\Omega$
- Ultra low gate charge (typ.  $Q_g = 23\text{nC}$ )
- Low effective output capacitance (typ.  $C_{oss,eff} = 60\text{pF}$ )
- 100% avalanche tested

**Description**

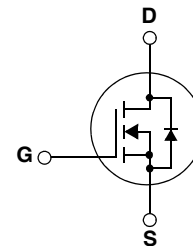
SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance. This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



**D-PAK**  
FCD Series



**I-PAK**  
FCU Series



**Absolute Maximum Ratings**

Symbol	Parameter	FCD7N60/FCU7N60	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	7 4.4	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	21	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	230	mJ
$I_{AR}$	Avalanche Current (Note 1)	7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.3	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	20	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	83 0.67	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

**Thermal Characteristics**

Symbol	Parameter	FCD7N60/FCU7N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	83	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD7N60	FCD7N60TM	D-PAK	380mm	16mm	2500
FCD7N60	FCD7N60TF	D-PAK	380mm	16mm	2000
FCU7N60	FCU7N60	I-PAK	-	-	70

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

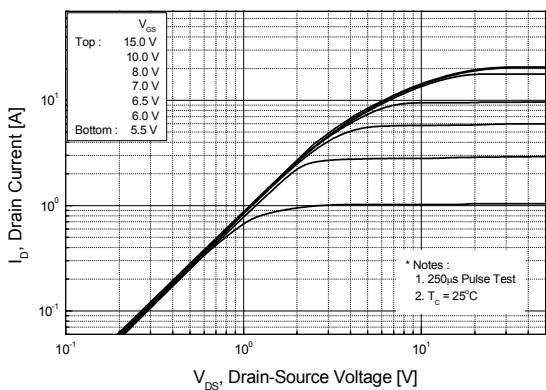
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	600	--	--	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 150°C	--	650	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 7A	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	--	--	1	μA
		V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A	--	0.53	0.6	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 3.5A (Note 4)	--	6	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	710	920	pF
C <sub>oss</sub>	Output Capacitance		--	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	34	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	22	29	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	60	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 7A R <sub>G</sub> = 25Ω  (Note 4, 5)	--	35	80	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		--	32	75	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 7A V <sub>GS</sub> = 10V  (Note 4, 5)	--	23	30	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.2	5.5	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	11.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A	--	360	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> /dt = 100A/μs (Note 4)	--	4.5	--	μC

### NOTES:

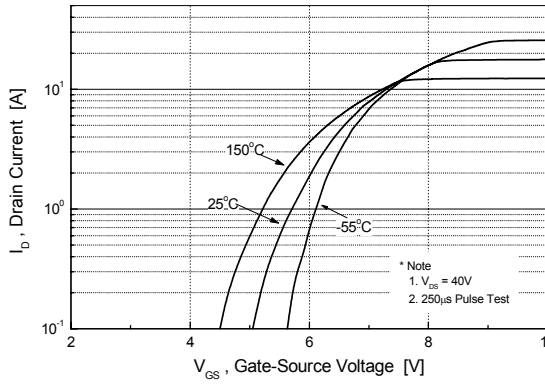
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 3.5A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 7A, di/dt ≤ 1200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

## Typical Performance Characteristics

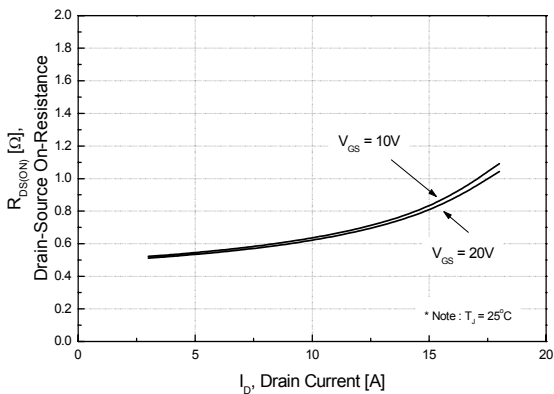
**Figure 1. On-Region Characteristics**



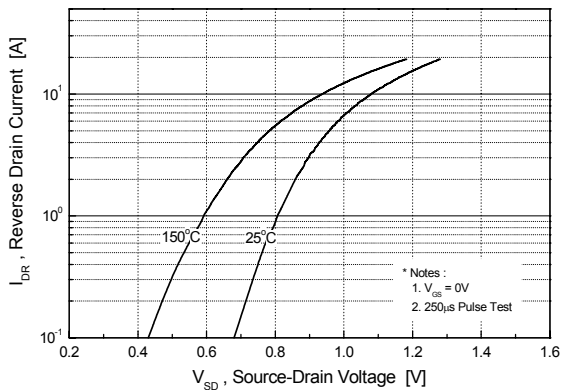
**Figure 2. Transfer Characteristics**



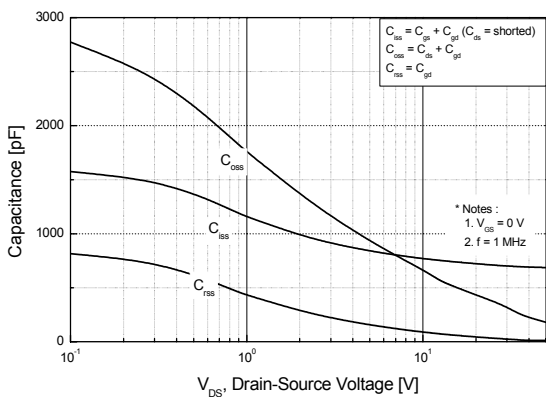
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



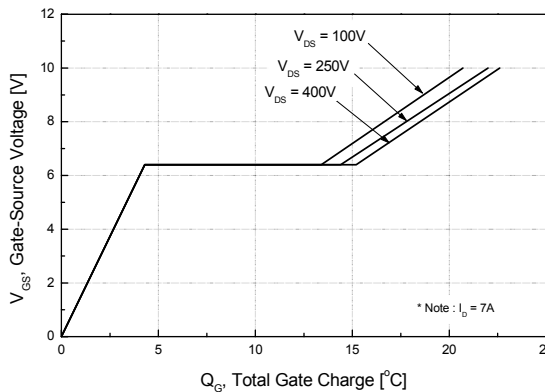
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

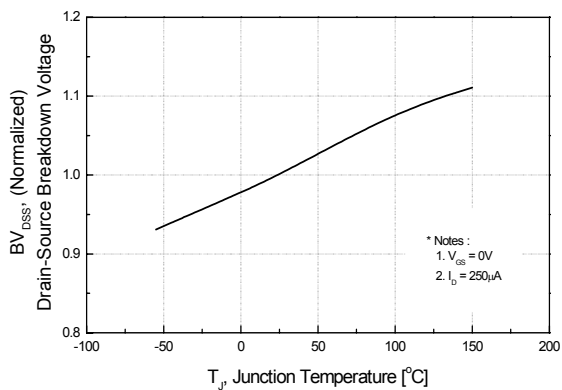


**Figure 6. Gate Charge Characteristics**

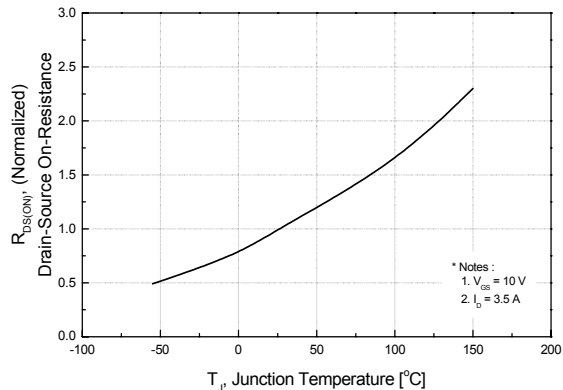


**Typical Performance Characteristics (Continued)**

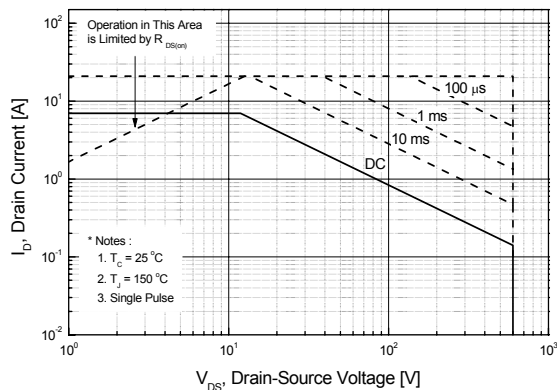
**Figure 7. Breakdown Voltage Variation vs. Temperature**



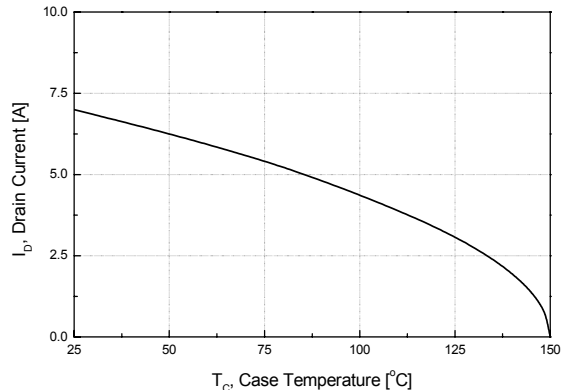
**Figure 8. On-Resistance Variation vs. Temperature**



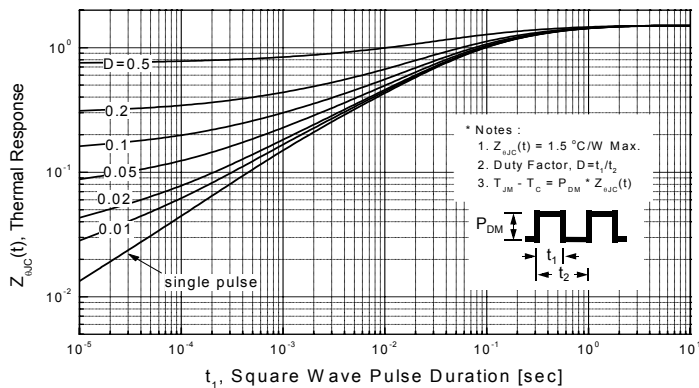
**Figure 9. Maximum Safe Operating Area**



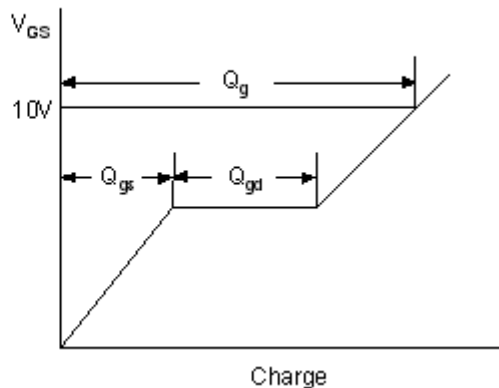
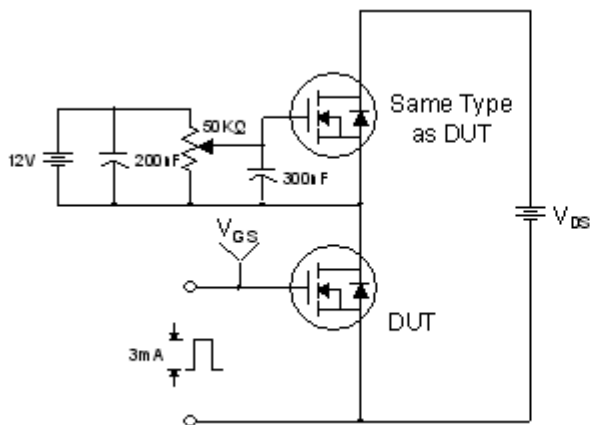
**Figure 10. Maximum Drain Current vs. Case Temperature**



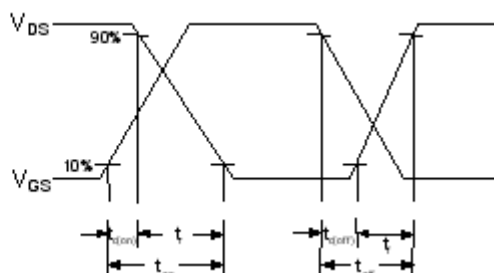
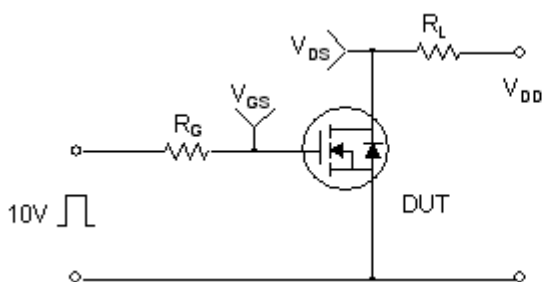
**Figure 11. Transient Thermal Response Curve**



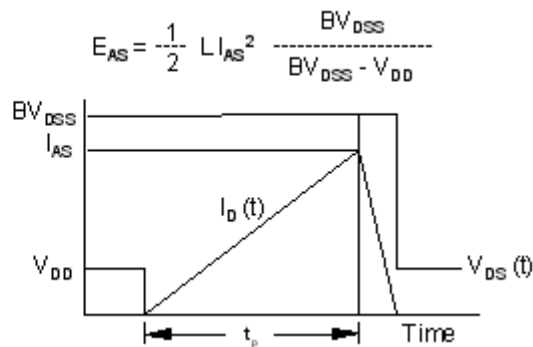
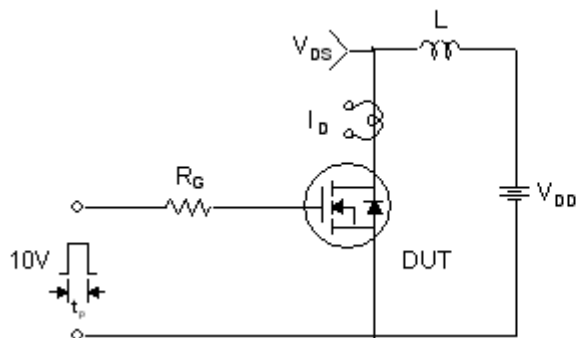
**Gate Charge Test Circuit & Waveform**



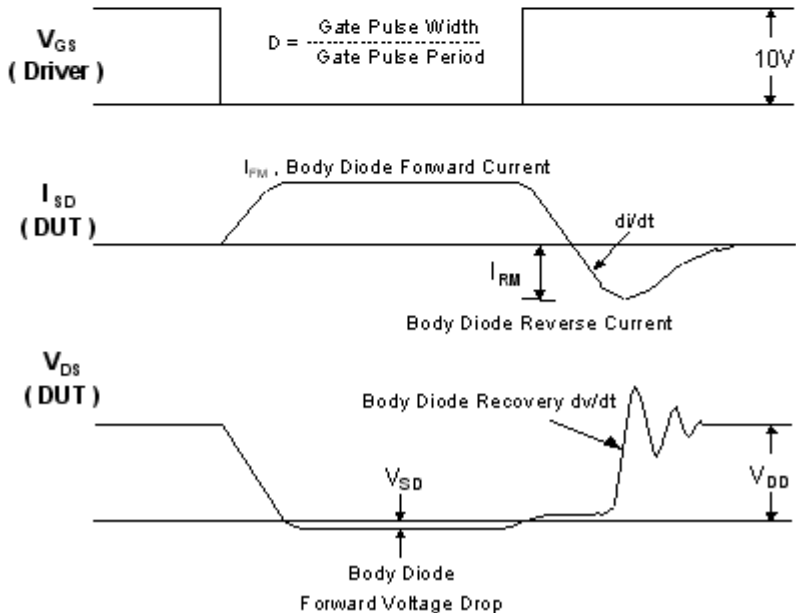
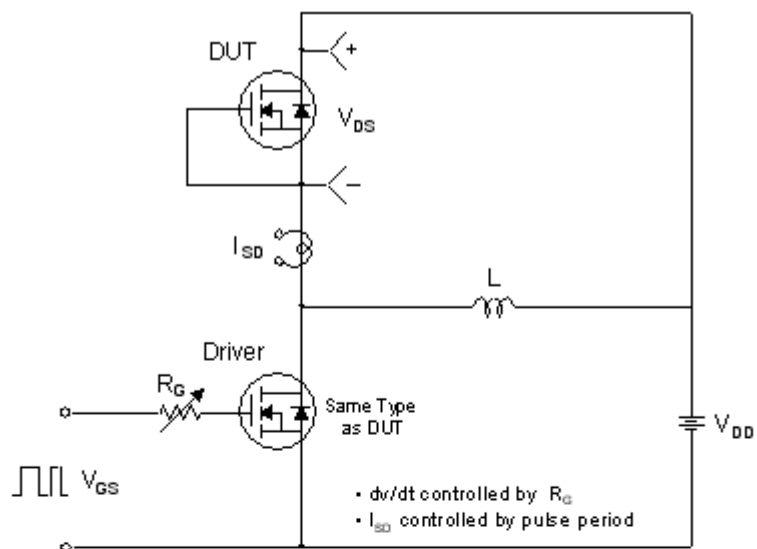
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

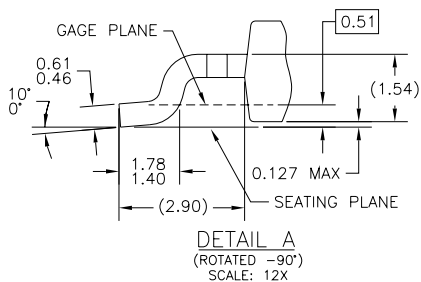
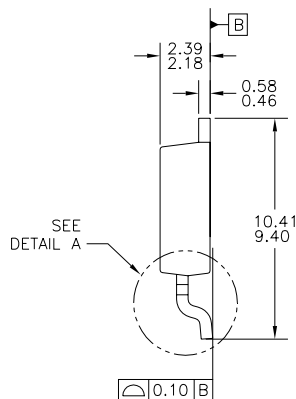
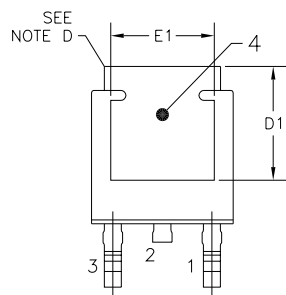
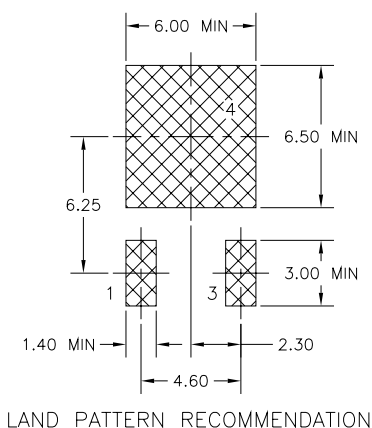
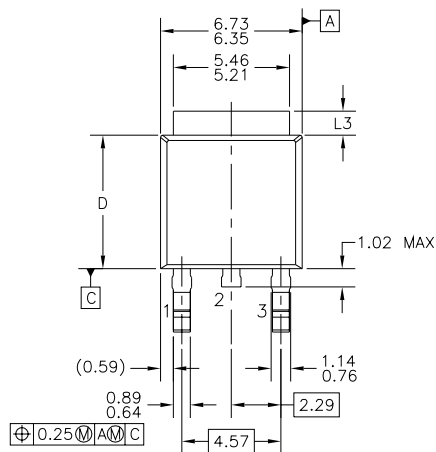


**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Mechanical Dimensions

### D-PAK

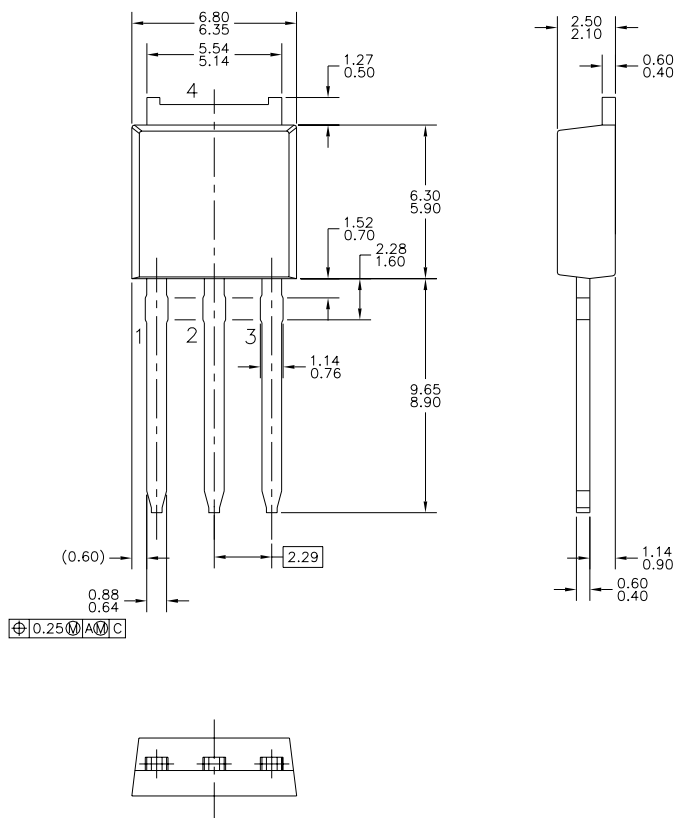


- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:
- |    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters



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Bottomless™	GTO™	OPTOLOGIC®	SPM™	VCX™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	Wire™
CoolFET™	I <sup>2</sup> C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E <sup>2</sup> CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QST™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
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Programmable Active Droop™				

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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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