



## Features

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual In-line Memory Module
- 4Mx64, 4Mx72 Extended Data Out Page Mode DIMMs
- Performance:

		-50	-60
t <sub>RAC</sub>	RAS Access Time	50ns	60ns
t <sub>CAC</sub>	CAS Access Time	13ns	15ns
t <sub>AA</sub>	Access Time From Address	25ns	30ns
t <sub>RC</sub>	Cycle Time	84ns	104ns
t <sub>HPC</sub>	EDO Mode Cycle Time	20ns	25ns

- Inputs and outputs are LVTTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Au contacts
- Optimized for byte-write non-parity, or ECC applications

- System Performance Benefits:
  - Non buffered for increased performance
  - Reduced noise (35 V<sub>SS</sub>/V<sub>CC</sub> pins)
  - Byte write, byte read accesses
  - Serial PDs
- Extended Data Out (EDO) Mode, Read-Modify-Write Cycles
- Refresh Modes:  $\overline{\text{RAS}}$ -Only, CBR and Hidden Refresh
- 2048 refresh cycles distributed across 32ms (11/11 addressing)
- 4096 refresh cycles distributed across 64ms (12/10 addressing)
- 11/11 or 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

## Description

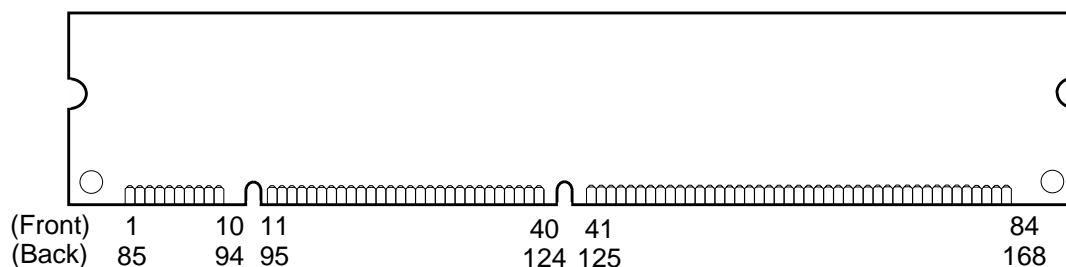
IBM11N4645BB/IBM11N4645CB are industry standard 168-pin 8-byte Dual In-line Memory Modules (DIMMs) which are organized as 4Mx64 and 4Mx72 high speed memory arrays designed with EDO DRAMs for non-parity or ECC applications. The DIMMs use 16 (x64) or 18 (x72) 4Mx4 EDO DRAMs in SOJ packages. The use of EDO DRAMs allows for a reduction in Page Mode Cycle time from 40ns (Fast Page) to 20ns for 50ns DRAM modules.

The DIMMs use serial presence detects implemented via a serial EEPROM using the two pin I<sup>2</sup>C protocol. This communication protocol uses Clock (SCL) and Data I/O (SDA) lines to synchronously

clock data between the master (system logic) and the slave EEPROM device (DIMM). The EEPROM device address pins (SA0-2) are brought out to the DIMM tabs to allow 8 unique DIMM/EEPROM addresses. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes of serial PD data are available to the customer.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products include the buffered DIMMs (x64 non-parity and x72 ECC Optimized) for applications which can benefit from the on-card buffers.

## Card Outline





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**4M x 64/72 DRAM Module**

## Pin Description

RAS0, RAS2	Row Address Strobe	V <sub>CC</sub>	Power (3.3V)
CAS0 - CAS7	Column Address Strobe	V <sub>SS</sub>	Ground
WE0, WE2	Read/write Input	NC	No Connect
OE0, OE2	Output Enable	DU	Don't Use
A0 - A11	Address Inputs	SCL	Serial Presence Detect Clock Input
DQx	Data Input/Output	SDA	Serial Presence Detect Data Input
CBx	Check Bit Data Input/Output	SA0-2	Serial Presence Detect Address Inputs

## Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V <sub>SS</sub>	85	V <sub>SS</sub>	22	CB	106	CB5	43	V <sub>SS</sub>	127	V <sub>SS</sub>	64	V <sub>SS</sub>	148	V <sub>SS</sub>
2	DQ0	86	DQ32	23	V <sub>SS</sub>	107	V <sub>SS</sub>	44	OE2	128	DU	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	RAS2	129	NC	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	CAS2	130	CAS6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V <sub>CC</sub>	110	V <sub>CC</sub>	47	CAS3	131	CAS7	68	V <sub>SS</sub>	152	V <sub>SS</sub>
6	V <sub>CC</sub>	90	V <sub>CC</sub>	27	WE0	111	DU	48	WE2	132	DU	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	CAS0	112	CAS4	49	V <sub>CC</sub>	133	V <sub>CC</sub>	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	CAS1	113	CAS5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	RAS0	114	NC	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	OE0	115	DU	52	CB2	136	CB6	73	V <sub>CC</sub>	157	V <sub>CC</sub>
11	DQ8	95	DQ40	32	V <sub>SS</sub>	116	V <sub>SS</sub>	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V <sub>SS</sub>	96	V <sub>SS</sub>	33	A0	117	A1	54	V <sub>SS</sub>	138	V <sub>SS</sub>	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V <sub>SS</sub>	162	V <sub>SS</sub>
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	NC	163	NC
17	DQ13	101	DQ45	38	A10	122	A11	59	V <sub>CC</sub>	143	V <sub>CC</sub>	80	NC	164	NC
18	V <sub>CC</sub>	102	V <sub>CC</sub>	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	V <sub>CC</sub>	124	V <sub>CC</sub>	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V <sub>CC</sub>	125	DU	62	DU	146	DU	83	SCL	167	SA2
21	CB0	105	CB4	42	DU	126	DU	63	NC	147	NC	84	V <sub>CC</sub>	168	V <sub>CC</sub>

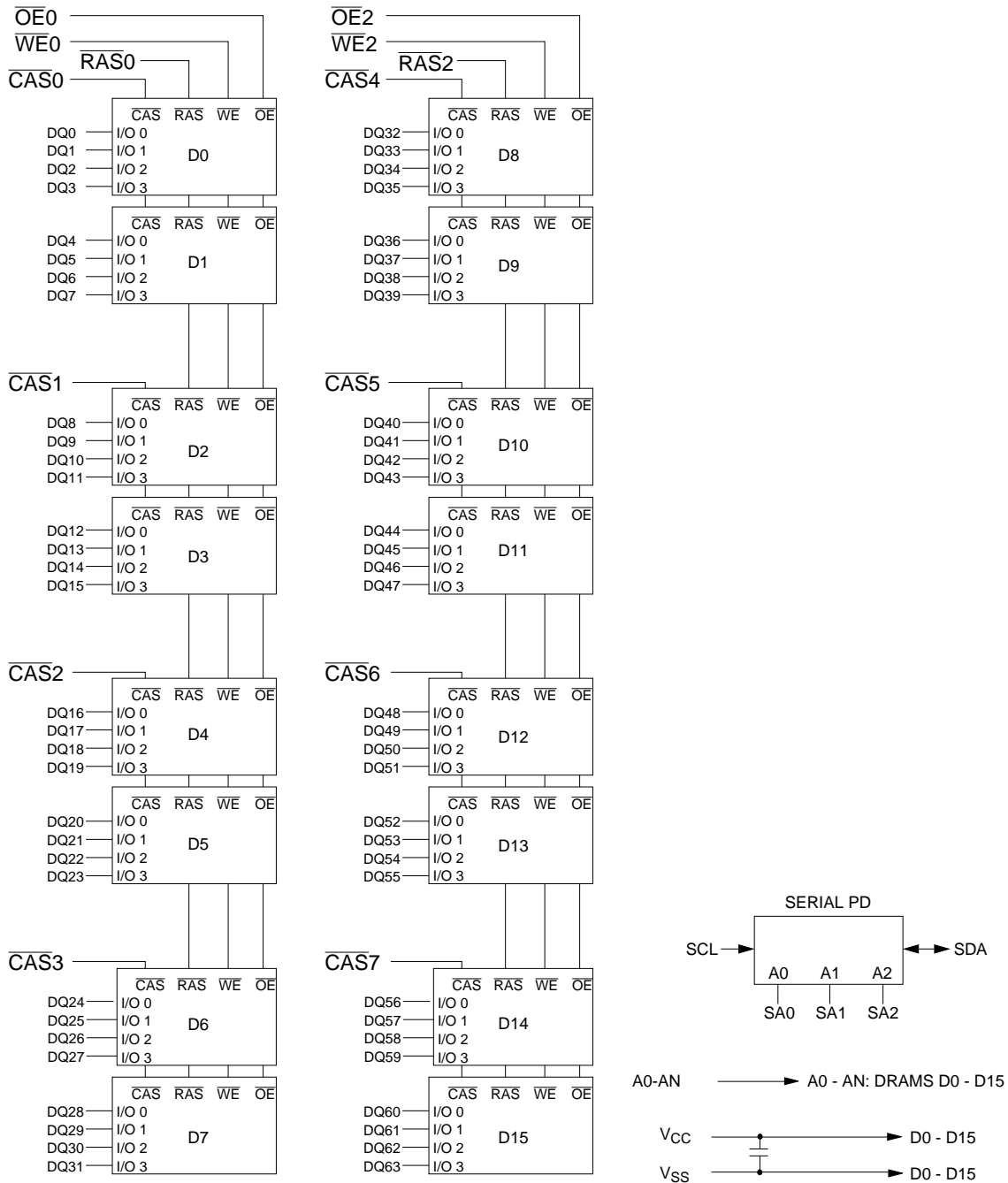
**Note:** All pin assignments are consistent for all 8 Byte unbuffered versions.

## Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimension	Power
IBM11N4645BB-60J	4Mx64	60ns	11/11	Au	5.25"x1.0"x 0.354"	3.3V
IBM11N4645CB-60J		60ns	12/10			
IBM11N4735BB-60J	4M x 72	60ns	11/11			
IBM11N4735CB-60J		60ns	12/10			
IBM11N4735CB-50J		50ns	12/10			



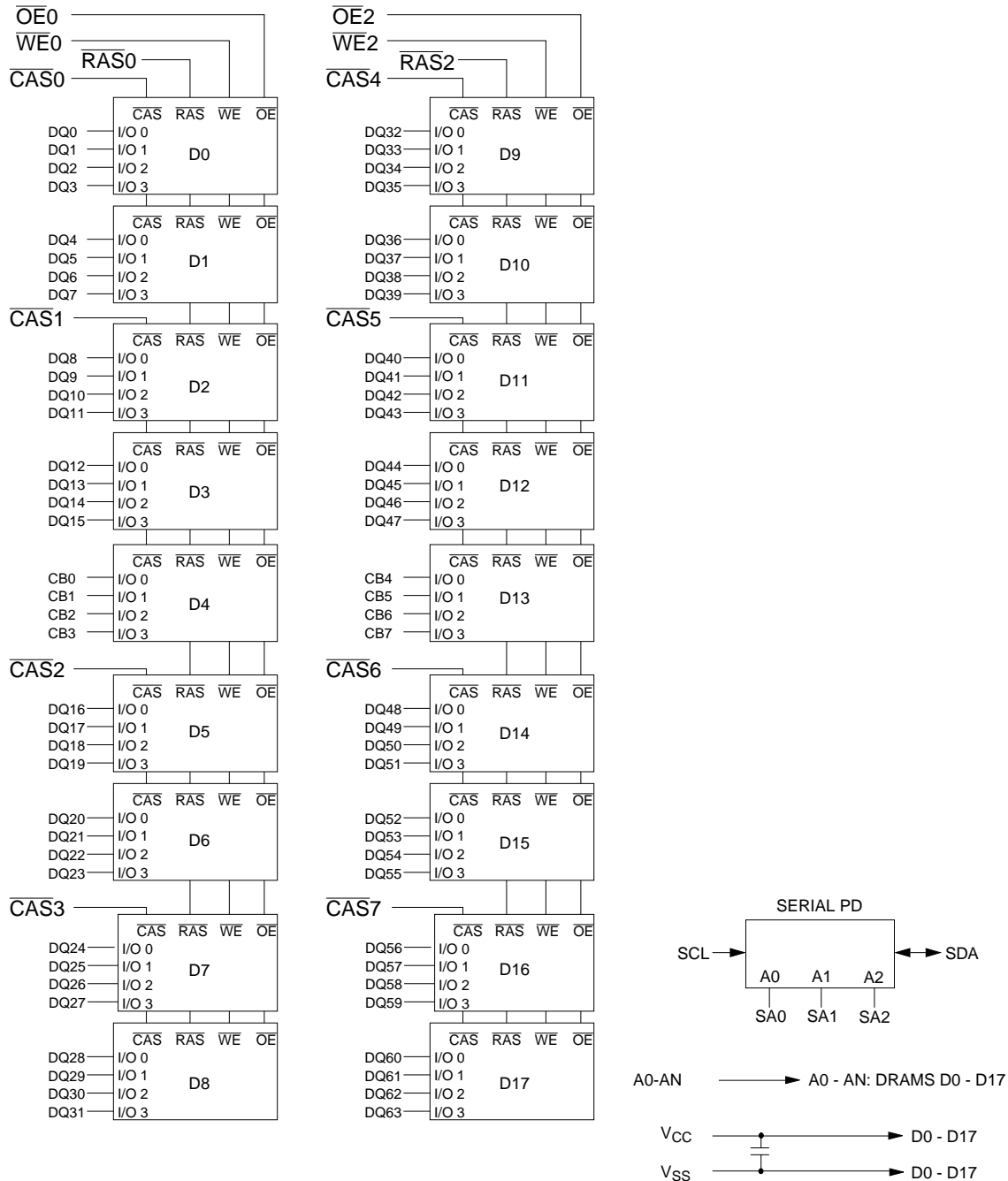
x64 DIMM Block Diagram (1 Bank, x4 DRAMs)





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 4M x 64/72 DRAM Module

### x72 ECC DIMM Block Diagram (1 Bank, x4 DRAMs)





## Truth Table

Function	RAS	CAS	WE	OE	Row Address	Column Address	DQx	
Standby	H	H→X	X	X	X	X	High Impedance	
Read	L	L	H	L	Row	Col	Valid Data Out	
Early-Write	L	L	L	X	Row	Col	Valid Data In	
Late-Write	L	L	H→L	H	Row	Col	Valid Data In	
RMW	L	L	H→L	L→H	Row	Col	Valid Data In/Out	
EDO Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	Valid Data Out	
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out	
EDO Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	Valid Data In	
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In	
EDO Page Mode - RMW 1st Cycle	L	H→L	H→L	L→H	Row	Col	Valid Data In/Out	
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data In/Out	
RAS-Only Refresh	L	H	X	X	Row	N/A	High Impedance	
CAS-Before-RAS Refresh	H→L	L	H	X	X	X	High Impedance	
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	H	X	Row	Col	Data In



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## Serial Presence Detect

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)
0	Number of Serial PD Bytes Written during Production	128	80
1	Total Number of Bytes in Serial PD device	256	08
2	Fundamental Memory Type	EDO	02
3	Number of Row Addresses on Assembly	12	0C
		11	0B
4	Number of Column Addresses on Assembly	10	0A
		11	0B
5	Number of DIMM Banks	1	01
6 - 7	Data Width of Assembly	4M x 64	x64
		4M x 72	x72
8	Voltage Interface Level of this Assembly	LVTTTL	01
9	$\overline{\text{RAS}}$ Access	50ns	32
		60ns	3C
10	$\overline{\text{CAS}}$ Access	13ns	0D
		15ns	0F
11	DIMM Configuration Type	4M x 64	Non-Parity
		4M x 72	ECC
12	Assembly Refresh Rate/Type	Normal 15.6us	00
13	Primary DRAM Data Width	x4	04
14	Error Checking DRAM Data Width	4M x 64	N/A
		4M x 72	x4
15 - 62	Reserved	Undefined	00
63	Checksum for bytes 0 - 62	Checksum Data	cc
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000
72	Module Manufacturing Location	Toronto, Canada	91
		Vimercate, Italy	53
73 - 90	Module Part Number (70ns examples not shown)	4M x 64	ASCII '11N4645BB'R'-60J' 31314E343634354242rr2D36304A20202020
		4M x 64	ASCII '11N4645CB'R'-60J' 31314E343634354342rr2D36304A20202020
		4M x 72	ASCII '11N4735BB'R'-60J' 31314E343733354242rr2D36304A20202020
		4M x 72	ASCII '11N4735CB'R'-60J' 31314E343733354342rr2D36304A20202020
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20
93 - 94	Module Manufacturing Date	Week/Year Code	wwwy
95 - 98	Module Serial Number	Serial Number	ssssssss
99 - 127	Reserved	Undefined	00
128 - 255	Open for Customer Use	Undefined	00

cc = Checksum Data byte, 00-FF (Hex)  
 "R" = Alphanumeric revision code, A-Z, 0-9  
 rr = ASCII coded revision code byte "R"  
 ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex)  
 yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex)  
 ss = Serial number data byte, 00-FF (Hex)



## Absolute Maximum Ratings

Symbol	Parameter	Rating (3.3V)		Units	Notes
V <sub>CC</sub>	Power Supply Voltage	-0.5 to +4.6		V	1
V <sub>IN</sub>	Input Voltage	-0.5 to min (V <sub>CC</sub> + 0.5, 4.6)		V	1
V <sub>IN/OUT</sub> (SPD)	Input Voltage (Serial PD Device)	-0.3 to +6.5		V	1
V <sub>OUT</sub>	Output Voltage	-0.5 to min (V <sub>CC</sub> + 0.5, 4.6)		V	1
T <sub>OPR</sub>	Operating Temperature	0 to +70		°C	1
T <sub>STG</sub>	Storage Temperature	-55 to +125		°C	1
P <sub>D</sub>	Power Dissipation	11/11 Addressing	12/10 Addressing	W	1, 2
		x64	4.9		
		x72	5.5	4.9	
I <sub>OUT</sub>	Short Circuit Output Current	50		mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Power calculated with 60ns part.

## Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70°C)

Symbol	Parameter	3.3V			Units	Notes
		Min	Typ	Max		
V <sub>CC</sub>	Supply Voltage	3.0	3.3	3.6	V	1
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 0.5	V	1, 2
V <sub>IL</sub>	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V<sub>SS</sub>.
2. V<sub>IH</sub> may overshoot to V<sub>CC</sub> + 1.2V for pulse widths of ≤ 4.0ns (or V<sub>CC</sub> + 1.0V for ≤ 8.0ns). Additionally, V<sub>IL</sub> may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

## Capacitance (T<sub>A</sub> = 0 to +70°C, V<sub>CC</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Max		Units
		x64	x72	
C <sub>I1</sub>	Input Capacitance (A0-A11)	90	100	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	70	75	pF
C <sub>I3</sub>	Input Capacitance ( $\overline{\text{CAS}}$ )	20	25	pF
C <sub>I4</sub>	Input Capacitance ( $\overline{\text{SCL}}$ , SA0-3)	8	8	pF
C <sub>IO1</sub>	Input/Output Capacitance (DQx, CBx)	11	11	pF
C <sub>IO2</sub>	Input/Output Capacitance (SDA)	10	10	pF



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**4M x 64/72 DRAM Module**

**DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Parameter	11/11 Addressing				12/10 Addressing				Units	Notes	
		x64		x72		x64		x72				
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
I <sub>CC1</sub>	Operating Current	-50	—	—	—	—	—	—	—	1530	mA	1, 2, 3
	Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC} = t_{RC \text{ min.}}$ )	-60	—	1360	—	1530	—	1200	—	1350		
I <sub>CC2</sub>	Standby Current (TTL)	—	32	—	36	—	32	—	36		mA	
	Power Supply Standby Current (RAS = CAS = $V_{IH}$ )											
I <sub>CC3</sub>	$\overline{\text{RAS}}$ Only Refresh Current	-50	—	—	—	—	—	—	—	1530	mA	1, 3
	Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode (RAS Cycling, CAS = $V_{IH}$ : $t_{RC} = t_{RC \text{ min.}}$ )	-60	—	1360	—	1530	—	1200	—	1350		
I <sub>CC4</sub>	EDO Page Mode Current	-50	—	—	—	—	—	—	—	1530	mA	1, 2, 3
	Average Power Supply Current, EDO Page Mode (RAS = $V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{HPC} = t_{HPC \text{ min.}}$ )	-60	—	1040	—	1170	—	1040	—	1170		
I <sub>CC5</sub>	Standby Current (CMOS)	—	16	—	18	—	16	—	18		mA	
	Power Supply Standby Current (RAS = CAS = $V_{CC} - 0.2\text{V}$ )											
I <sub>CC6</sub>	$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current	-50	—	—	—	—	—	—	—	1530	mA	1, 3
	Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode (RAS, $\overline{\text{CAS}}$ , Cycling: $t_{RC} = t_{RC \text{ min.}}$ )	-60	—	1360	—	1530	—	1200	—	1350		
I <sub>I(L)</sub>	Input Leakage Current	$\overline{\text{RAS}},$ $\overline{\text{WE}}, \overline{\text{OE}}$	-80	+80	-90	+90	-80	+80	-90	+90	$\mu\text{A}$	
	Input Leakage Current, any input ( $0.0 \leq V_{IN} \leq (V_{CC} + 0.3\text{V})$ ), All Other Pins Not Under Test = 0V	$\overline{\text{CAS}}$	-20	+20	-30	+30	-20	+20	-30	+30		
	Address	-160	+160	-180	+180	-160	+160	-180	+180			
I <sub>O(L)</sub>	Output Leakage Current ( $D_{OUT}$ is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$ )		-10	+10	-10	+10	-10	+10	-10	+10	$\mu\text{A}$	
V <sub>OH</sub>	Output Level (TTL) Output "H" Level Voltage ( $I_{OUT} = -2.5\text{mA}$ )		2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
V <sub>OL</sub>	Output Level (TTL) Output "L" Level Voltage ( $I_{OUT} = +2.1\text{mA}$ )		0.0	0.4	0.0	0.4	0.0	0.4	0.0	0.4	V	

- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> depend on cycle rate.
- I<sub>CC1</sub> and I<sub>CC4</sub> depend on output loading. Specified values are obtained with the output open.
- Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ . In the case of I<sub>CC4</sub>, it can be changed once or less when  $\overline{\text{CAS}} = V_{IH}$ .




**AC Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of  $200\mu\text{s}$  is required after power-up followed by  $8 \overline{\text{RAS}}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of  $8 \overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles instead of  $8 \overline{\text{RAS}}$  only refresh cycles is required..
- AC measurements assume  $t_T = 2\text{ns}$ .

**Read, Write, Read-Modify-Write and Refresh Cycles** (Common Parameters)

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
$t_{RC}$	Random Read or Write Cycle Time	84	—	104	—	ns	
$t_{RP}$	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns	
$t_{CP}$	$\overline{\text{CAS}}$ Precharge Time	8	—	10	—	ns	
$t_{RAS}$	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	ns	
$t_{CAS}$	$\overline{\text{CAS}}$ Pulse Width	8	10K	10	10K	ns	
$t_{ASR}$	Row Address Setup Time	0	—	0	—	ns	
$t_{RAH}$	Row Address Hold Time	10	—	10	—	ns	
$t_{ASC}$	Column Address Setup Time	0	—	0	—	ns	
$t_{CAH}$	Column Address Hold Time	8	—	10	—	ns	
$t_{RCD}$	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	14	37	14	45	ns	1
$t_{RAD}$	$\overline{\text{RAS}}$ to Column Address Delay Time	12	25	12	30	ns	2
$t_{RSH}$	$\overline{\text{RAS}}$ Hold Time	8	—	10	—	ns	
$t_{CSH}$	$\overline{\text{CAS}}$ Hold Time	43	—	50	—	ns	
$t_{CRP}$	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	
$t_{ODD}$	$\overline{\text{OE}}$ to $D_{IN}$ Delay Time	15	—	15	—	ns	3
$t_{DZO}$	$\overline{\text{OE}}$ Delay Time from $D_{IN}$	0	—	0	—	ns	4
$t_{DZC}$	$\overline{\text{CAS}}$ Delay Time from $D_{IN}$	0	—	0	—	ns	4
$t_T$	Transition Time (Rise and Fall)	2	30	2	30	ns	

- Operation within the  $t_{RCD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met. The  $t_{RCD}(\text{max})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled by  $t_{CAC}$ .
- Operation within the  $t_{RAD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met. The  $t_{RAD}(\text{max})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled by  $t_{AA}$ .
- Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.



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## Write Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
$t_{WCS}$	Write Command Set Up Time	0	—	0	—	ns	1
$t_{WCH}$	Write Command Hold Time	7	—	10	—	ns	
$t_{WP}$	Write Command Pulse Width	7	—	10	—	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	7	—	10	—	ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	7	—	10	—	ns	
$t_{DS}$	$D_{IN}$ Setup Time	0	—	0	—	ns	2
$t_{DH}$	$D_{IN}$ Hold Time	7	—	10	—	ns	2

- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ , and  $t_{AWD}$  are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
- Data-in set-up and hold is measured from the latter of the two timings,  $\overline{CAS}$  or  $\overline{WE}$ .



## Read Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
$t_{RAC}$	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2
$t_{CAC}$	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 2
$t_{AA}$	Access Time from Address	—	25	—	30	ns	1, 2
$t_{OEA}$	Access Time from $\overline{OE}$	—	13	—	15	ns	1, 2
$t_{RCS}$	Read Command Setup Time	0	—	0	—	ns	
$t_{RCH}$	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
$t_{RRH}$	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	
$t_{CLZ}$	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
$t_{OES}$	$\overline{OE}$ setup time prior to $\overline{CAS}$	5	—	5	—	ns	
$t_{ORD}$	$\overline{OE}$ setup time prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	ns	
$t_{CDD}$	$\overline{CAS}$ to $D_{IN}$ Delay Time	13	—	15	—	ns	5
$t_{OEZ}$	Output Buffer Turn-off Delay from $\overline{OE}$	—	13	—	15	ns	4
$t_{OFF}$	Output Buffer Turn-off Delay	—	13	—	15	ns	4, 6

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{CPA}$ ,  $t_{AA}$ ,  $t_{OEA}$ .
3. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied.
4.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
6.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever is last.



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## Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
$t_{RWC}$	Read-Modify-Write Cycle Time	110	—	135	—	ns	
$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	—	79	—	ns	1
$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	—	34	—	ns	1
$t_{AWD}$	Column Address to $\overline{WE}$ Delay Time	42	—	49	—	ns	1
$t_{OEH}$	$\overline{OE}$ Command Hold Time	7	—	10	—	ns	

1.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ , and  $t_{AWD}$  are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

## EDO Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{HCAS}$	$\overline{CAS}$ Pulse Width (EDO Page Mode)	8	10K	10	10K	ns	
$t_{HPC}$	EDO Page Mode Cycle Time (Read/Write)	20	—	25	—	ns	
$t_{HPRWC}$	EDO Page Mode Read Modify Write Cycle Time	51	—	60	—	ns	
$t_{DOH}$	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
$t_{WHZ}$	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	ns	
$t_{WPZ}$	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	ns	
$t_{CPRH}$	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	ns	
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge	—	28	—	35	ns	1
$t_{RASP}$	EDO Page Mode $\overline{RAS}$ Pulse Width	50	125K	60	125K	ns	
$t_{OEP}$	$\overline{OE}$ High Pulse Width	5	—	10	—	ns	
$t_{OEHC}$	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	5	—	10	—	ns	

1. Measured with the specified current load and 100pF at  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ .



## Refresh Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
$t_{CSR}$	$\overline{CAS}$ Setup Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
$t_{WRP}$	$\overline{WE}$ Setup Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
$t_{WRH}$	$\overline{WE}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
$t_{RPC}$	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
$t_{REF}$	Refresh Period	—	32	—	32	ms	1
		—	64	—	64	ms	2

- 2048 refreshes are required every 32ms (11/11 addressing).
- 4086 refreshes are required every 64ms (12/10 addressing).

## Presence Detect Read and Write Cycle

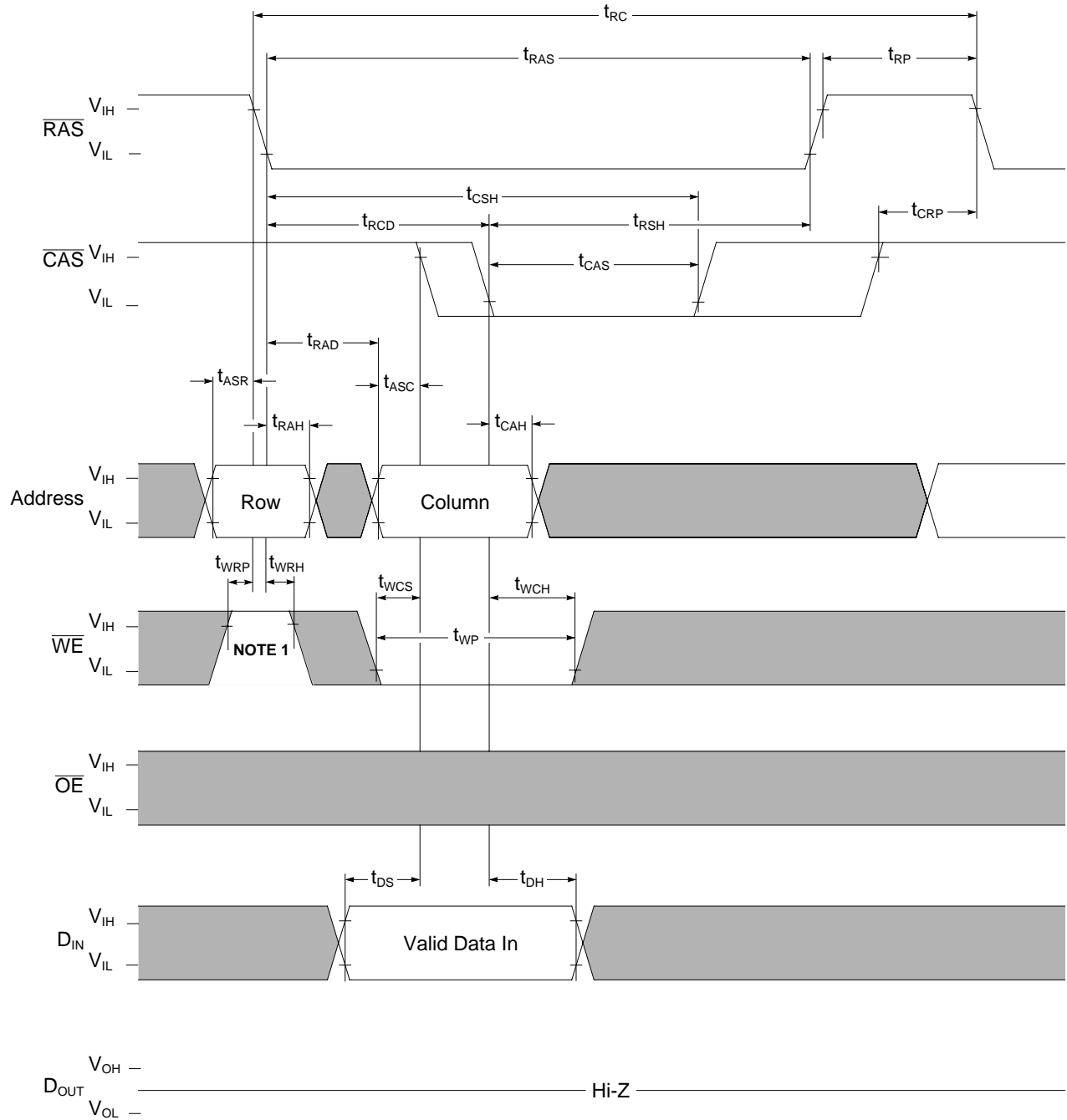
Symbol	Parameter	Min	Max	Unit	Notes
$f_{SCL}$	SCL Clock Frequency		100	KHZ	
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s	
$t_{BUF}$	Time the Bus Must Be Free before a New Transmission Can Start	4.7		$\mu$ s	
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s	
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s	
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s	
$t_{SU:STA}$	Start Condition Setup Time(for a Repeated Start Condition)	4.7		$\mu$ s	
$t_{HD:DAT}$	Data in Hold Time	0		$\mu$ s	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
$t_r$	SDA and SCL Rise Time		1	$\mu$ s	
$t_f$	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s	
$t_{DH}$	Data Out Hold Time	300		ns	
$t_{WR}$	Write Cycle Time		15	ms	1

- The write cycle time( $t_{WR}$ ) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.





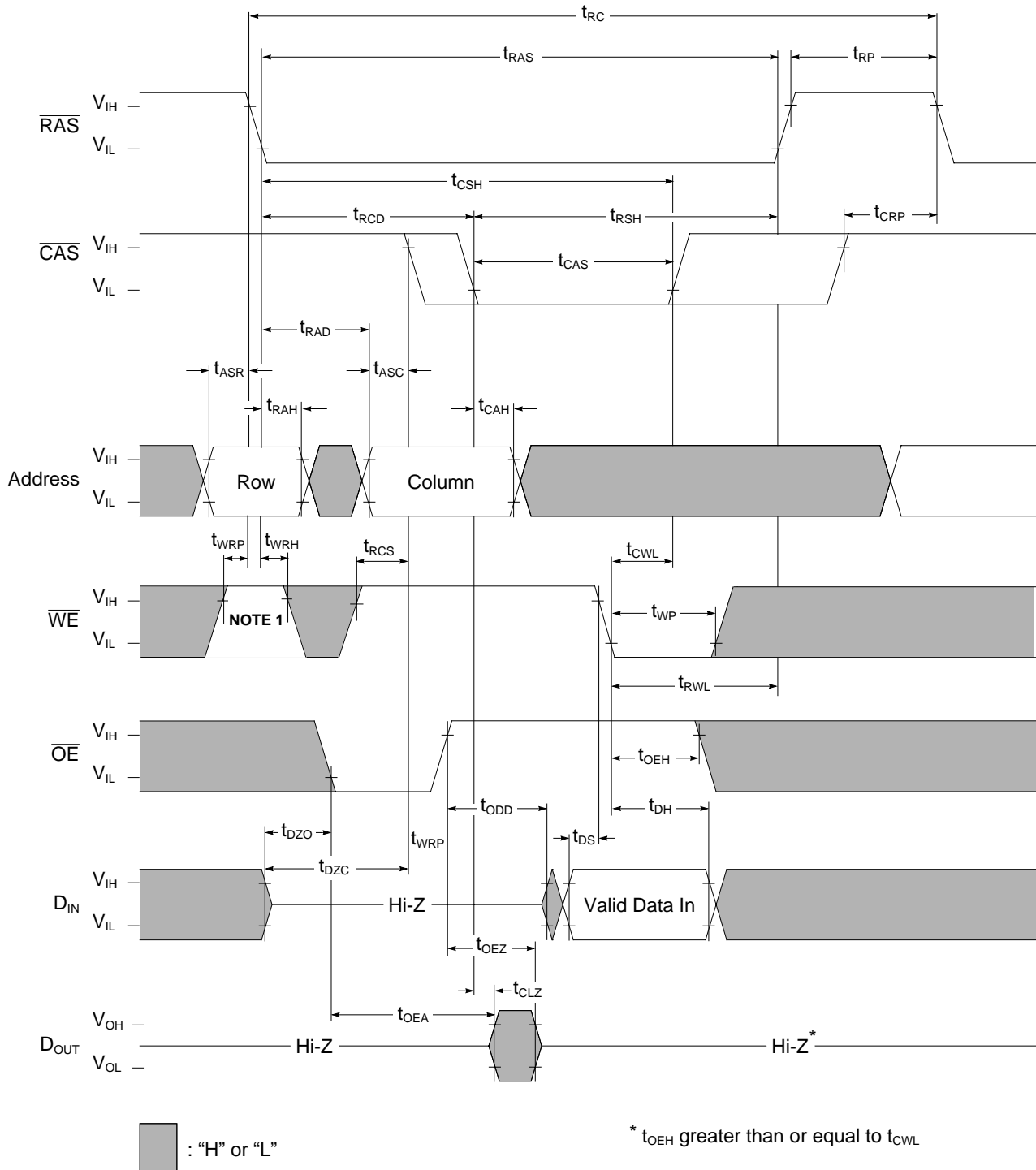
### Write Cycle (Early Write)



█ : "H" or "L"

**NOTE 1:** Implementing  $\overline{WE}$  at  $\overline{RAS}$  time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

### Write Cycle (Late Write)

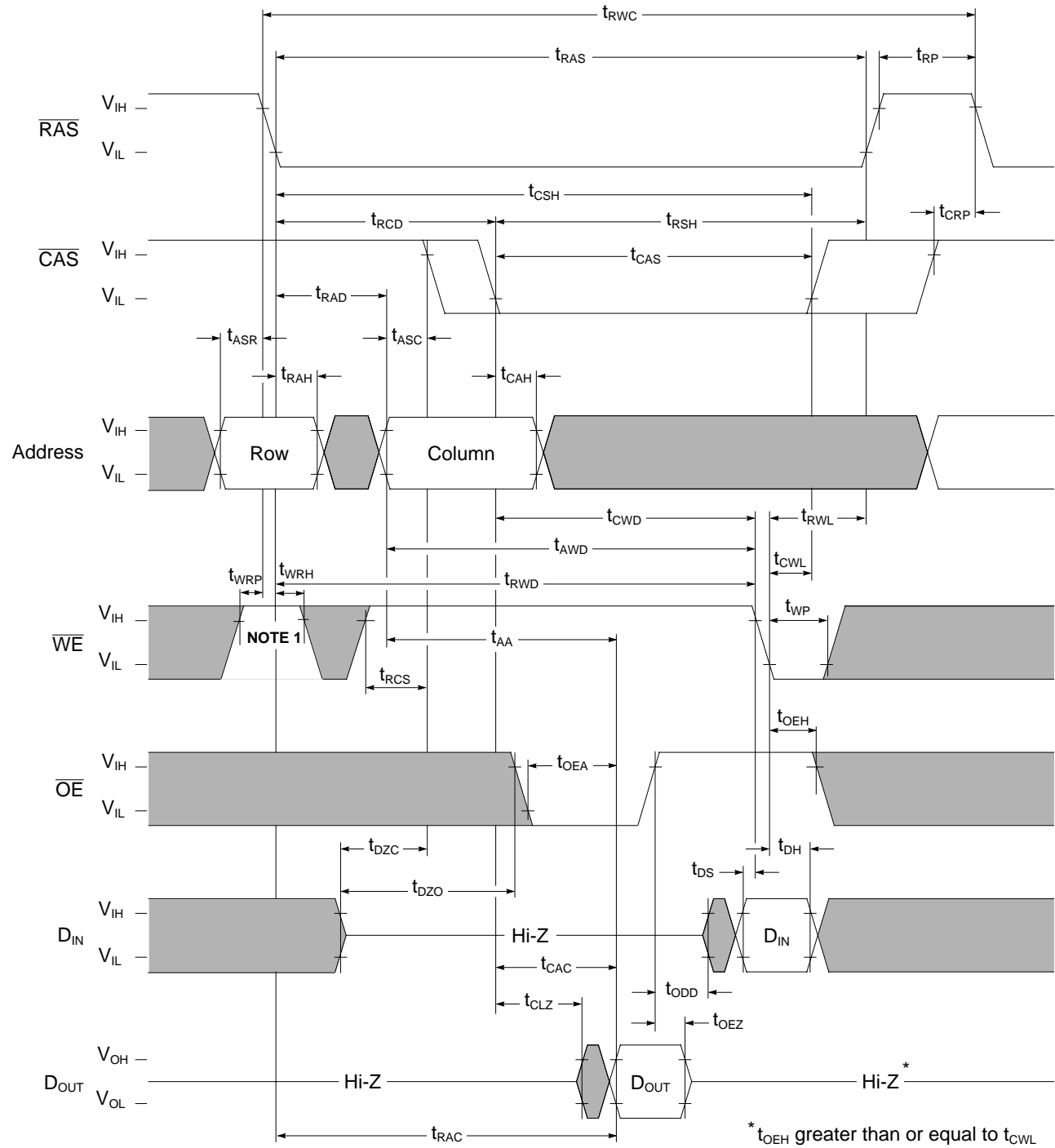


**NOTE 1:** Implementing  $\overline{WE}$  at  $\overline{RAS}$  time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.





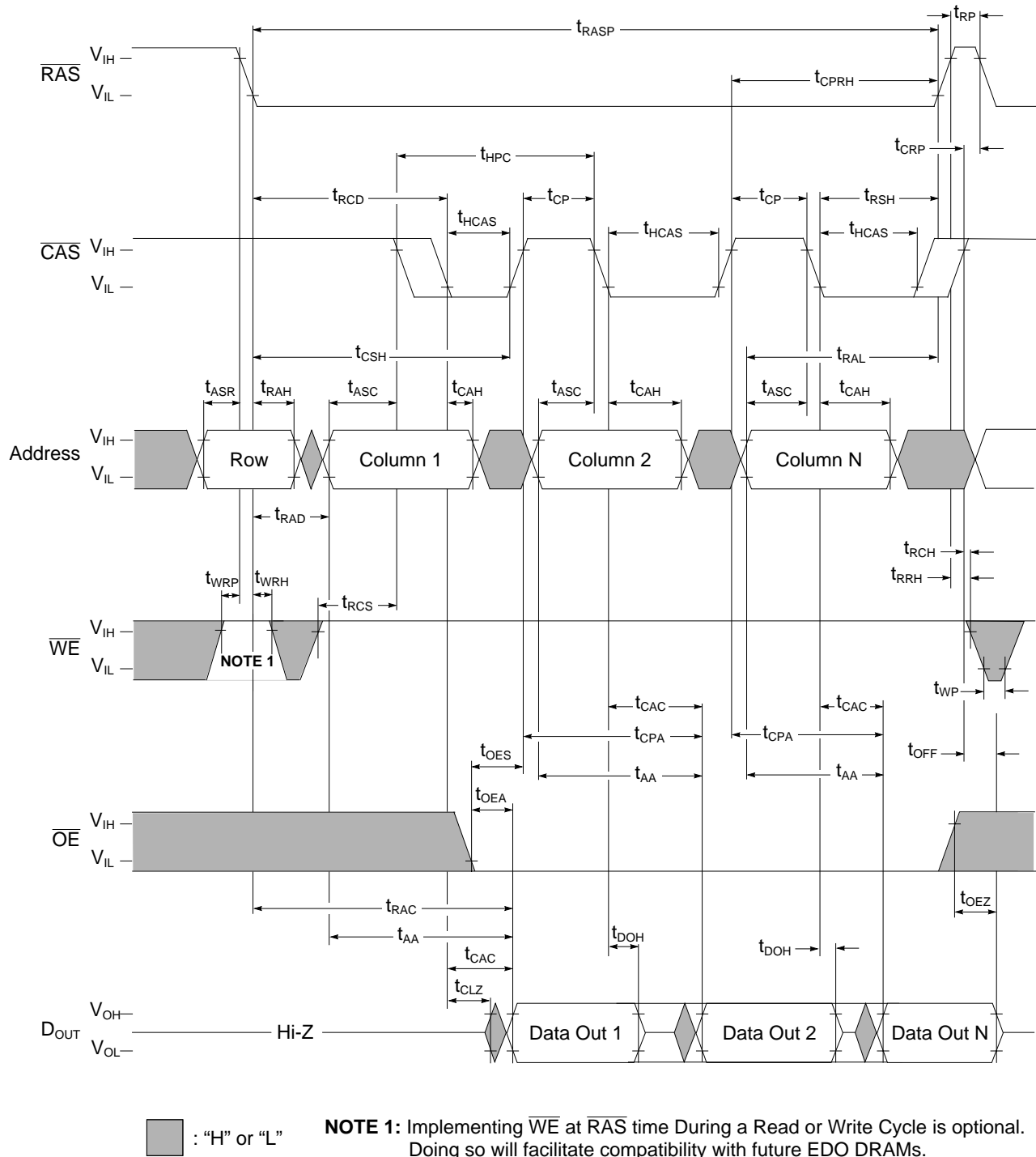
### Read-Modify-Write-Cycle





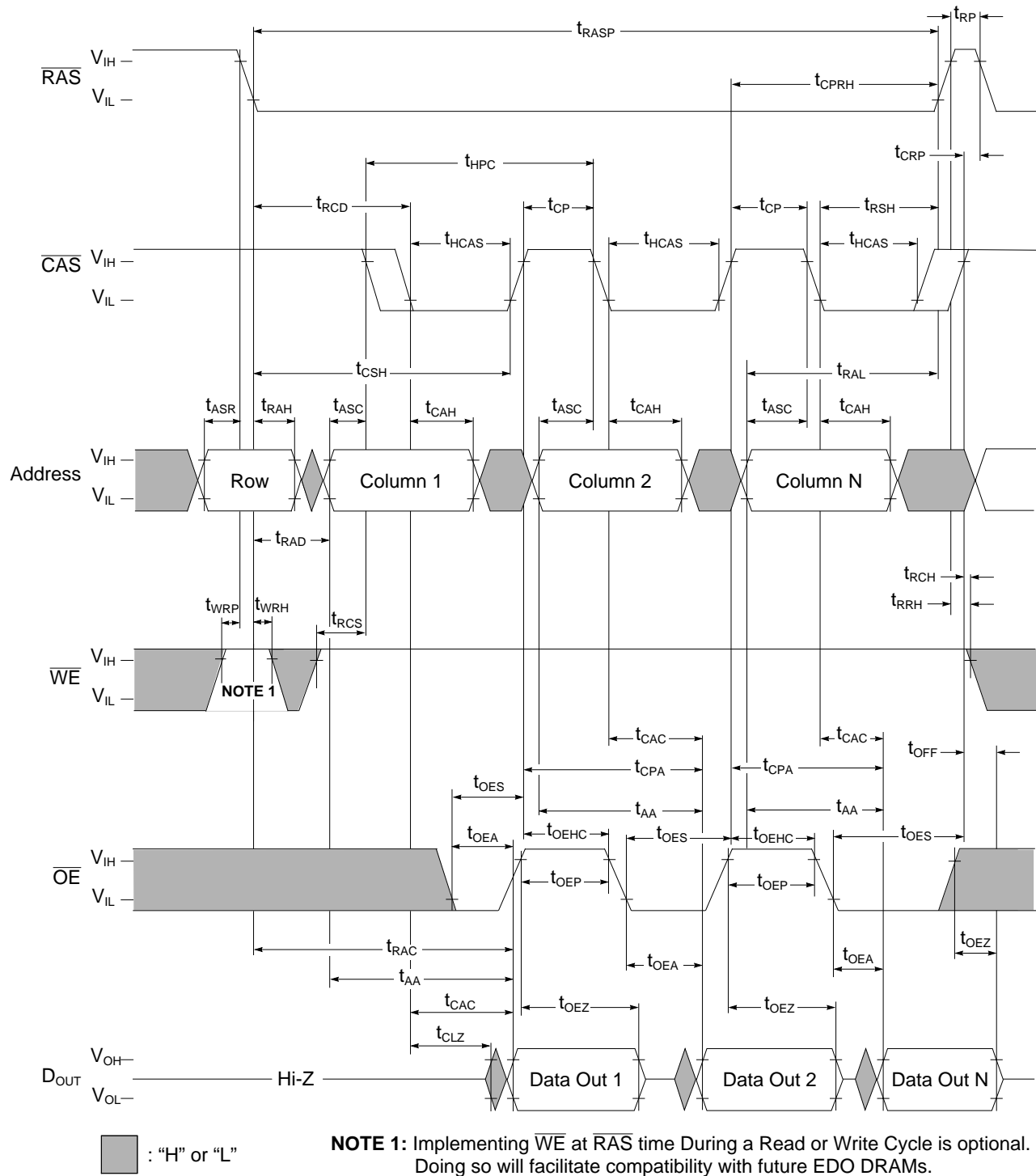
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### EDO Page Mode Read Cycle





### EDO Page Mode Read Cycle ( $\overline{OE}$ Control)



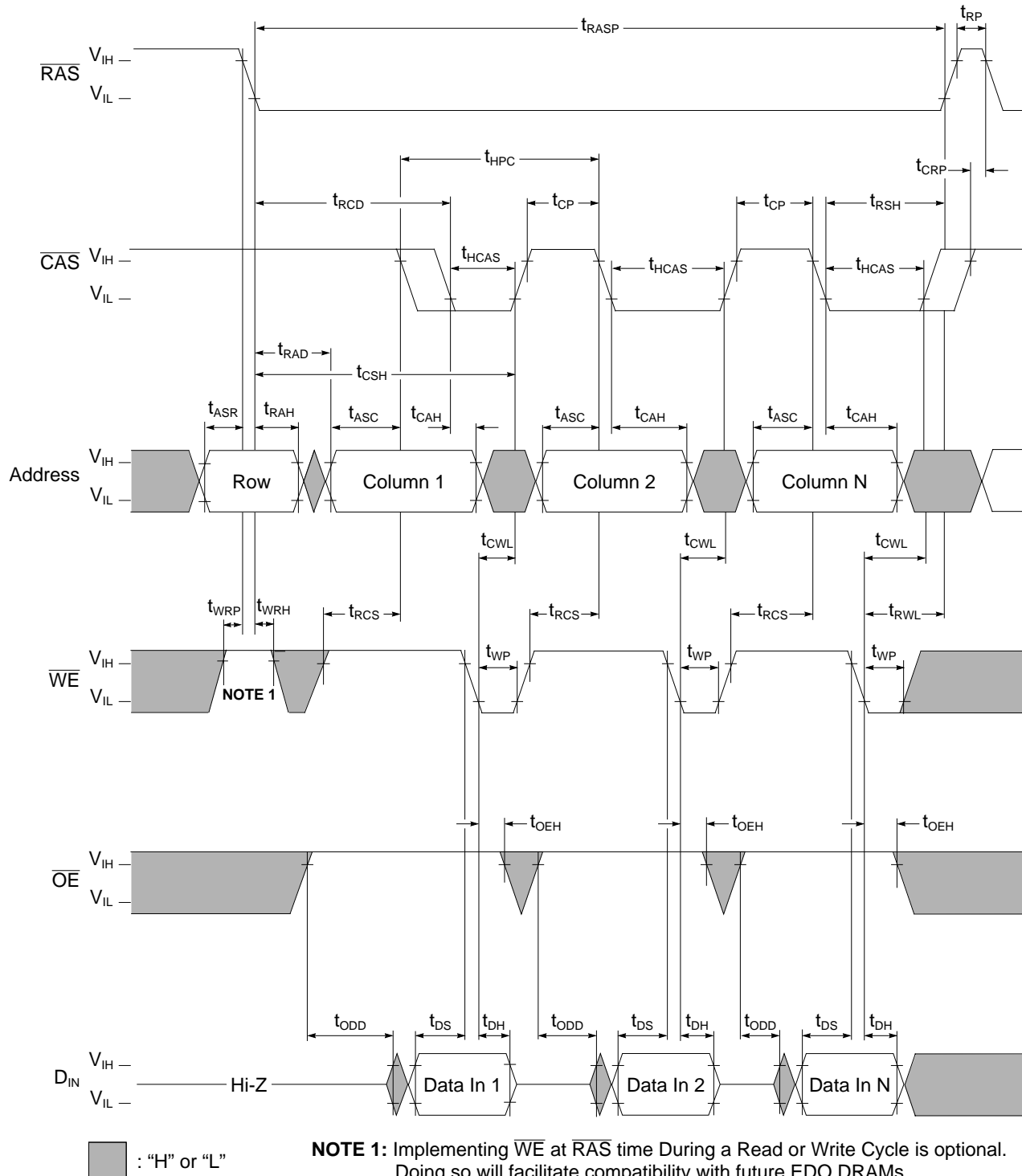






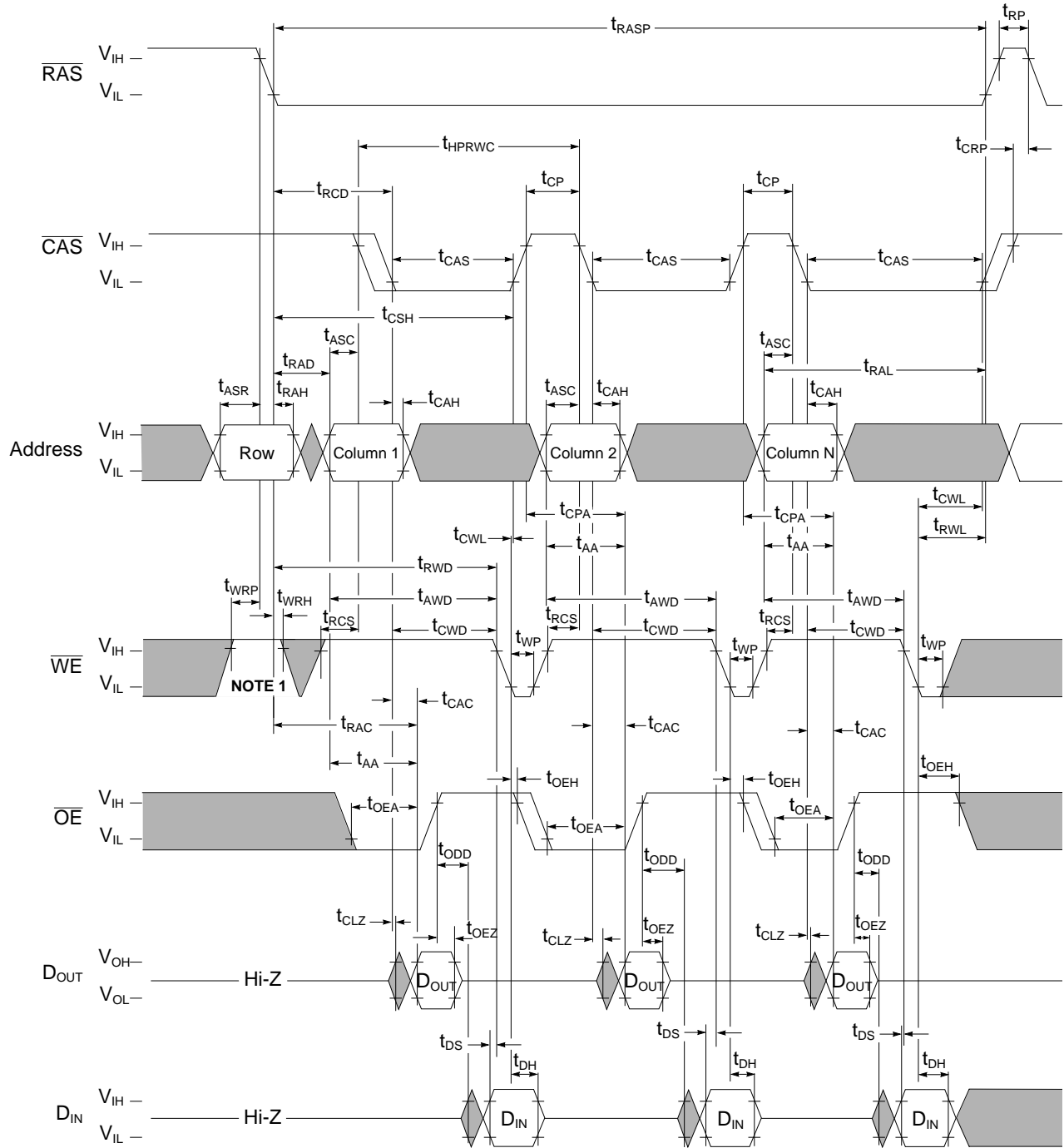
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### EDO Page Mode Late Write Cycle





### EDO Page Mode Read Modify Write Cycle



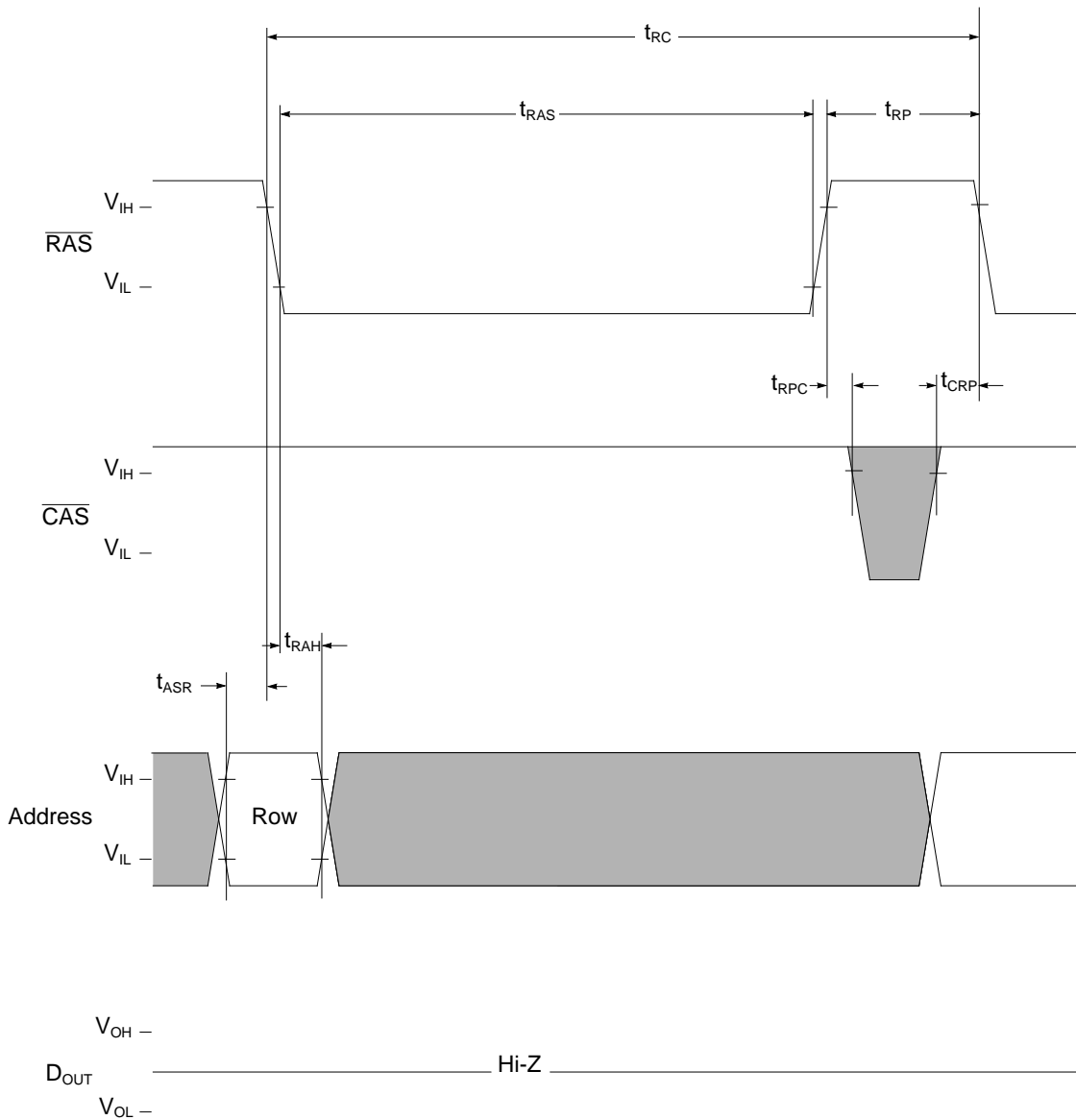
■ : "H" or "L"


**NOTE 1:** Implementing  $\overline{WE}$  at  $\overline{RAS}$  time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.



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### RAS Only Refresh Cycle



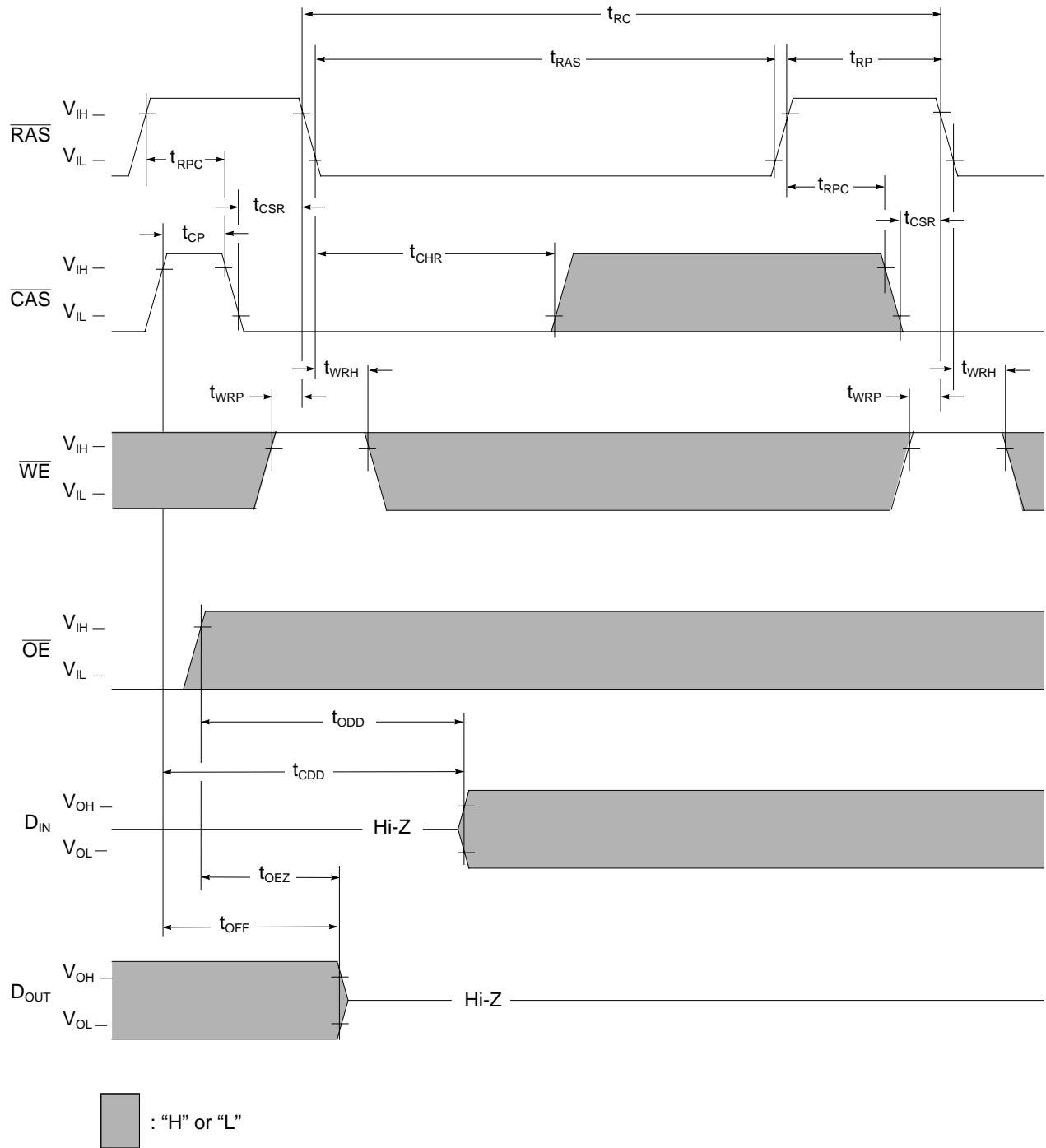
 : "H" or "L"

Note:  $\overline{WE}$ ,  $\overline{OE}$ ,  $D_{IN}$  are "H" or "L"





CAS Before RAS Refresh Cycle

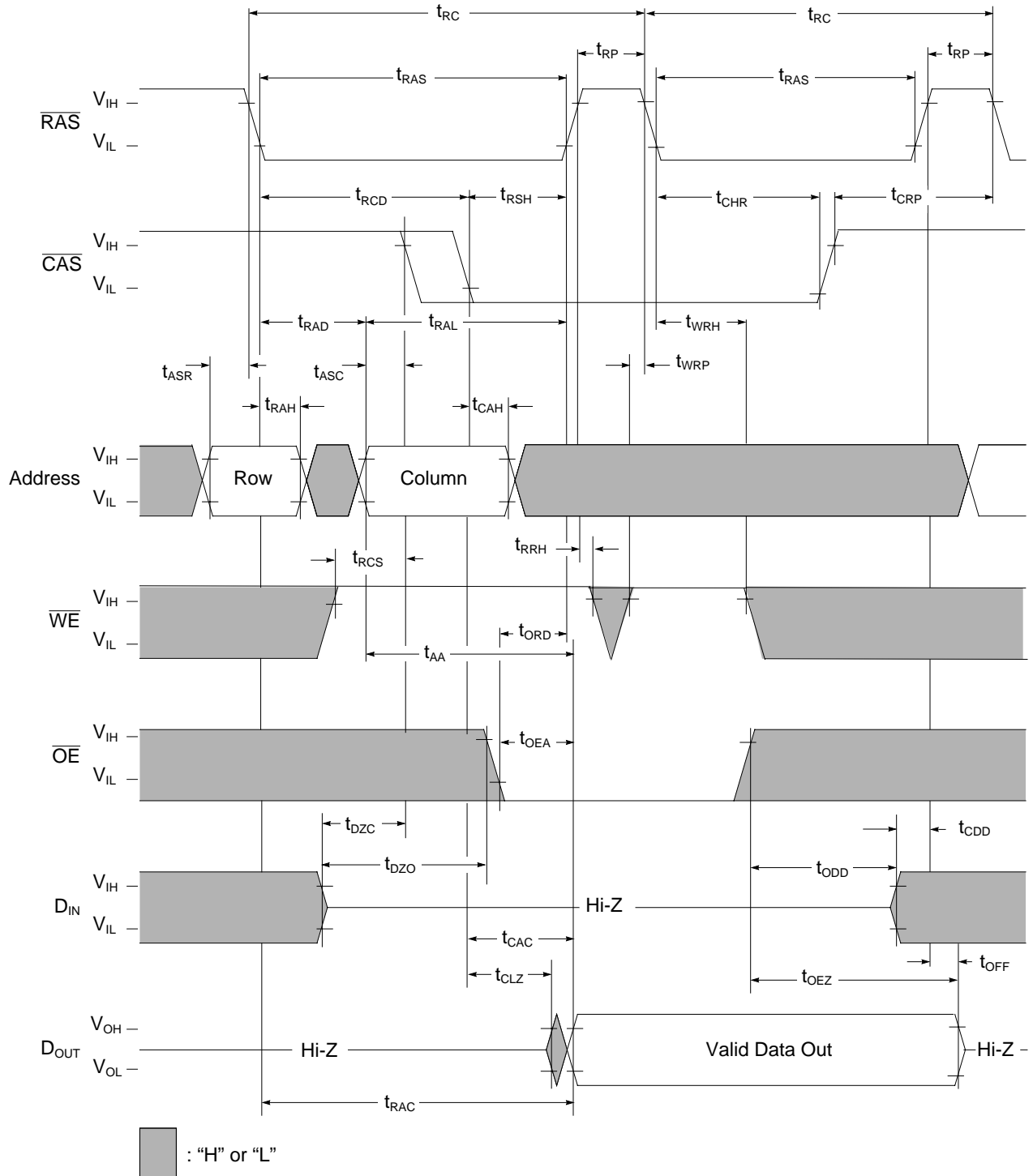


NOTE: Address is "H" or "L"



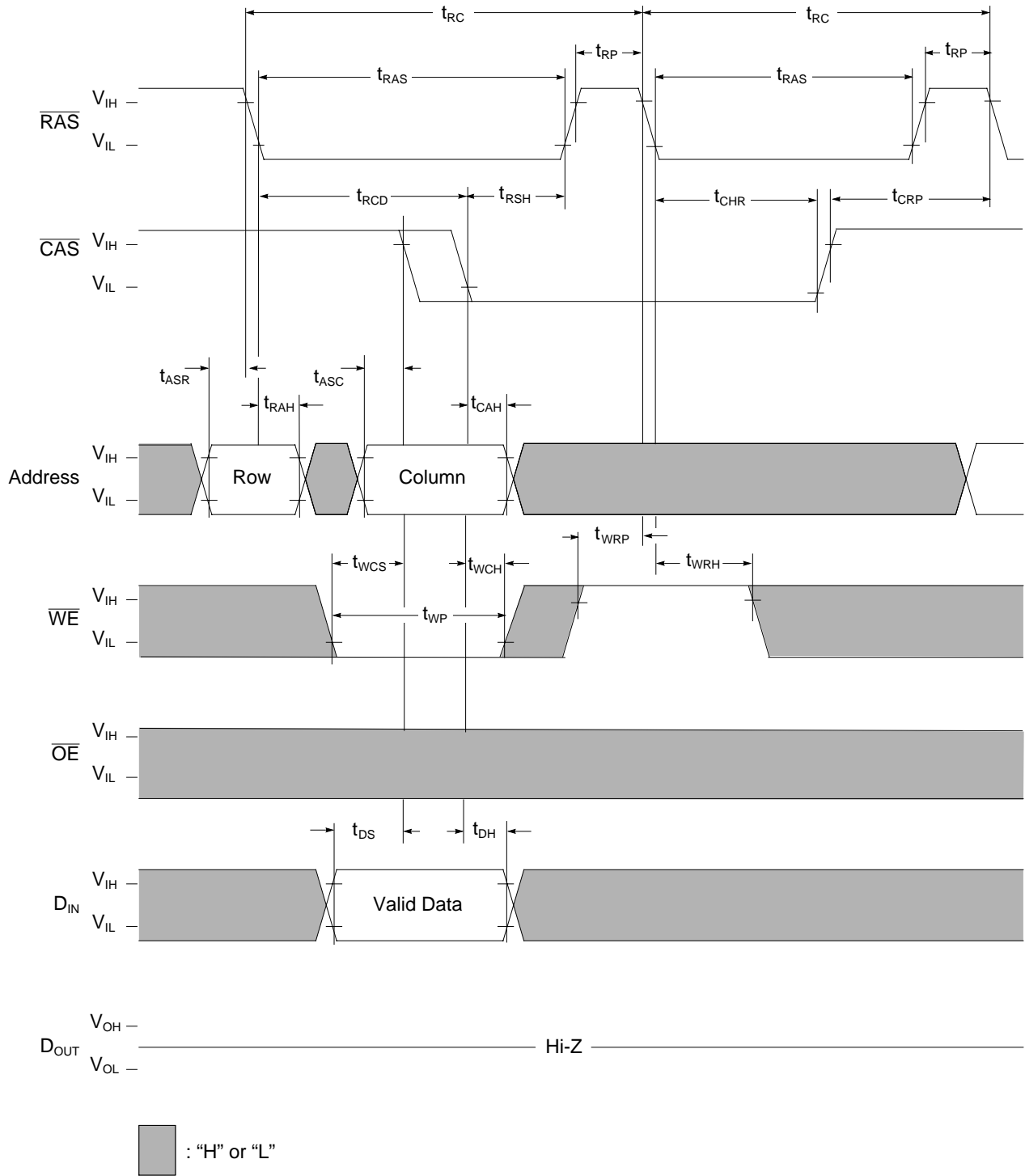
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### Hidden Refresh Cycle (Read)





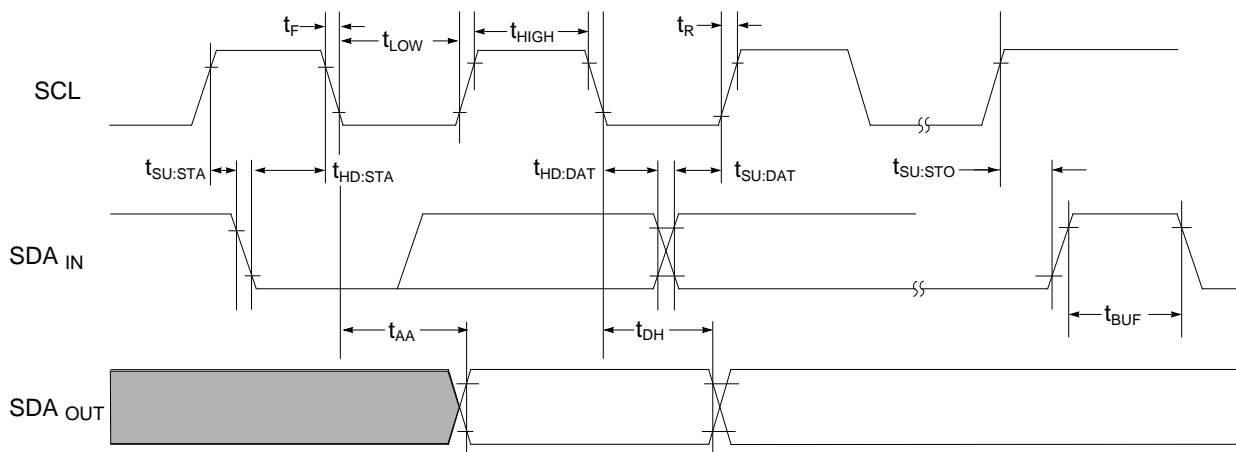
### Hidden Refresh Cycle (Write)





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## Presence Detect (EEPROM) Bus Timing



## Presence Detect Operation

**Clock and Data Conventions:** Data states on the SDA line can change only during SCL low. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 1 & Figure 2).

**Start Condition:** All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is high. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

**Stop Condition:** All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the serial PD device into standby power mode.

**Acknowledge:** Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, The PD device, will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an

acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 1. Data Window

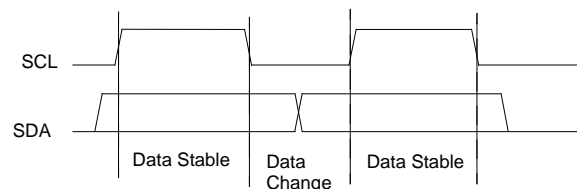


Figure 2. Definition of Start & Stop

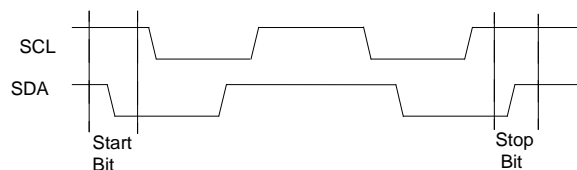
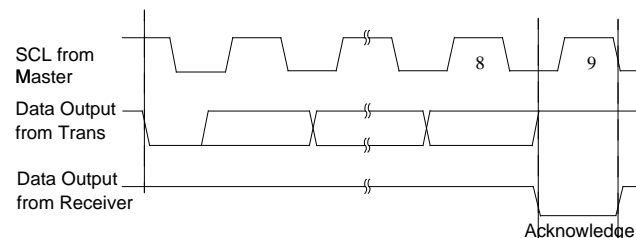
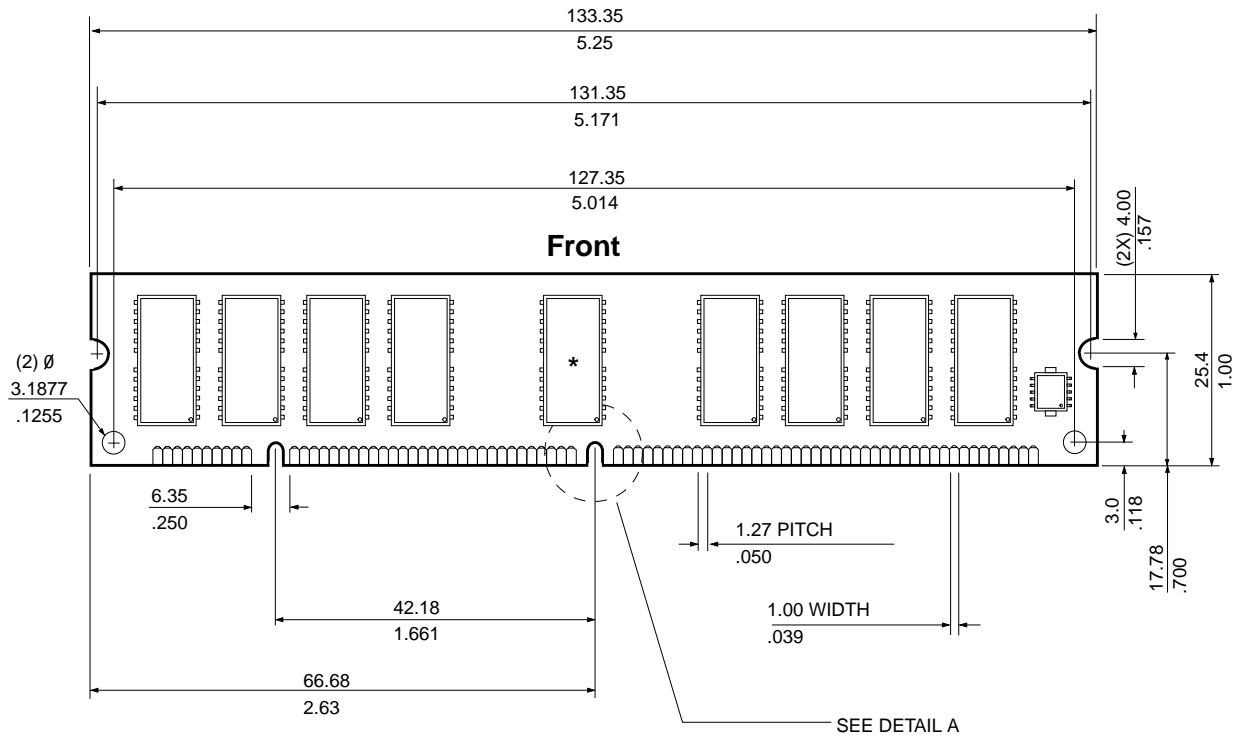


Figure 3. Acknowledge Response From Receiver

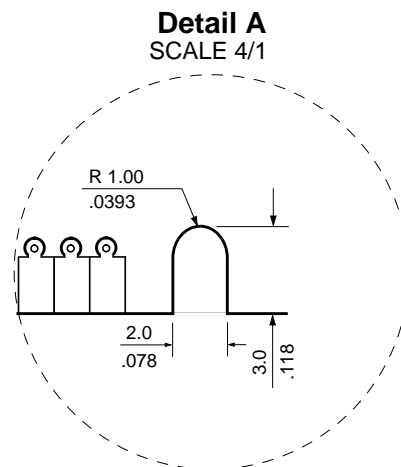
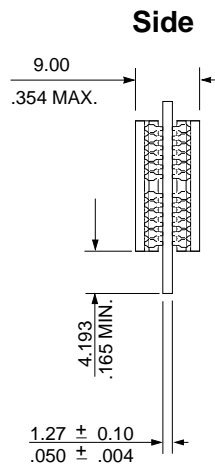




Layout Drawing



\* On x72 only (CBx)



**Note:** All dimensions are typical unless otherwise stated.  $\frac{\text{Millimeters}}{\text{Inches}}$



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## Revision Log

Rev	Contents of Modification
1/96	Initial Release.
3/96	Added 11/11 addressing Updated capacitance Updated $I_{I(L)}$ , $I_{OUT}$ Improved timings $t_{CAH}$ , $t_{CDD}$ , $t_{OEZ}$ , $t_{OFF}$ , PD timings Increased $t_{OEZ}$ timing Updated EDO timing diagrams CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. Hidden Refresh Cycle (Read) timing diagram was changed to show data being turned off with $\overline{RAS}$ not $\overline{CAS}$
5/96	Updated ordering information Added bytes 13 and 14 to Serial Presence Detect table
12/96	Updated Serial Presence Detect table
6/97	Updated Serial Presence Detect table, added 50ns part
5/98	Eliminate 70ns speed sort, and added 50ns

**Discontinued (9/98 - last order; 3/99 last ship)**



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