Precision Wide Bandwidth Analog Switches

Features

- Single-Supply Operation (+2V to +6V)
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (6Ω typ with 5V supply) Minimizes Distortion and Error Voltages
- R_{ON} Matching Between Channels, 0.8 Ω typ
- On-Resistance Flatness, 3Ω typ
- Low Charge Injection Reduces Glitch Errors. Q=4pC typ
- High Speed. t_{ON}, 10ns typ
- Very Good Off-Isolation: -55dB @ 30 MHz
- Wide -3dB Bandwidth: 200 MHz
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (0.5µW typ)
- Pin-compatible with DG40X, MAX38X

Applications

- Audio, Video Switching and Routing
- Battery-Powered Communication Systems
- Computer Peripherals
- Telecommunications
- Portable Instrumentation
- Replaces Mechanical Relays

Description

The PI5A381/383/385A are dual monolithic analog switches designed for single-supply operation. These high-precision devices are ideal for low-distortion audio, video, signal switching and routing.

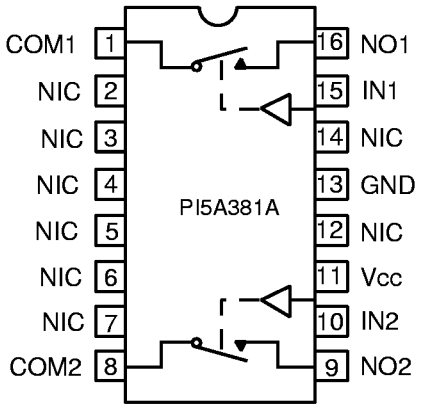
The PI5A381 is a dual single-pole single-throw (SPST), normally open (NO) switch. The PI5A383 is a dual single-pole double-throw (SPDT) switch. The PI5A385 is a dual double-pole single-throw (DPST), normally open (NO) function.

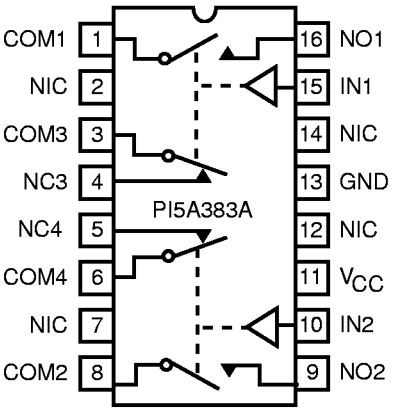
Each switch conducts current equally well in either direction when on. When off they block voltages up to the power-supply rails.

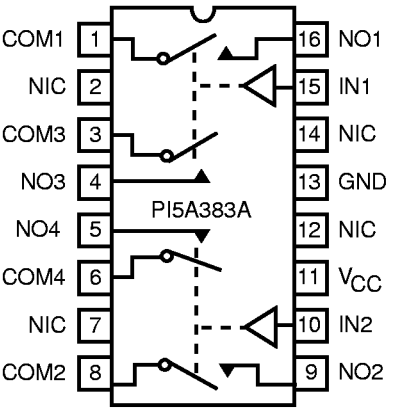
The PI5A381/383/385 are fully specified with +5V, and +3.3V supplies. With +5V, they guarantee <12Ω on-resistance. On-resistance matching between channels is within 2Ω. On-resistance flatness is less than 5Ω over the full signal range. The PI5A38X family guarantees fast switching speeds (t_{ON} < 20ns).

These products are available in the 16-pin narrow-body SOIC, QSOP, and PDIP packages for operation over the industrial (-40°C to +85°C) temperature range.

Functional Diagram, Pin Configurations and Truth Tables







Switches shown for Logic "0" input
NC = Normally Closed, NO = Normally Open, NIC = Not internally Connected

PI5A381A	
Logic	**Switch**
0	OFF
1	ON

PI5A383A		
Logic	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

PI5A385A	
Logic	**Switch**
0	OFF
1	ON

Absolute Maximum Ratings

Voltages Referenced to GND

V_{CC} .....–0.5V to +7V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... –0.5V to V_{CC} +2V

. or 30mA, whichever occurs first

Current (any terminal except COM, NO, NC) 30mA

Current, COM, NO, NC 100mA

(pulsed at 1ms, 10% duty cycle) 120mA

Thermal Information

Continuous Power Dissipation

PDIP (derate 10.5mW/°C above 70°C) 800mW

Narrow SO & QSOP

(derate 8.7mW/°C above +70°C) 650mW

Storage Temperature ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Characteristics-Single 5.0V Supply

(V_{CC} = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Test Conditions	Temp(°C)	Min(2)	Typ(2)	Max(2)	Unit
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V_{CC}	V
ON-Resistance	R_{ON}	V_{CC} = 4.5V, I_{COM} = 30mA V_{NO} or V_{NC} = +2.5V	25		6	10	Ω
			Full			12	
On-Resistance Match Between Channels(4)	ΔR_{ON}		25		0.4		
			Full			2	
On-ResistanceFlatness(5)	$R_{FLAT(ON)}$	V_{CC} = 5V, I_{COM} = -30mA V_{NO} or V_{NC} = 1V, 2.5V, 4V	25		3	4	
			Full			5	
NO or NCOff LeakageCurrent(6)	$I_{NO(OFF)}$ $I_{NC(OFF)}$	V_{CC} = 5.5V, V_{COM} = 0V V_{NO} or V_{NC} = 4.5V	25		0.07		nA
			Full	-80		80	
COMOff Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = +4.5V V_{NO} or V_{NC} = ±0V	25		0.07		
			Full	-80		80	
COMOn Leakage Current(6)	$I_{COM(ON)}$	V_{CC} = 5.5V, V_{COM} = +4.5V V_{NO} or V_{NC} = +4.5V	25		0.07		
			Full	-80		80	

Electrical Characteristics-Single 5.0V Supply (continued)

(V_{CC} = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Unit
Logic Input							
Input High Voltage	V_{INH}	Guaranteed logic High Level	Full	2			V
Input Low Voltage	V_{INL}	Guaranteed logic Low Level				0.8	
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-1	0.005	1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On Time	t_{ON}	V_{CC} = 5V, Figure 1	25		10	15	ns
			Full			20	
Turn-Off Time	t_{OFF}		25		5	8	
			Full			10	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω Figure 2	25		4	6	pC
Off Isolation	OIRR	R_L = 100Ω, C_L = 5pF, f = 30MHz, Figure 3			-55		dB
Crosstalk(8)	$I_{COM(OFF)}$	R_L = 100Ω, C_L = 5pF, f = 30MHz, Figure 4			-72		
NC or NO Capacitance	$C_{(OFF)}$	f = 1kHz, Figure 5			13		pF
COM Off Capacitance	$C_{COM(OFF)}$				15		
COM On Capacitance	$C_{COM(ON)}$	f = 1kHz, Figure 6			35		
-3dB Bandwidth	BW	R_L = 50Ω, Figure 7	Full		200		MHz
Distortion(9)	D	R_L = 10kΩ			0.03		%
Supply							
Power-Supply Range	V_{CC}		Full	2		6	V
Positive Supply Current	I_{CC}	V_{CC} = 5.5V, V_{IN} = 0V or V_{CC}, all channels on or off				1	µA

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Off Isolation = $20\log_{10} [V_{COM}/ (V_{NO}$ or $V_{NC})]$. See figure 3.
8. Between any two stitches. See figure 4.
9. $D = R_{FLAT(ON)}/RL$

Electrical Specifications - Single +3.3V Supply

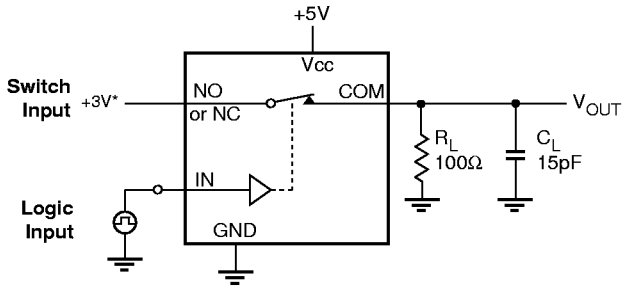
(V_{CC} = +3.3V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

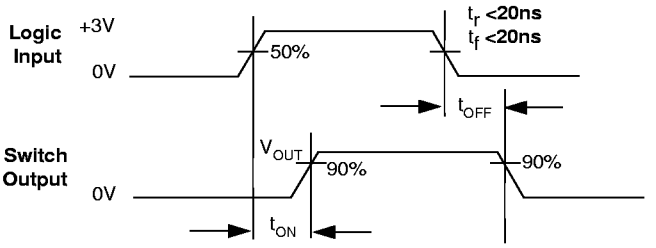
Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 3V, I_{COM} = -30mA, V_{NO} or V_{NC} = 1.5V	25		15	18	Ω
			Full			22	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{CC} = 3.3V, I_{COM} = -30mA, V_{NO} or V_{NC} = 0.8V, 2.5V	25		0.4	1	
			Full			2	
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$		25		6	10	
			Full			12	
Dynamic							
Turn-On Time	t_{ON}	V_{CC} = 3.3V, V_{NO} or V_{NC} = 1.5V Figure 1	25		10		ns
			Full			20	
Turn-Off Time	t_{OFF}		25		5		
			Full			10	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		3	5	pC
Supply							
Positive Supply Current	I_{CC}	Vcc = 3.6V, V_{IN} = 0V or Vcc, all channels on or off	Full			1	µA

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}max - R_{ON}min$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.

Test Circuits/Timing Diagrams



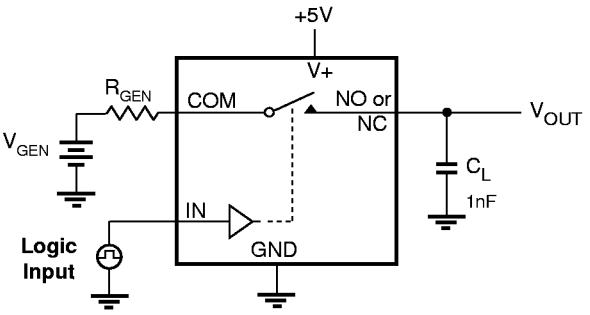


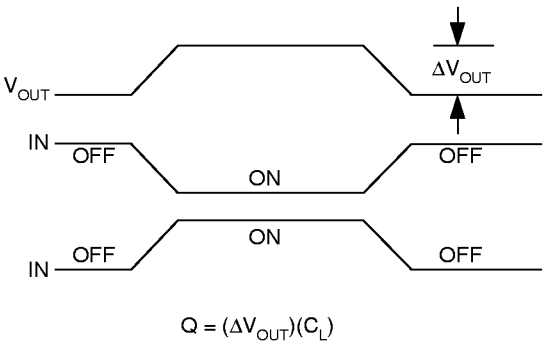
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time





$$Q = (\Delta V_{OUT})(C_L)$$

Figure 2. Charge Injection

Test Circuits/Timing Diagrams (continued)

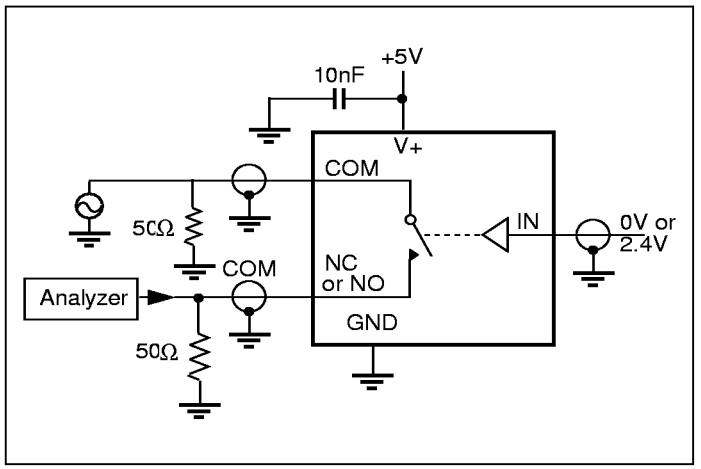


Figure 3. Off Isolation

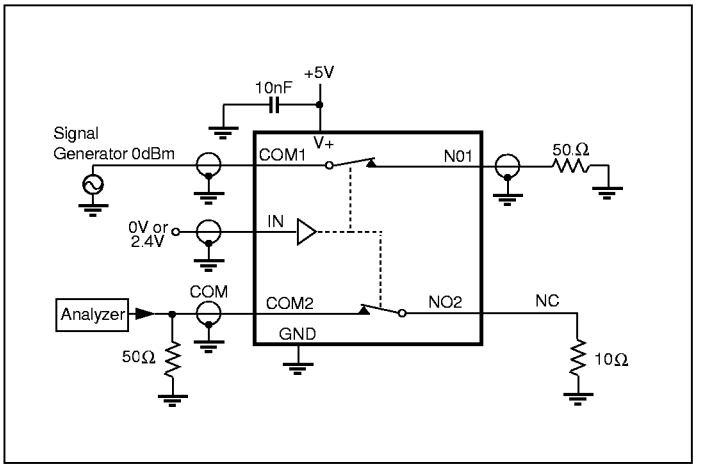


Figure 4. Crosstalk

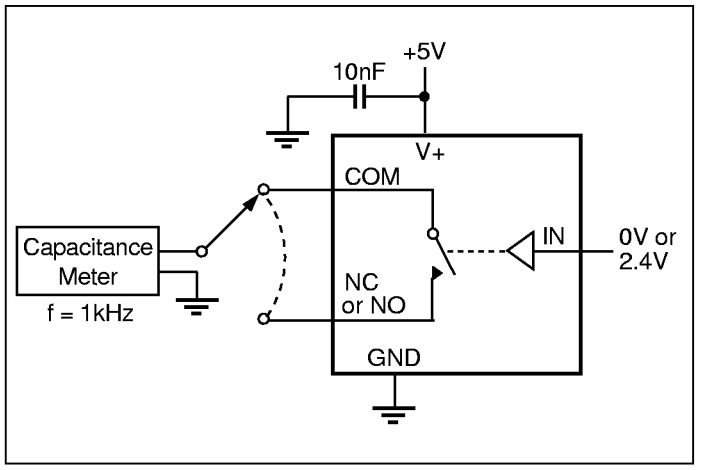


Figure 5. Channel-Off Capacitance

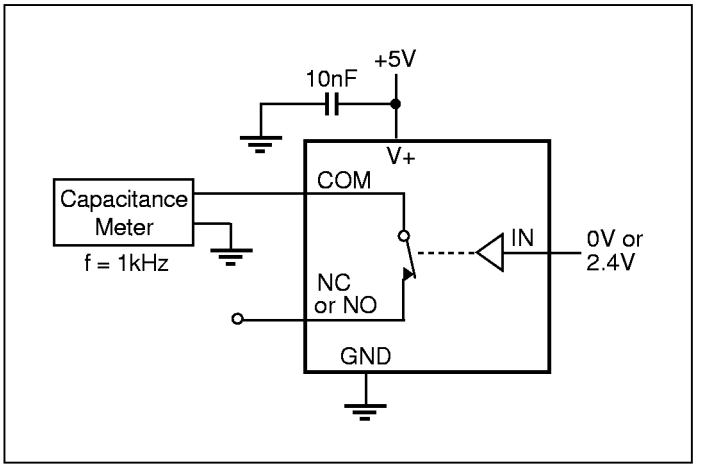


Figure 6. Channel-On Capacitance

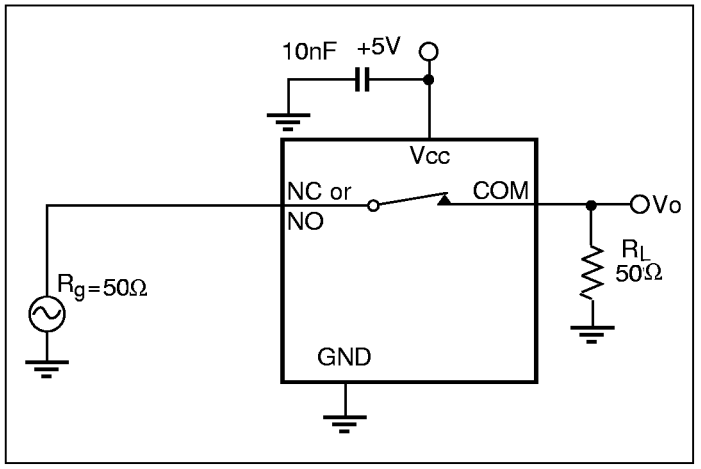
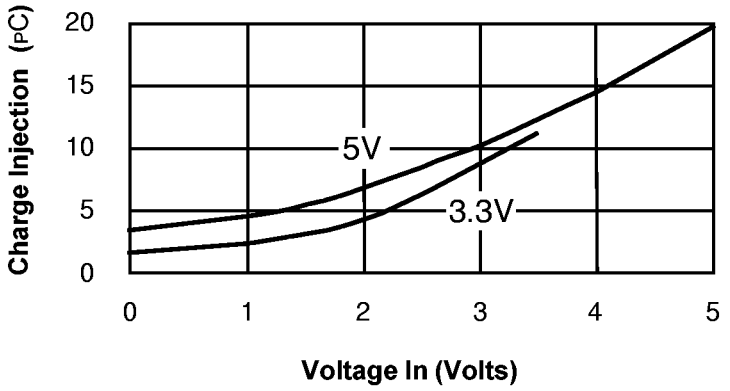


Figure 7. Bandwidth

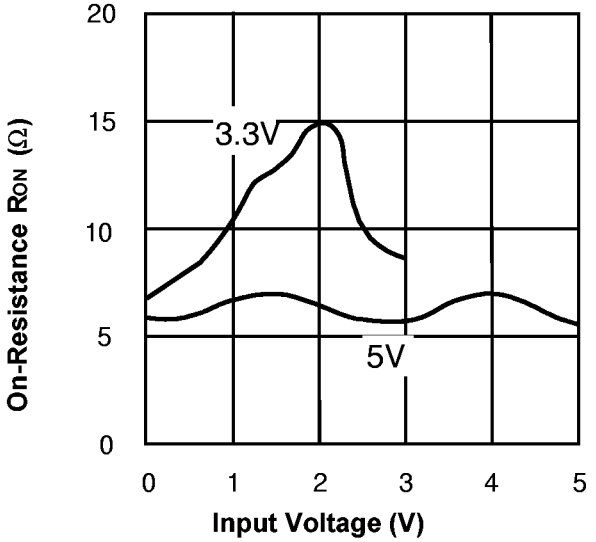
Charge Injection vs Voltage In

V_{CC} = +5V, 3.3V
T_A = 25°C
CL = 1nF



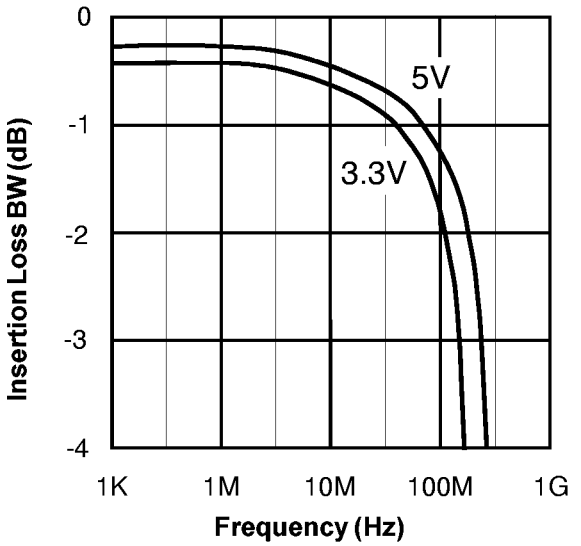
On-Resistance vs Input Voltage

R_H = 100Ω
T_A = 25°C

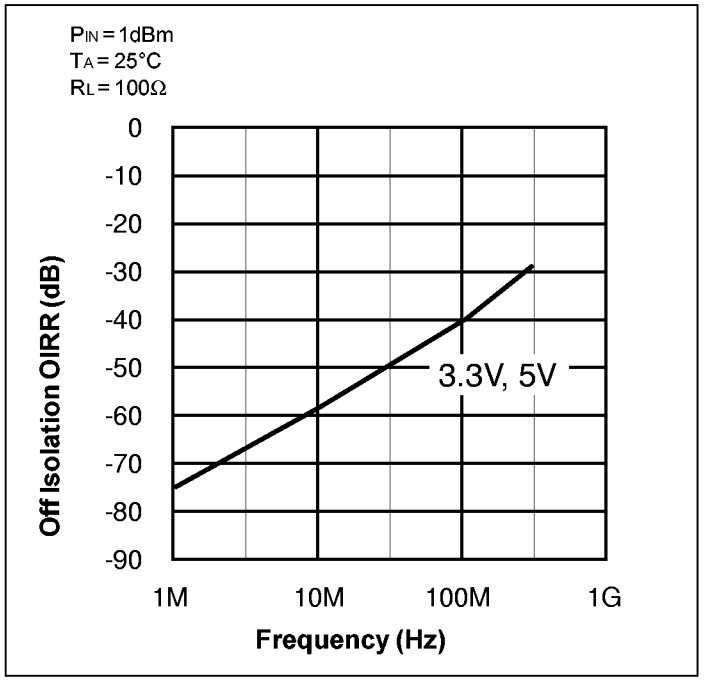


Insertion Loss vs Frequency

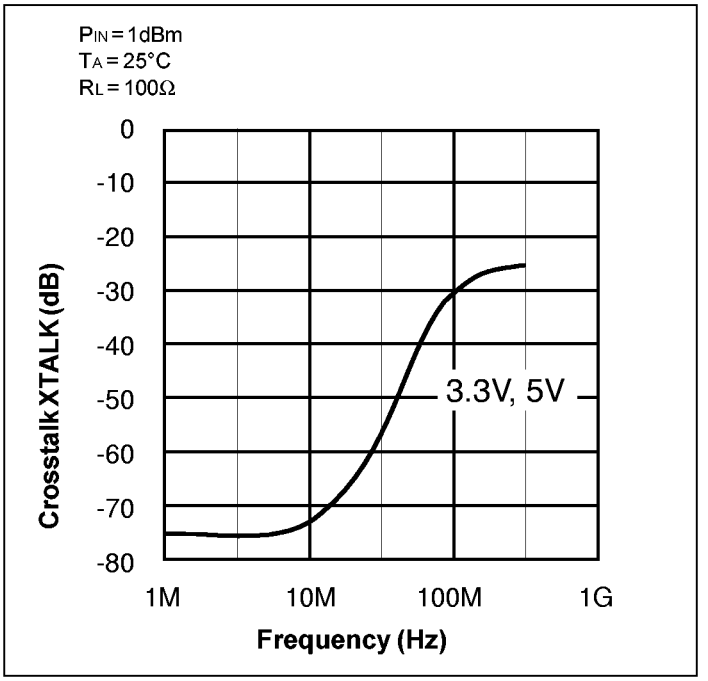
R_{IN} = 1dBm
R_L = 100Ω
T_A = 25°C



Off Isolation vs Frequency



Crosstalk vs Frequency

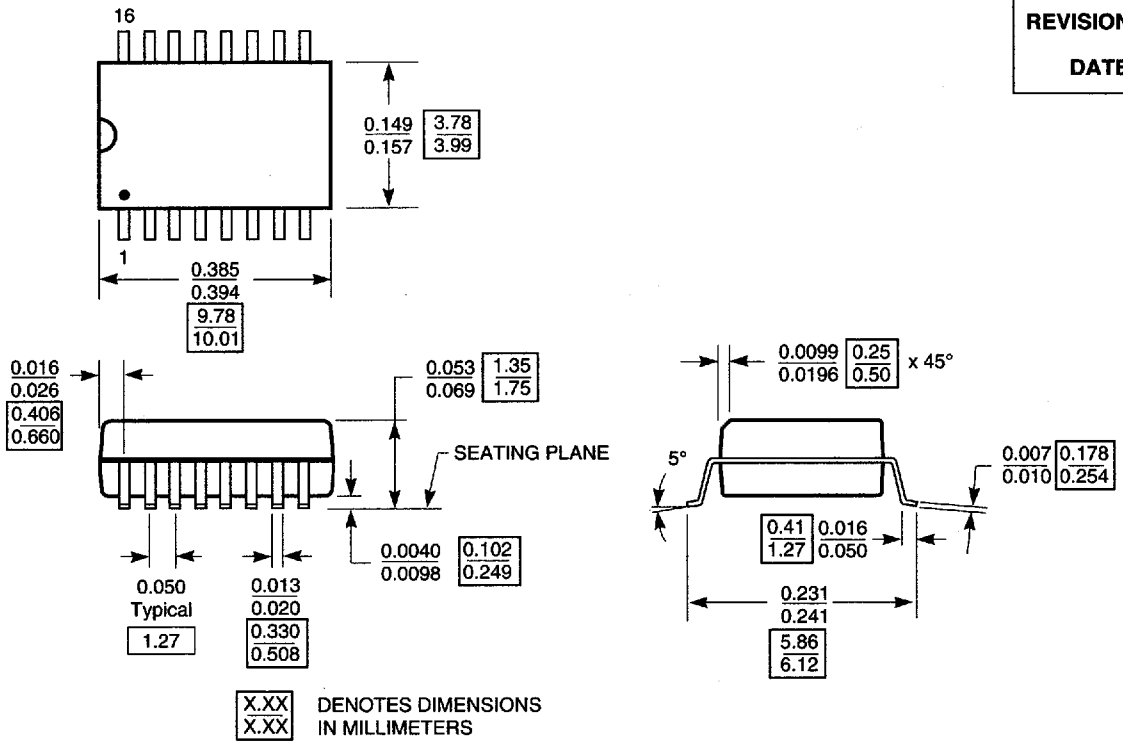


Ordering Information

P/N	Package
PI5A381AP	16 Pin PDIP
PI5A381AW	Narrow Body SOIC-16
PI5A381AQ	16 Pin QSOP
PI5A383AP	16 Pin PDIP
PI5A383AW	Narrow Body SOIC-16

P/N	Package
PI5A383AQ	16 Pin QSOP
PI5A385AP	16 Pin PDIP
PI5A385AW	Narrow Body SOIC-16
PI5A385AQ	16 Pin QSOP

DOCUMENT CONTROL NO.
PD- 1004
REVISION:
DATE: 11/13/95



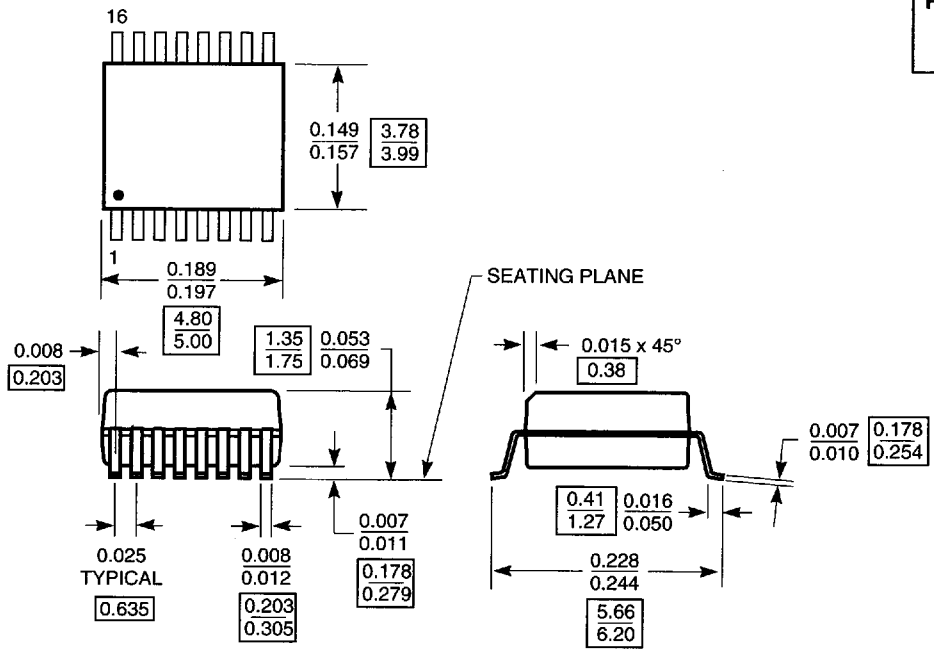
PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive • San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100

DESCRIPTION: 16-PIN SOIC (150 MIL WIDE)

PACKAGE CODE: W16

PACKAGE MECHANICAL DIMENSIONS

DOCUMENT CONTROL NO.
PD- 1201
REVISION:
DATE: 11/13/95



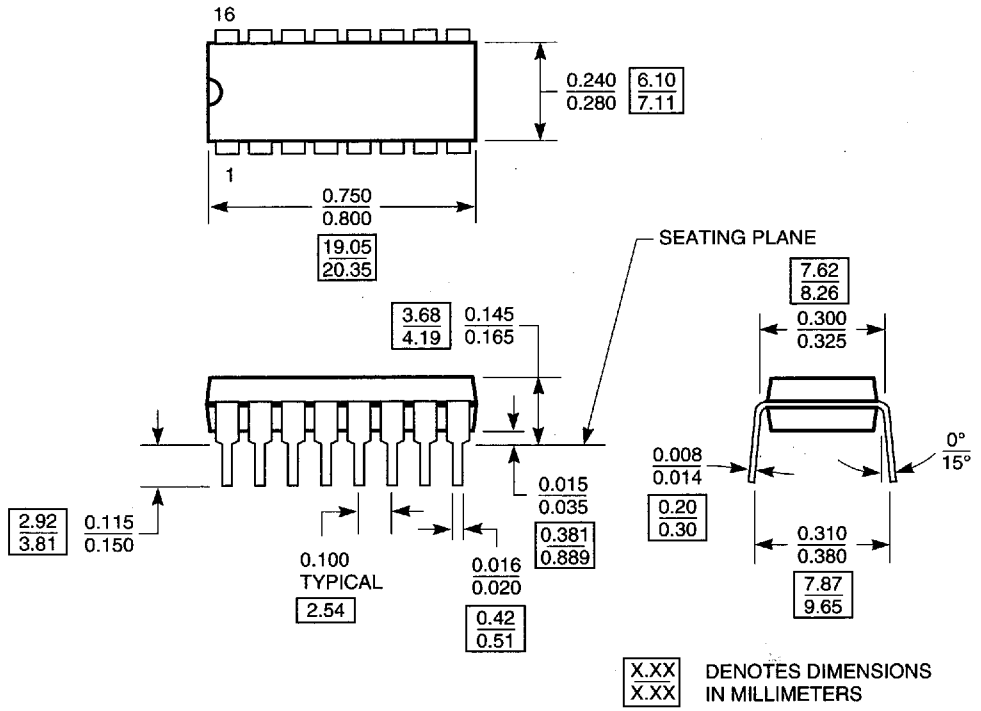
X.XX
X.XX DENOTES DIMENSIONS IN MILLIMETERS

PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive • San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100

DESCRIPTION:	16-PIN QSOP (150 MIL WIDE)
PACKAGE CODE:	Q16

PACKAGE MECHANICAL DIMENSIONS

DOCUMENT CONTROL NO.
PD- 1703
REVISION:
DATE: 11/13/95



PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive • San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100

DESCRIPTION:	16-PIN PLASTIC DIP (300 MIL WIDE)
PACKAGE CODE:	P16

PACKAGE MECHANICAL DIMENSIONS