

Product Features

- Ideal for address line driving and clock distribution
- Eight banks with 1:4 fanout with 3-state control
- Typical $t_{SK(O)}$ output skew < 500ps
- Balanced output drivers: $\pm 24\text{mA}$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240-mil wide plastic TSSOP (A)
 - 56-pin 300-mil wide plastic SSOP (V)

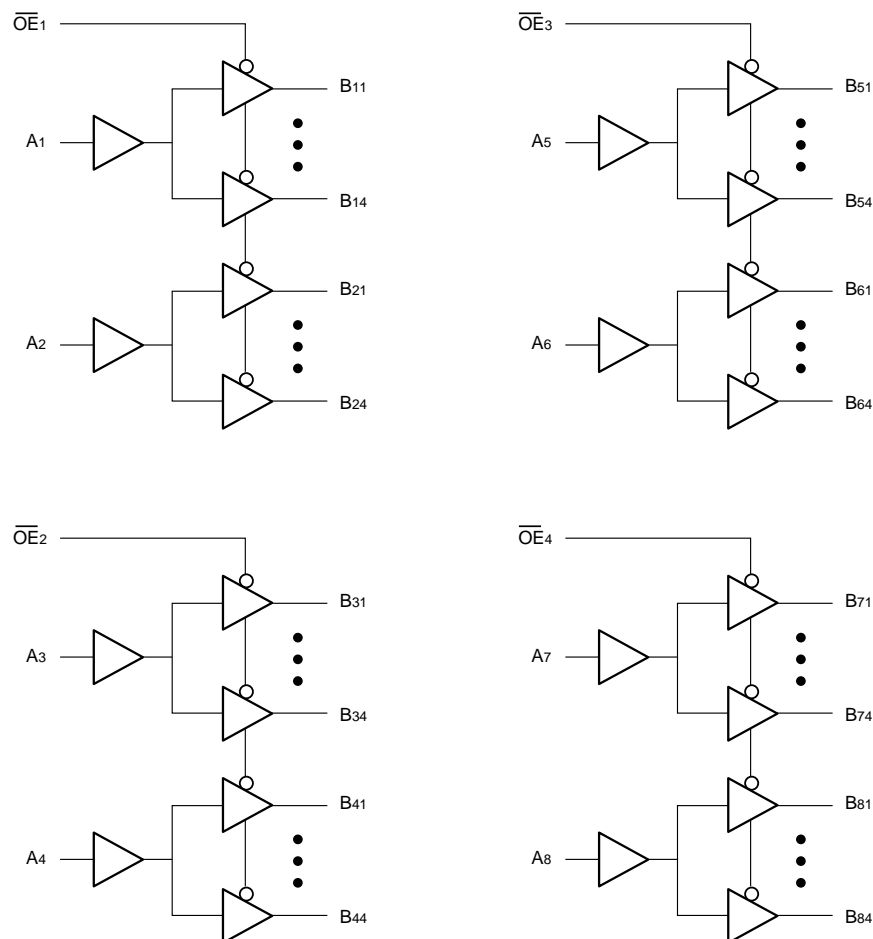
Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

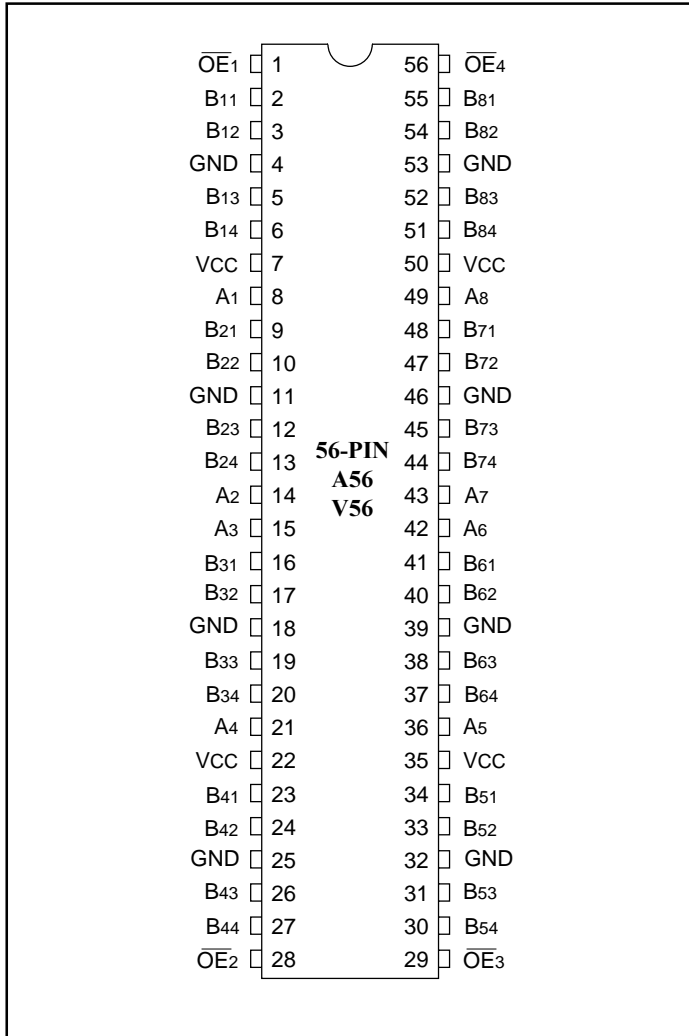
The PI74FCT162344T is an address/clock driver designed to provide the ability to fanout to memory arrays. Eight banks, each with a fanout of four, and 3-state control, provide efficient address distribution. One or more banks may be used for clock distribution.

The PI74FCT162344T has balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
OE _x	3-State Output Enable Inputs (Active LOW)
A _x	Inputs
B _{xx}	3-State Outputs
GND	Ground
VCC	Power

Truth Table⁽¹⁾

Inputs		Outputs
OE _x	A _x	B _{xx}
L	L	L
L	H	H
H	X	Z

Note: 1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8.0	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	–60 to +120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Ambient Temperature = –40°C to +85°C
V_{CC} = 5.0V ±10%

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = –24mA	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	—	0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC} (Input Pins)	—	—	±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND (Input & I/O Pins)	—	—	±1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V	—	—	±1	μA
I _{OZL}	Output Current	(3-State Output Pins)	V _{OUT} = 0.5V	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18mA		—	–0.7	–1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		–60	–115	–150	mA
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _{OUT} = GND ⁽⁴⁾		–80	–140	–225	mA
I _{OUT}	Output Drive Current	V _{CC} = Max., V _{OUT} = 2.5V ⁽³⁾		–50	—	–180	mA
V _H	Input Hysteresis			—	100	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. This parameter is determined by device characterization but is not production tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4 V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open O _{EX} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		170	220	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle O _{EX} = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	2.7 ⁽⁵⁾	mA
			V _{IN} = 3.4 V V _{IN} = GND		2.0	3.5 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle O _{EX} = GND 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND		3.4	4.9 ⁽⁵⁾	
			V _{IN} = 3.4 V V _{IN} = GND		5.4	10.9 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0 V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

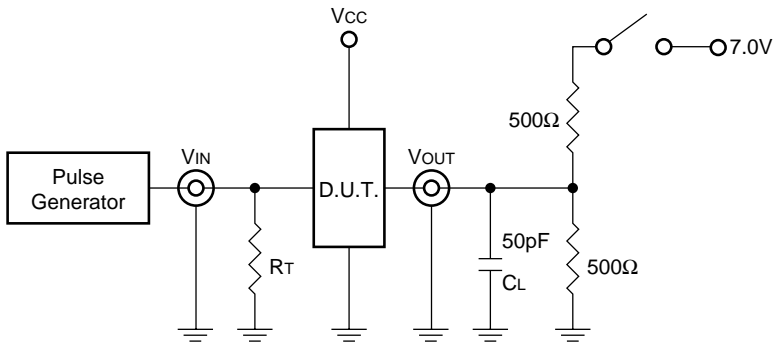
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162344AT		162344CT		162344ET		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Ax to Bx	CL = 50pF RL = 500Ω	1.5	4.8	1.5	4.3	1.5	3.8	ns
tpZH tpZL	Output Enable Time OEx to Bx		1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time OEx to Bx		1.5	5.6	1.5	5.2	1.5	4.6	ns
tsk1(o) ^(3,5)	Output Skew		—	0.5	—	0.35	—	0.25	ns
tsk2(o) ^(4,5)	Output Skew		—	0.5	—	0.5	—	0.3	ns

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between outputs of the same bank and same package, switching in the same transition.
4. Skew between outputs of all banks of the same package with A1 through A8 tied together, switching in the same transition.
5. This parameter is guaranteed but not production tested.

Tests Circuits For All Outputs⁽¹⁾



Switch Position

Test	Switch
Disable LOW Enable LOW	7V
All Other Tests	Open

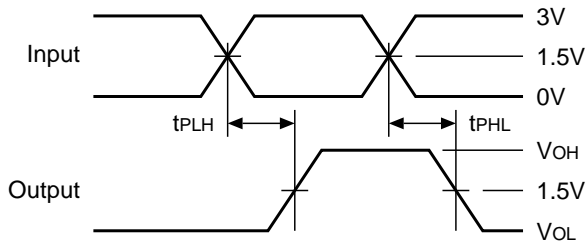
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

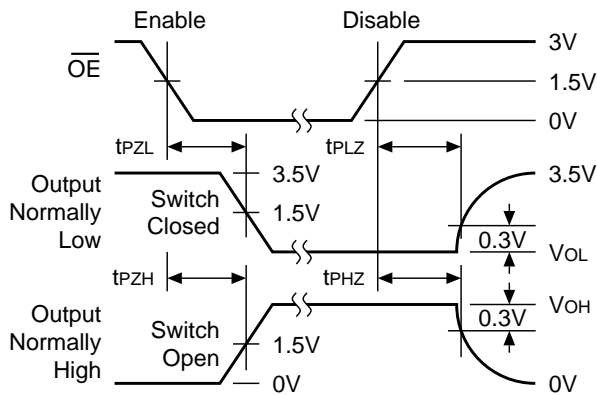
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SWITCHING WAVEFORMS

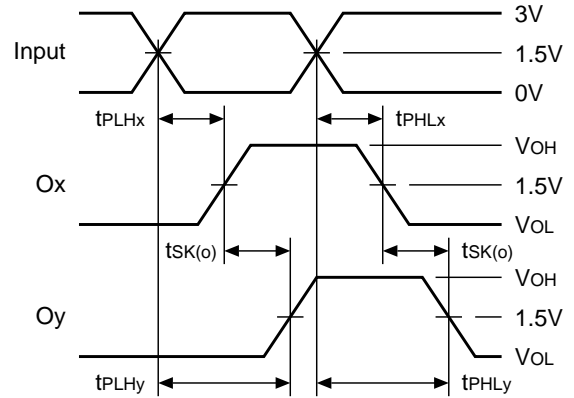
Propagation Delay



Enable and Disable Times



Output Skew – tsk1(o), tsk2(o)



$$t_{SK(o)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Note:

t_{SK1(o)} = Ox and Oy are in the same bank.

t_{SK21(o)} = Ox and Oy are in a different bank on the same port.