SUMMIT
MICROELECTRONICS, Inc.

SMS2902/SMS2904/SMS2916

Voltage Supervisory Circuit With Watchdog Timer
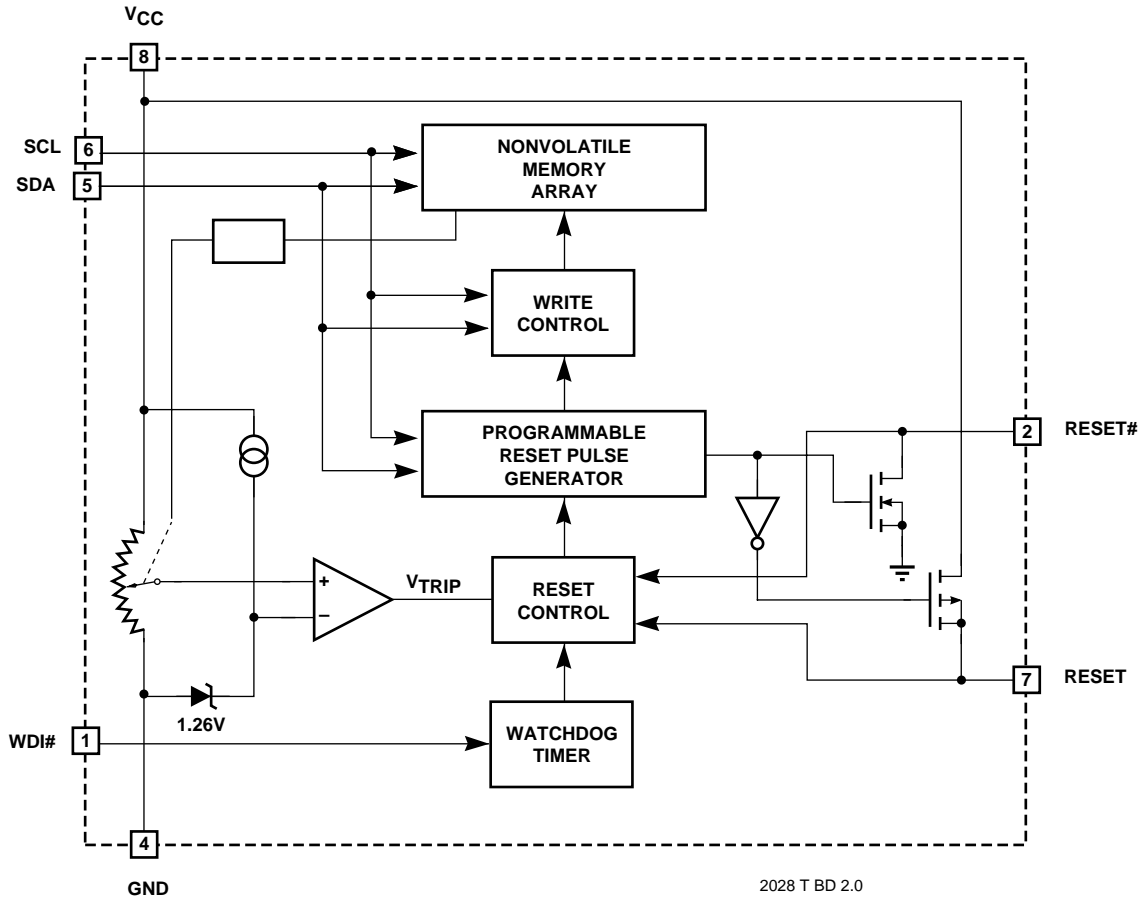
FEATURES

- **Precision Voltage Monitor**
  - **V_{CC} Supply Monitor**
    - **Complementary reset outputs for complex microcontroller systems**
    - **Integrated memory write lockout function**
    - **No external components required**
- **Watchdog Timer**
  - **1600 ms, internal**
- **Two Wire Serial Interface (I^2C™)**
- **Extended Programmable Functions available on SMS24**
- **High Reliability**
  - **Endurance: 100,000 erase/write cycles**
  - **Data retention: 100 years**
- **8-Pin SOIC Packages**

OVERVIEW

The SMS29xx is a power supervisory circuit that monitors V_{CC} and will generate complementary reset outputs. The reset pins also act as I/Os and may be used for signal conditioning. The SMS29xx also has an on-board watchdog timer.

The SMS29xx integrates a nonvolatile serial memory. It features the industry standard I^2C serial interface allowing quick implementation in an end-users' system.
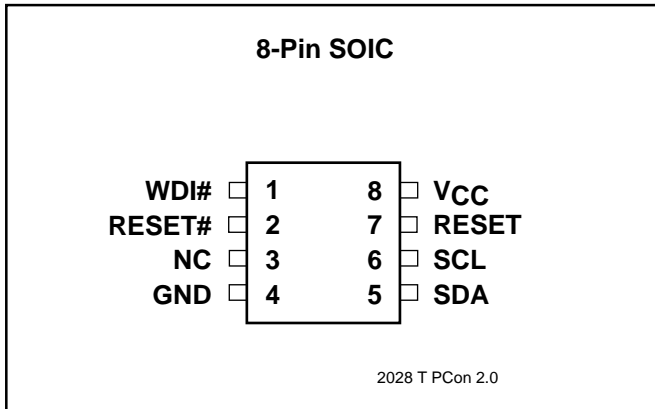
BLOCK DIAGRAM

2028 T BD 2.0

Characteristics subject to change without notice

PIN CONFIGURATIONS

8-Pin SOIC

WDI#	1	8	V_{CC}

WDI# □ 1   8 □ V$_{CC}$
RESET# □ 2   7 □ RESET
NC □ 3   6 □ SCL
GND □ 4   5 □ SDA

2028 T PCon 2.0

PIN NAMES

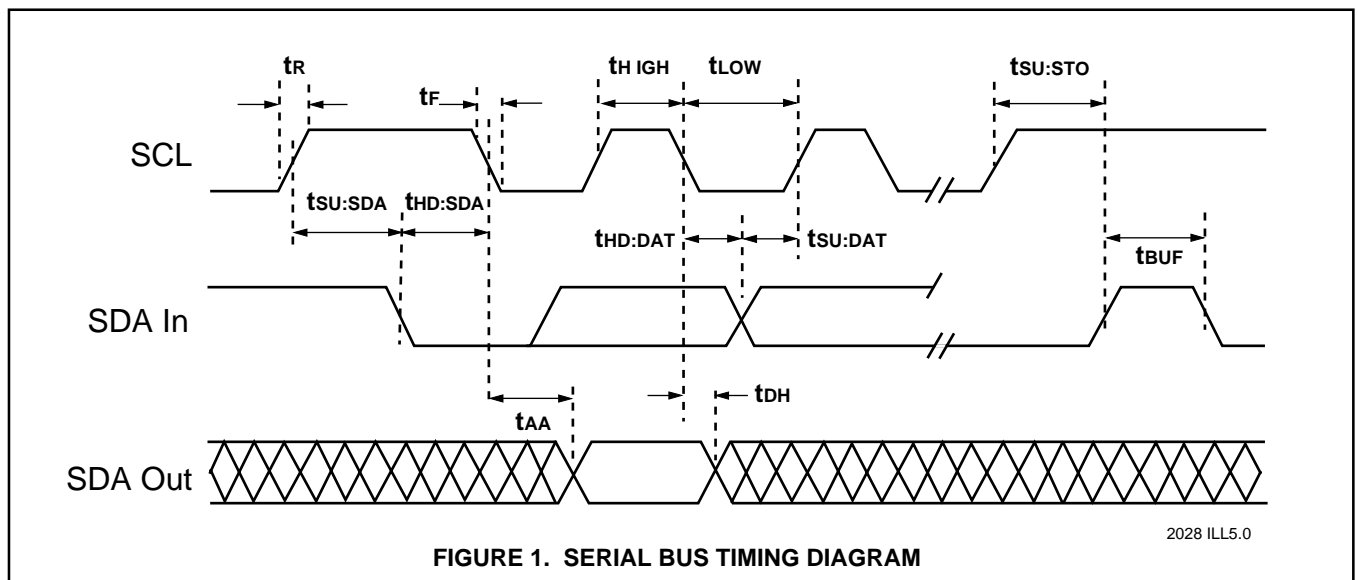| Symbol	Pin	Description
WDI#	1	Watchdog Input /a high to low transition will clear the watchdog timer
RESET#	2	Active Low RESET Input/Output
NC	3	No Connect, tie to ground or leave open
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/ Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/ Output
V$_{CC}$	8	Supply Voltage

2028 PGM T1.1

CAPACITANCE

$T_A = 25°C$, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
L_{OUT}	Output Capacitance	8	pF

2028 PGM T2..0

FIGURE 1. SERIAL BUS TIMING DIAGRAM

2028 ILL5.0

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... -40°C to +85°C
Storage Temperature .... -65°C to +125°C
Soldering Temperature (less than 10 seconds) .... 300°C
Supply Voltage .... 0 to 6.5V
Voltage on Any Pin .... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2028 PGM T3.0

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =3.3V		2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		50	µA
			V_{CC} =3.3V		25	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET#			0.3xV_{CC}	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA, RESET		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA SDA			0.4	V

2028 PGM T4.0

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

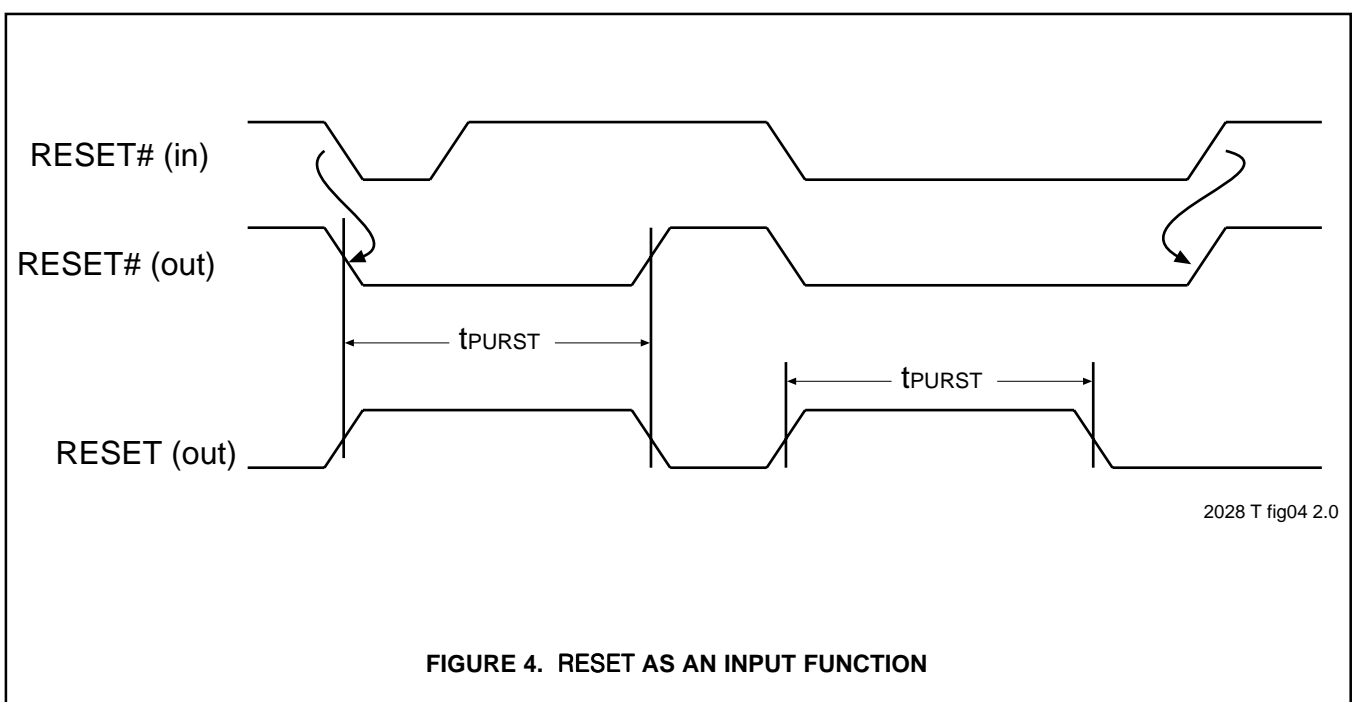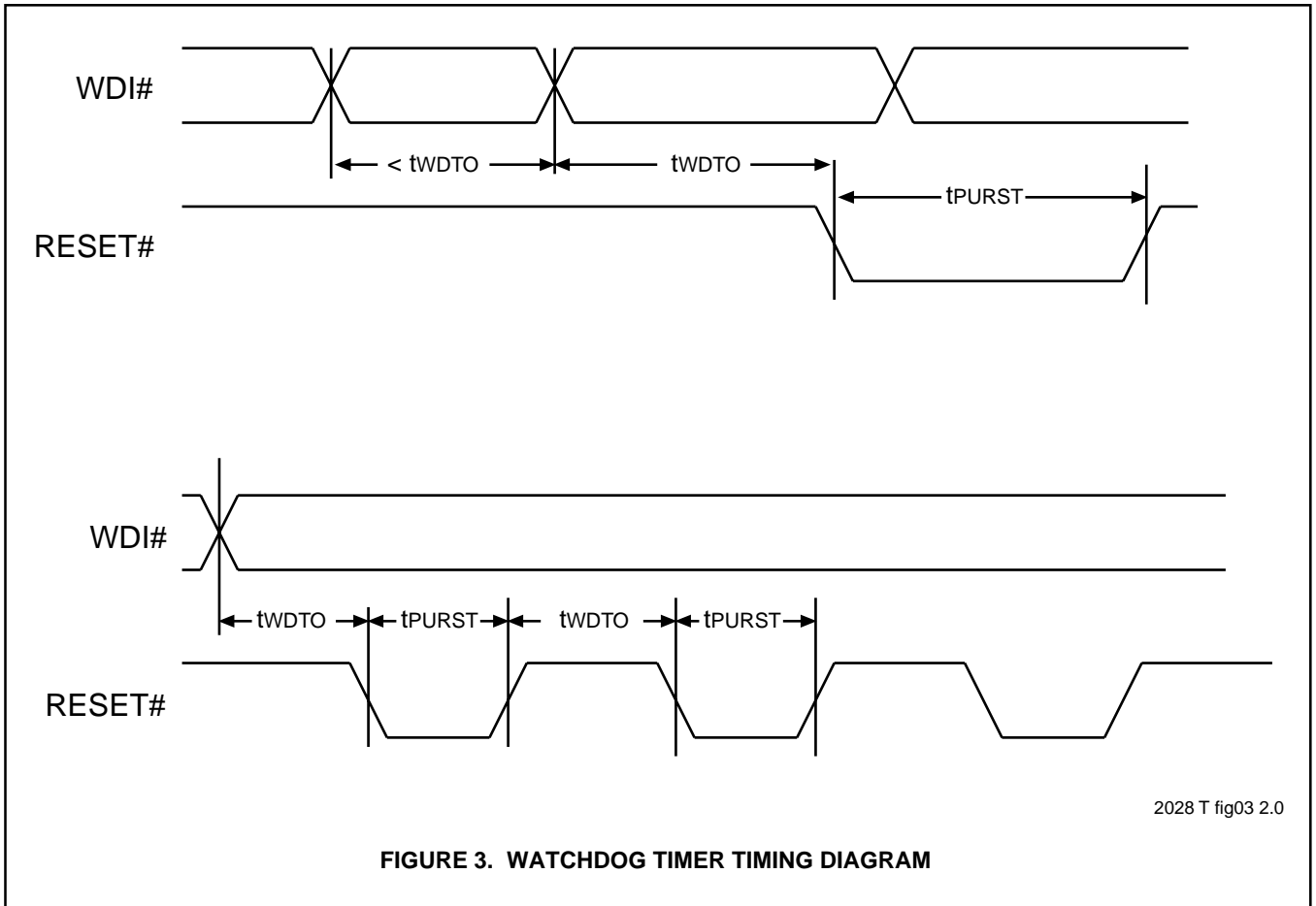| Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4.0		0.6		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		µs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

2028 PGM T5.0

2028 5.1 8/2/00
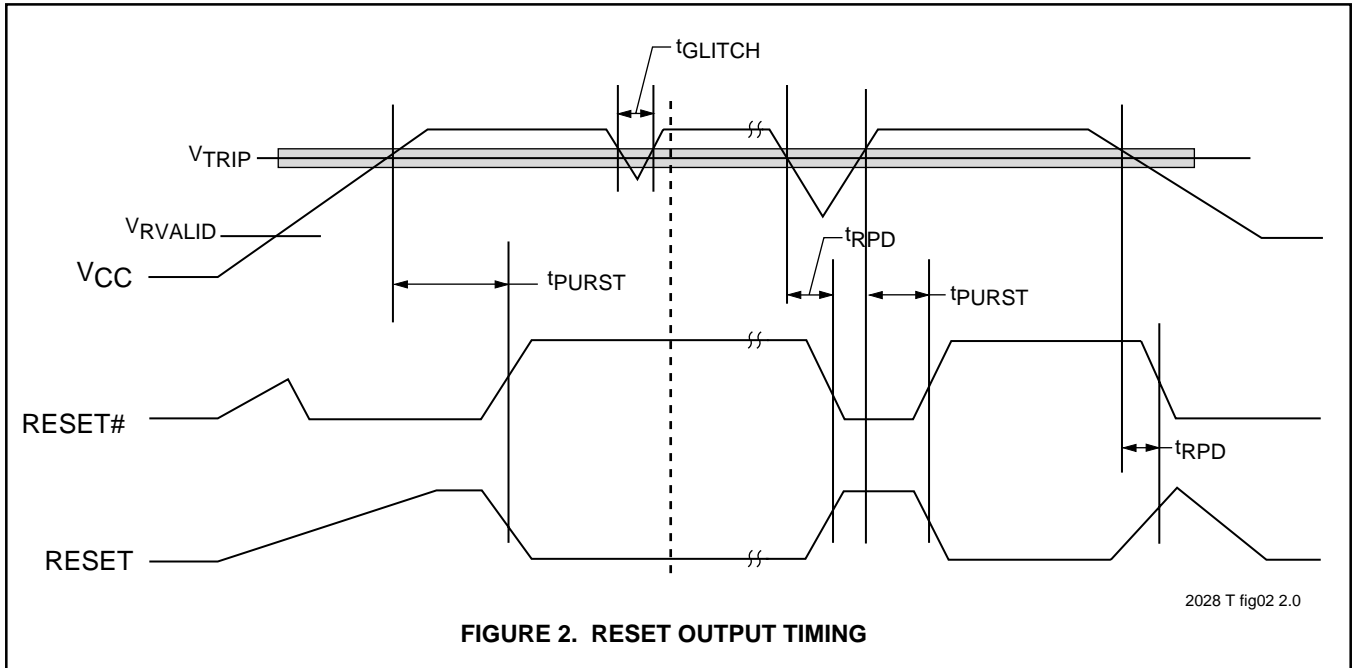
FIGURE 2. RESET OUTPUT TIMING

2028 T fig02 2.0

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS
T_A=-40°C to +85°C

Symbol	Parameter	Part no. Suffix	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset Trip Point	A (or) Blank	4.250	4.375	4.5	V
		B	4.50	4.625	4.75	V
		2.7	2.55	2.65	2.75	V
t_{PURST}	Reset Timeout			200		ms
t_{RPD}	V_{TRIP} to RESET Output Delay				5	µs
V_{RVALID}	RESET Output Valid to V_{CC} min. Guarantee		1			V
t_{GLITCH}	Glitch Reject Pulse Width note 1			30		ns
V_{OLRS}	RESET Output Low Voltage I_{OL} = 1mA				0.4	V
V_{OHRS}	RESET High Voltage Output I_{OH} = 800µA		V_{CC}-.75			V
V_{ULH}	V_{SENSE} Under-voltage threshold low to high		1.20	1.25	1.30	V
V_{UHL}	V_{SENSE} Under-voltage threshold high to low		1.20	1.25	1.30	V
V_{OLH}	V_{SENSE} Over-voltage threshold low to high		1.20	1.25	1.30	V
V_{OHL}	V_{SENSE} Over-voltage threshold high to low		1.20	1.25	1.30	V
t_{VD1}	Delay to V_{LOW} Active				5	µs
t_{VD2}	Delay to V_{LOW} Released				5	µs
t_{WDTO}	Watchdog timeout Period			1600		ms

WDI#

< t_{WDTO}

t_{WDTO}

t_{PURST}

RESET#

WDI#

t_{WDTO} → ← t_{PURST} → ← t_{WDTO} → ← t_{PURST} →

RESET#

2028 T fig03 2.0

FIGURE 3. WATCHDOG TIMER TIMING DIAGRAM

RESET# (in)

RESET# (out)

t_{PURST}

t_{PURST}

RESET (out)

2028 T fig04 2.0

FIGURE 4. RESET AS AN INPUT FUNCTION

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET# - RESET# is an active low output. Whenever V_{CC} is below V_{TRIP} the SMS29xx will drive the RESET# pin to ground. The RESET# pin is an I/O and can be used as a reset input. Refer to Figure 1 as an example use of this pin as a push button switch debounce circuit. It should be noted this is an open drain output and an external pull-up resistor tied to V_{CC} is needed for proper operation.

RESET — RESET is an active high output. Whenever V_{CC} is below V_{TRIP} the SMS29xx will drive the RESET pin to the V_{CC} rail. The RESET pin is an I/O and can be used as a reset input. It should be noted this is an open drain output and an external pull-down resistor tied to ground is needed for proper operation.

WDI# - The WDI# input is used as a hardware method of clearing the watchdog timer. A high to low transition on this pin will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

ENDURANCE AND DATA RETENTION

The SMS29xx is designed for applications requiring 100,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 erase/write cycles.

Reset Controller Description

The SMS29xx provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for t_{PURST} (200 msec) after reaching V_{TRIP}. The RESET outputs will be valid so long as V_{CC} is > 1.0V. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The RESET pins are I/Os; therefore, the SMS29xx can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET# input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.

WATCHDOG TIMER OPERATION

The SMS29xx has a watchdog timer with a programmable timeout period. Whenever the watchdog times out it will generate a reset output on both RESET# and RESET.

Any transition on WDI will clear the watchdog timer. If a transition is not detected within t_{WDTO} seconds the watchdog will time out and force the reset outputs active.
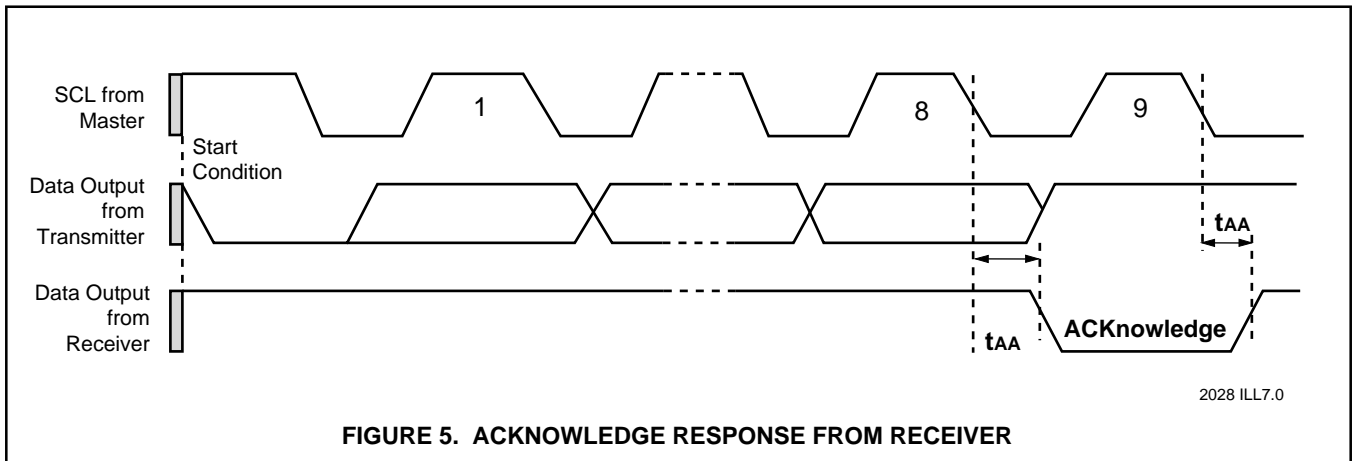
FIGURE 5. ACKNOWLEDGE RESPONSE FROM RECEIVER

CHARACTERISTICS OF THE I^{2}C BUS

General Description
The I^{2}C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition.

START and STOP Conditions
When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition .

DEVICE OPERATION

The SMS29xx is a 2K/4K/16K serial E^{2}PROM. The device supports the I^{2}C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the SMS29xx will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 5).

The SMS29xx will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS29xx will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS29xx transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS29xx will continue to transmit data. If an ACKnowledge is not detected, the SMS29xx will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier ('1010') (see figure 6).
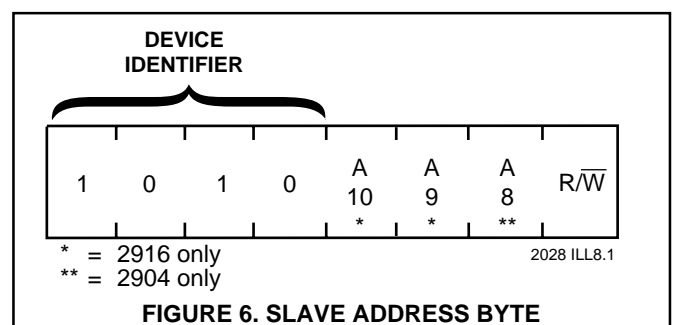

DEVICE IDENTIFIER							
1	0	1	0	A 10 *	A 9 *	A 8 **	R/$\overline{W}$

* = 2916 only
** = 2904 only

FIGURE 6. SLAVE ADDRESS BYTE

The next three bits are the high order address bits on the 2904 and 2916 and are "Don't Care" on the 2902.

Read/Write Bit
The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The SMS29xx allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte WRITE
Upon receipt of both the slave address and word address, the SMS29xx responds with an ACKnowledge for each. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS29xx begins the internal write cycle.

While the internal write cycle is in progress, the SMS29xx inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

Page WRITE
The SMS29xx is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the SMS29xx will respond with an ACKnowledge.

The SMS29xx automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

**FIGURE 7. PAGE/BYTE WRITE MODE**
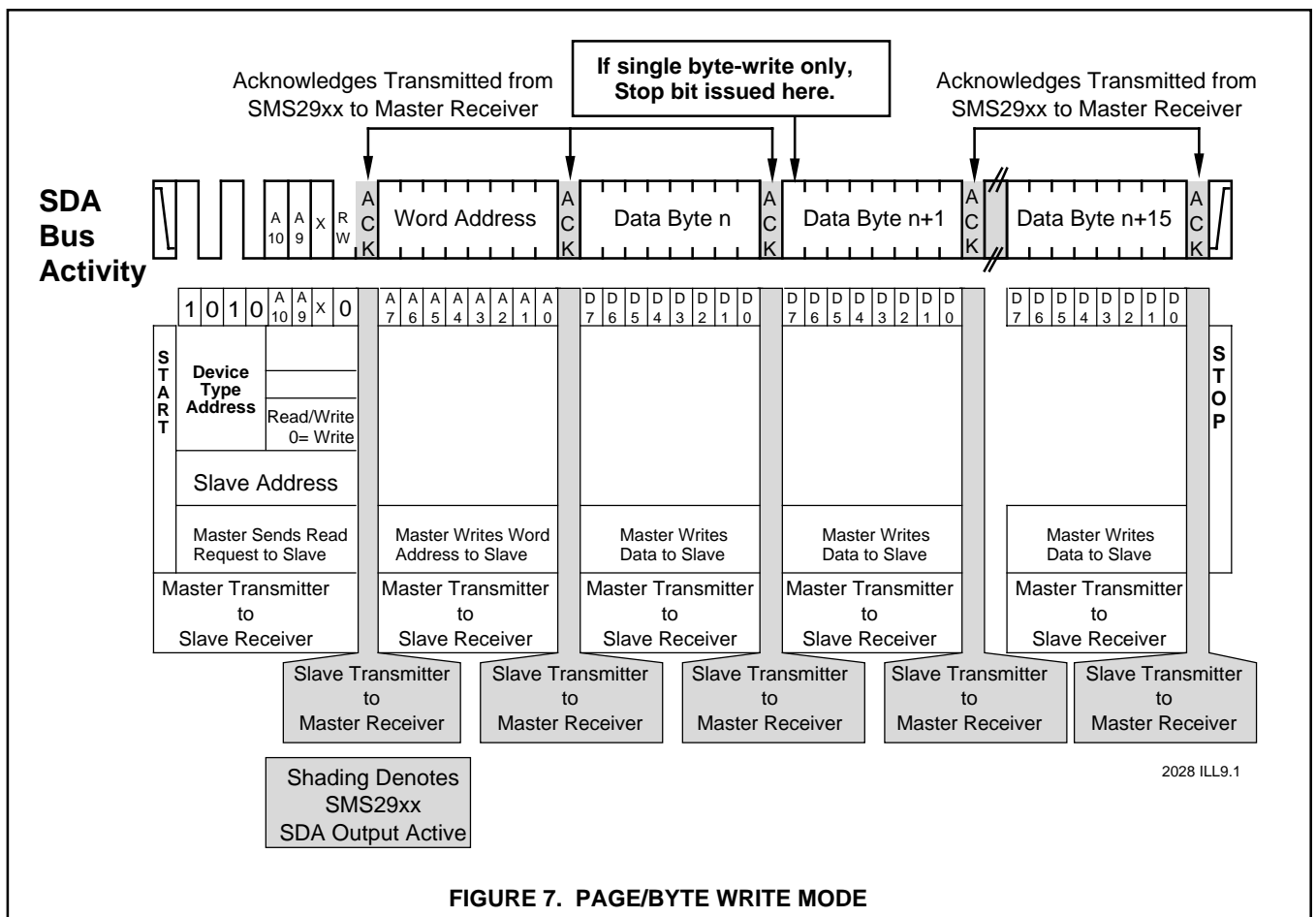
Acknowledge Polling

When the SMS29xx is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 8).

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FIGURE 8. ACKNOWLEDGE POLLING
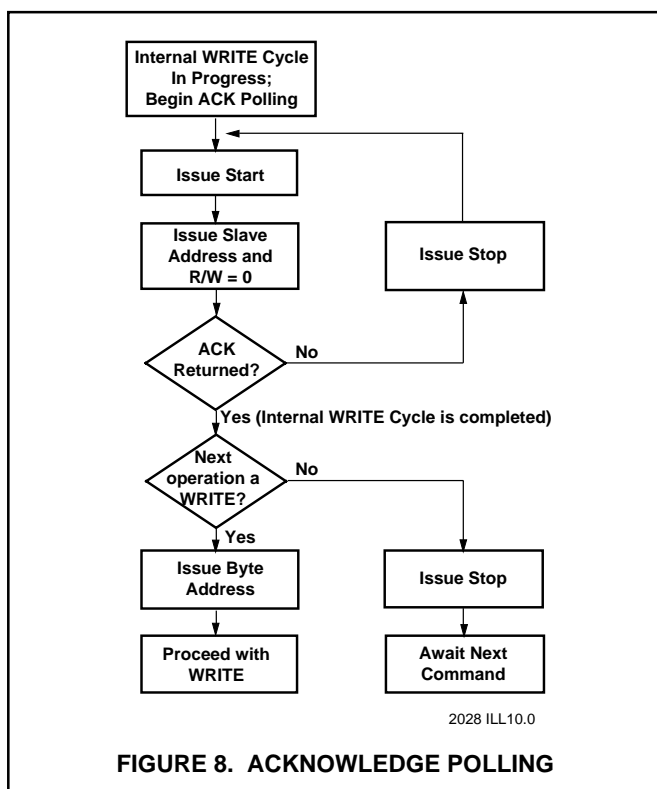
READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The SMS29xx contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS29xx receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS29xx discontinues data transmission. See Figure 9 for the address acknowledge and data transfer sequence.

2028 ILL11.1

FIGURE 9. CURRENT ADDRESS BYTE READ MODE
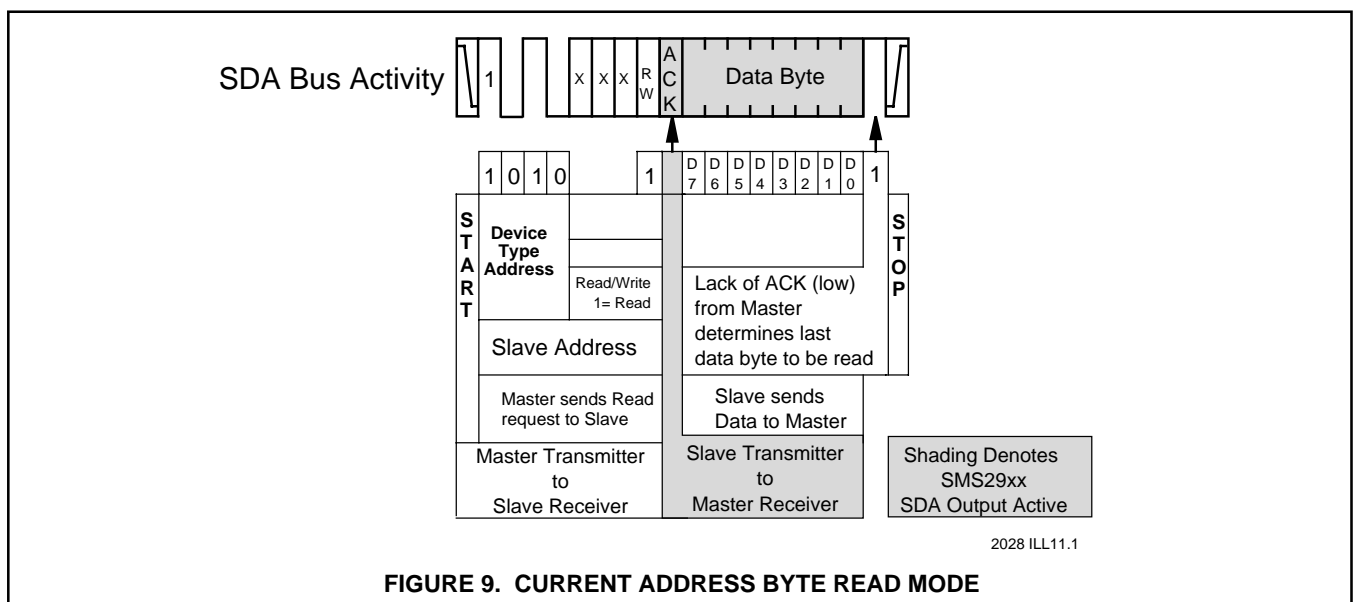
Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS29xx to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS29xx will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS29xx discontinues data transmission and reverts to its standby power mode. See Figure 10 for the address, acknowledge and data transfer sequence.

**FIGURE 10. RANDOM ADDRESS BYTE READ MODE**

2028 ILL12.1
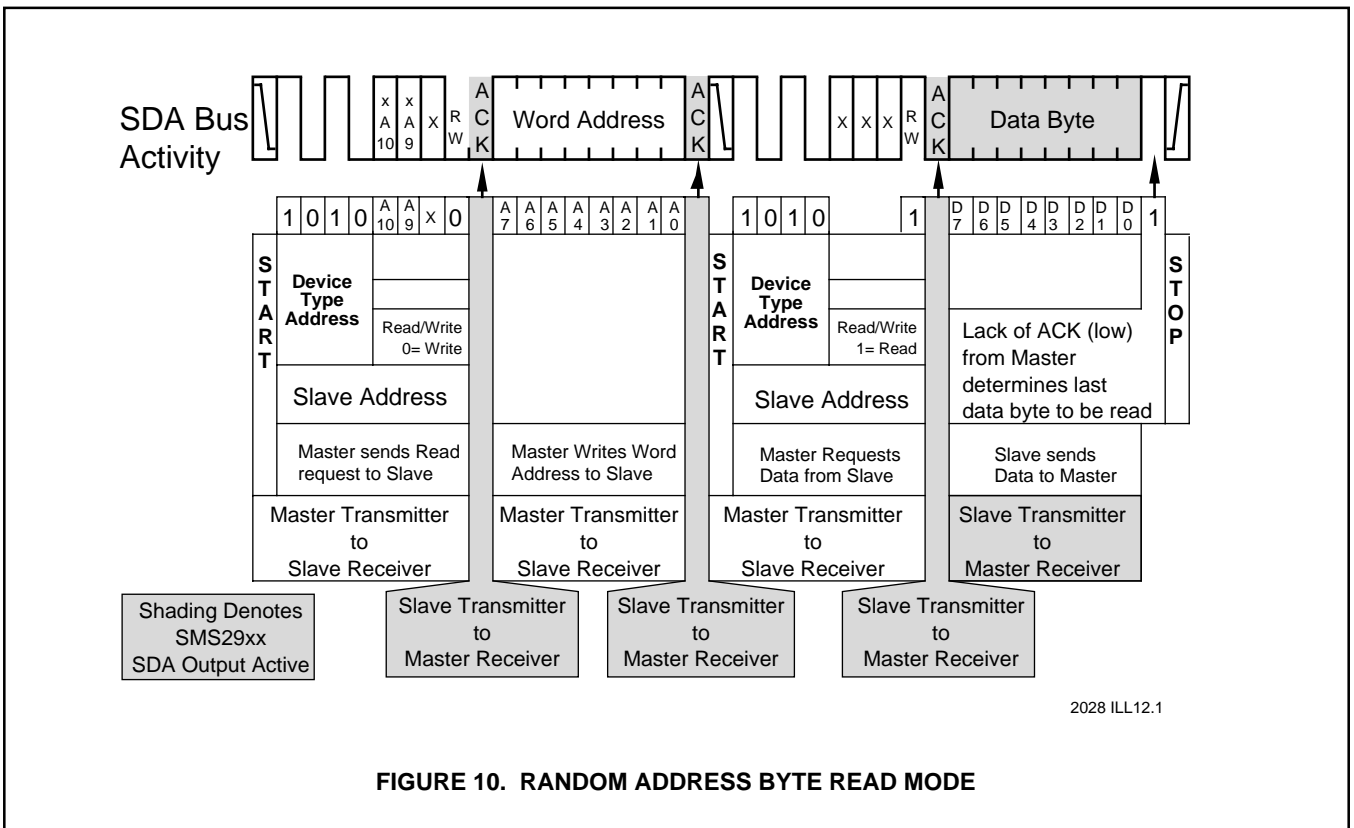
Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS29xx. The SMS29xx continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 11 for the address, acknowledge and data transfer sequence.
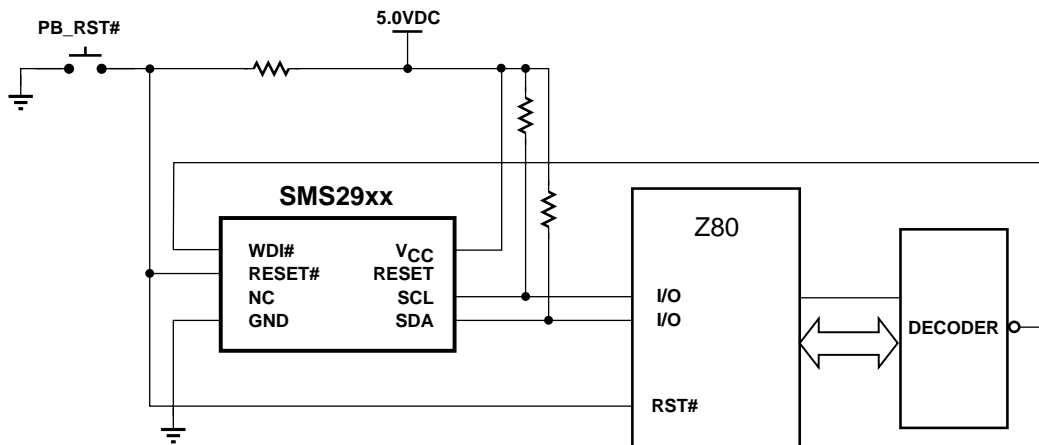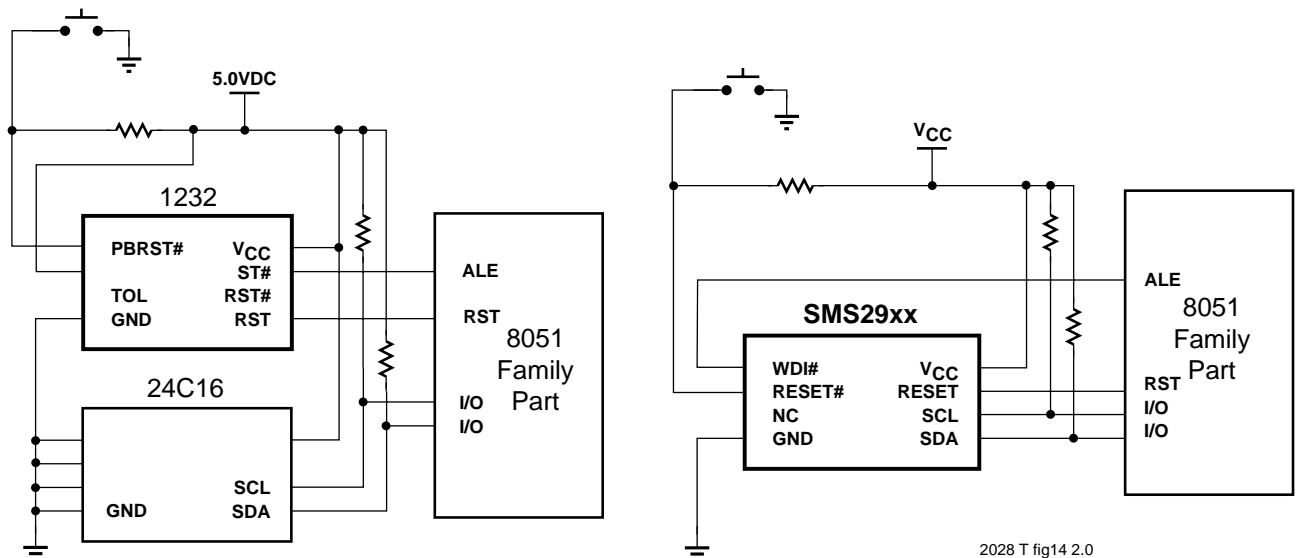

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FIGURE 11. SEQUENTIAL READ OPERATION (starting with a Random Address READ)
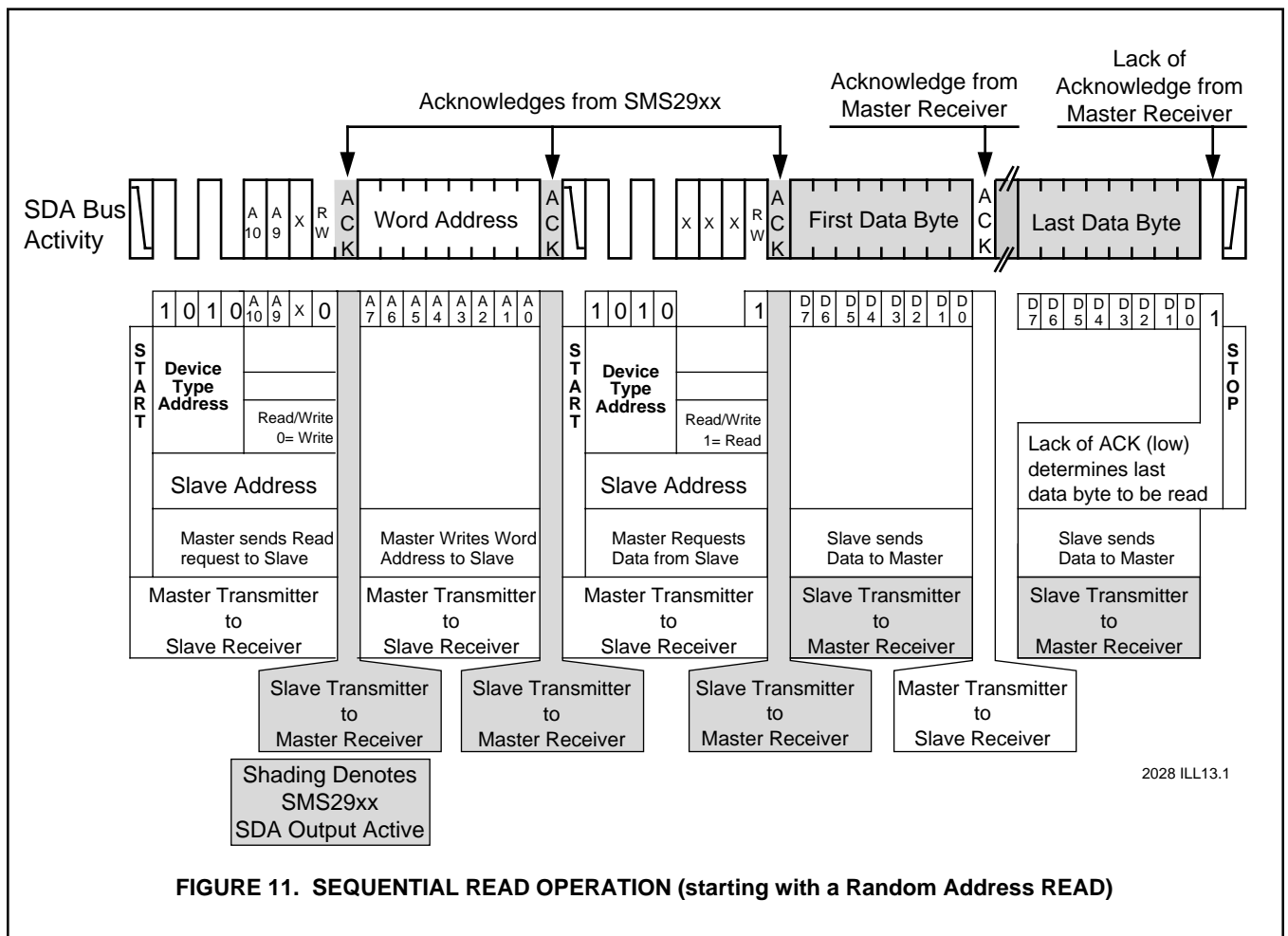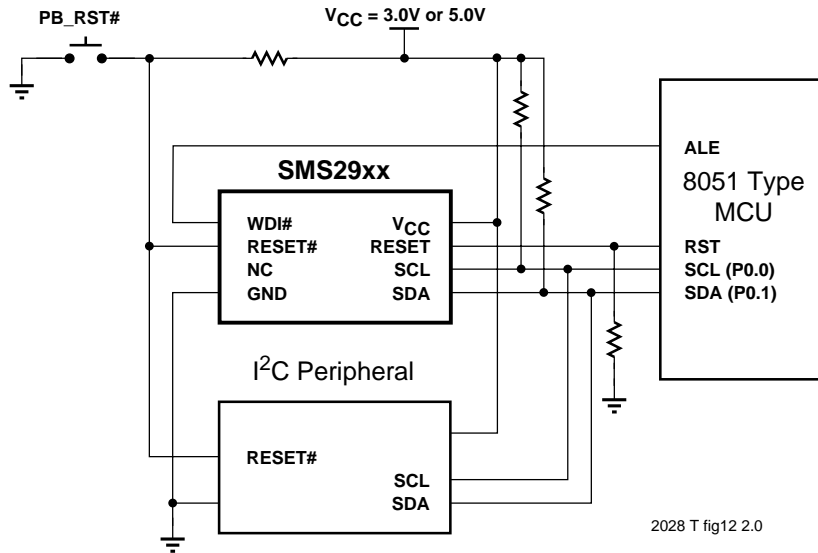
TYPICAL APPLICATION USING DUAL RESET FUNCTION AND WATCHDOG TIMER

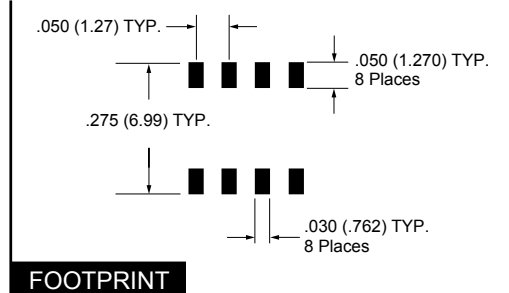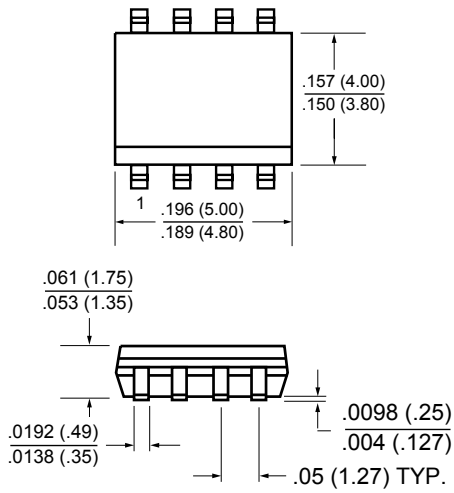**TYPICAL APPLICATION CONFIGURATION USING SYSTEM DECODE LOGIC TO RESET WDI**
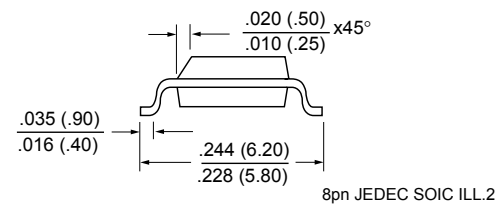
From This   **To This**

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)

.157 (4.00)
.150 (3.80)

1   .196 (5.00)
.189 (4.80)

.061 (1.75)
.053 (1.35)

.0192 (.49)
.0138 (.35)

.0098 (.25)
.004 (.127)

.05 (1.27) TYP.

.050 (1.27) TYP.

.050 (1.270) TYP.
8 Places

.275 (6.99) TYP.

.030 (.762) TYP.
8 Places

FOOTPRINT

.020 (.50)
.010 (.25) x45°

.035 (.90)
.016 (.40)

.244 (6.20)
.228 (5.80)

8pn JEDEC SOIC ILL.2

ORDERING INFORMATION

SMS2902 **S** **A**

Base Part Number

Package
S = SOIC

V_{TRIP}
A = 4.5V
B = 4.75V
2.7 = 2.7V
Blank = 4.5V

2028-02 Tree 2.0

SMS2904 **S** **A**

Base Part Number

Package
S = SOIC

V_{TRIP}
A = 4.5V
B = 4.75V
2.7 = 2.7V
Blank = 4.5V

2028-04 Tree 2.0

SMS2916 **S** **A**

Base Part Number

Package
S = SOIC

V_{TRIP}
A = 4.5V
B = 4.75V
2.7 = 2.7V
Blank = 4.5V

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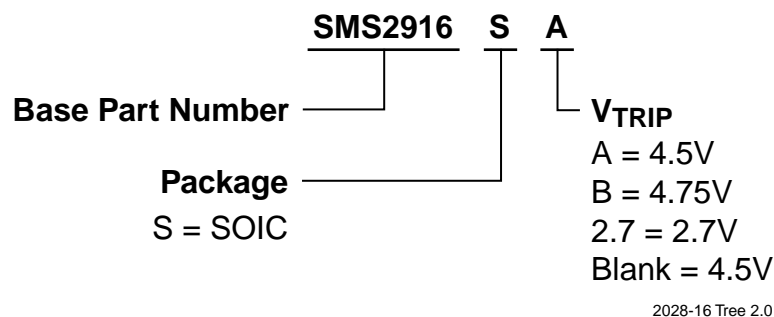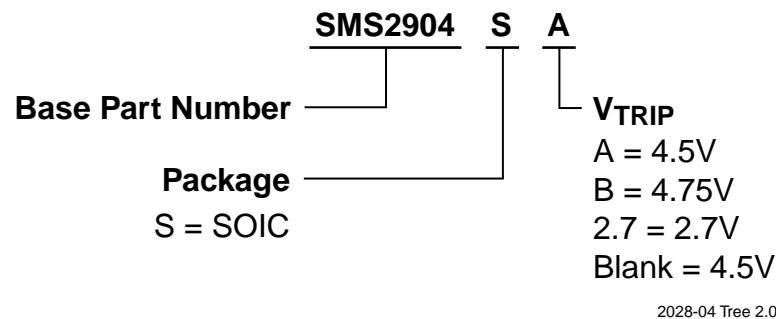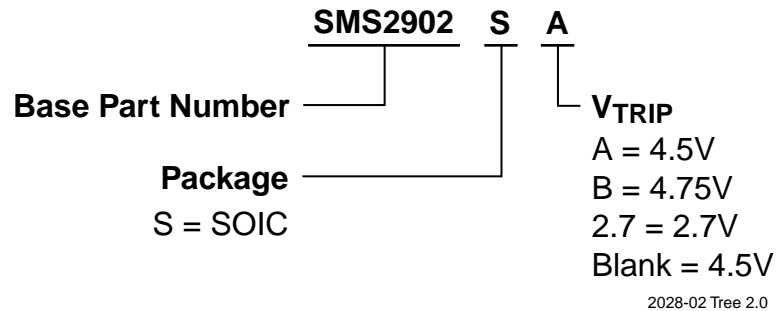
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