

## SWITCHING

### N-CHANNEL POWER MOS FET

#### DESCRIPTION

The  $\mu$ PA2702GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

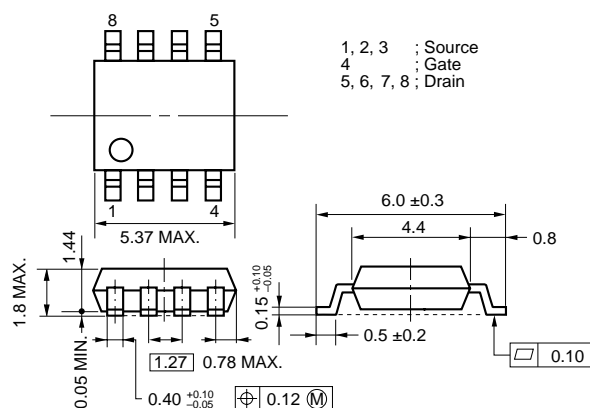
#### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 9.2 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$   
 $R_{DS(on)2} = 14.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 900 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA2705GR	Power SOP8

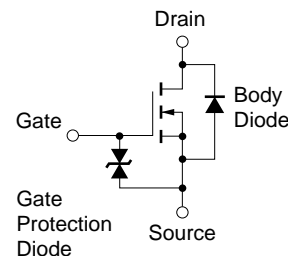
#### PACKAGE DRAWING (Unit: mm)



#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 13$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 52$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	13	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	16.9	mJ

#### EQUIVALENT CIRCUIT



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

**3.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu\text{H}$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

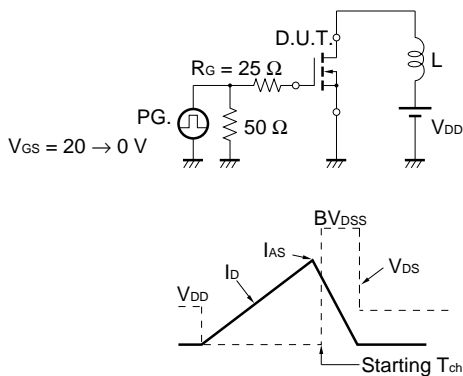
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.  
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

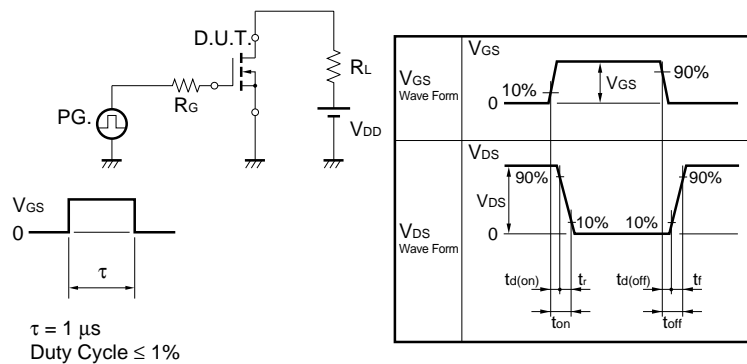
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5		2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.0 A	7	13		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.0 A		7.3	9.2	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.0 A		11.1	14.8	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 7.0 A		12.7	17.0	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		900		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		380		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		120		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 7.0 A		9		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		5		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		35		ns
Fall Time	t <sub>f</sub>			8		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V		9		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		3		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 13 A		4		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		0.82	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		28		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		22		nC

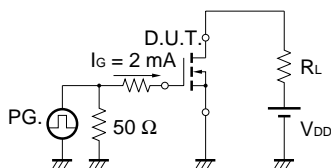
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**



[MEMO]

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