8 Mb (1024K x 8) MoBL® Static RAM

Features

- **Very high speed: 55 ns**
  - **— Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
  - **— Typical active current:1.5 mA @ f = 1 MHz**
  - **— Typical active current: 12 mA @ f = f_{max}(55-ns speed)**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball BGA, 48-pin TSOPI, and 44-pin TSOPII**

Functional Description[1]

The CY62158DV is a high-performance CMOS static RAMs organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable 2 (CE_2) HIGH. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.
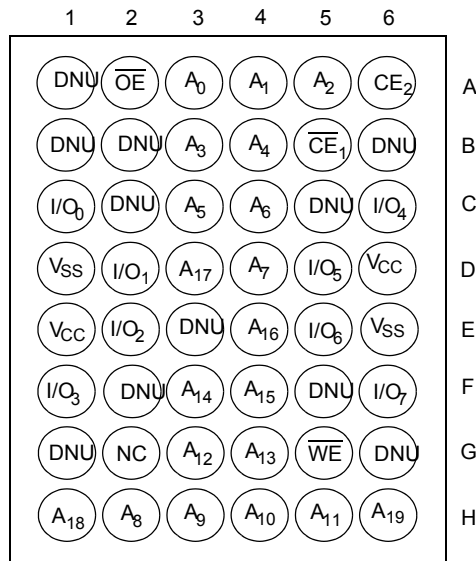
The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the truth table for a complete description of read and write modes.

Logic Block Diagram
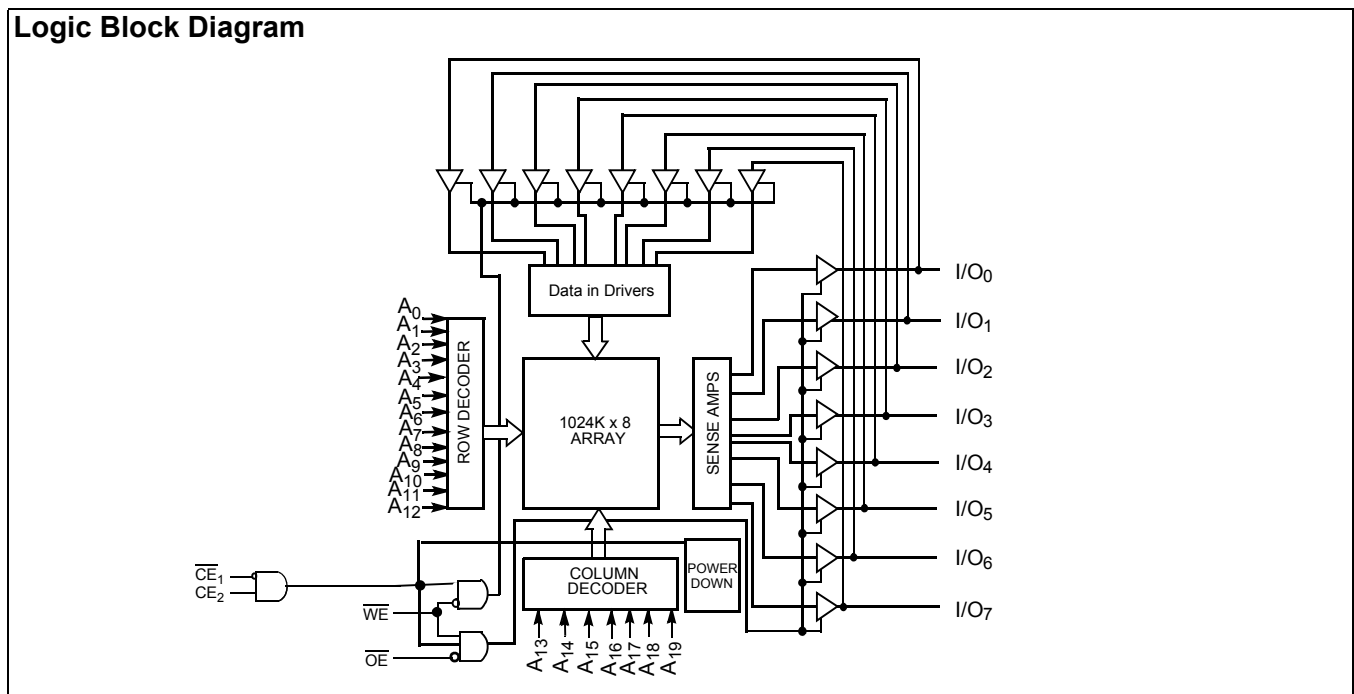
Note:
1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at http://www.cypress.com.

PRELIMINARY

Pin Configuration[2,3]

FBGA
Top View

	1	2	3	4	5	6	
A	DNU	$\overline{OE}$	A_0	A_1	A_2	CE_2	A
B	DNU	DNU	A_3	A_4	$\overline{CE_1}$	DNU	B
C	I/O_0	DNU	A_5	A_6	DNU	I/O_4	C
D	V_{SS}	I/O_1	A_{17}	A_7	I/O_5	V_{CC}	D
E	V_{CC}	I/O_2	DNU	A_{16}	I/O_6	V_{SS}	E
F	I/O_3	DNU	A_{14}	A_{15}	DNU	I/O_7	F
G	DNU	NC	A_{12}	A_{13}	$\overline{WE}$	DNU	G
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{19}	H

48TSOPI
Top View

Pin	Signal		Pin	Signal
1	A15		48	A16
2	A14		47	Vss
3	A13		46	Vss
4	A12		45	A19
5	A11		44	I/O7
6	A10		43	DNU
7	A9		42	I/O6
8	A8		41	DNU
9	NC		40	I/O5
10	DNU		39	DNU
11	$\overline{WE}$		38	I/O4
12	CE_2		37	Vcc
13	DNU		36	DNU
14	$\overline{BHE}$		35	I/O3
15	$\overline{BLE}$		34	DNU
16	A18		33	I/O2
17	A17		32	DNU
18	A7		31	I/O1
19	A6		30	DNU
20	A5		29	I/O0
21	A4		28	$\overline{OE}$
22	A3		27	Vss
23	A2		26	$\overline{CE_1}$
24	A1		25	A0

44 TSOPII
Top View

Pin	Signal		Pin	Signal
1	A_4		44	A_5
2	A_3		43	A_6
3	A_2		42	A_7
4	A_1		41	$\overline{OE}$
5	A_0		40	CE_2
6	$\overline{CE_1}$		39	A8
7	DNU		38	DNU
8	DNU		37	DNU
9	I/O_0		36	I/O_7
10	I/O_1		35	I/O_6
11	V_{CC}		34	V_{SS}
12	V_{SS}		33	V_{CC}
13	I/O_2		32	I/O_5
14	I/O_3		31	I/O_4
15	DNU		30	DNU
16	DNU		29	DNU
17	$\overline{WE}$		28	A_9
18	A_{19}		27	A_{10}
19	A_{18}		26	A_{11}
20	A_{17}		25	A_{12}
21	A_{16}		24	A_{13}
22	A_{15}		23	A_{14}

Notes:
2. NC pins are not internally connected to the die.
3. DNU pins have to be left floating or tied to V_{SS} to ensure proper application.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...55°C to +125°C

Supply Voltage to Ground Potential .–0.2V to $V_{cc(max)}$ + 0.2V

DC Voltage Applied to Outputs
in High-Z State[4] ....–0.2V to $V_{CC(max)}$ + 0.2V

DC Input Voltage[4] .... –0.2V to $V_{CC(max)}$ + 0.2V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage..>2001V
(per MIL-STD-883, Method 3015)

Latch-up Current...>200 mA

Operating Range

Product	Range	Ambient Temperature (T_A)	V_{CC}[5]
CY62158DVL	Industrial	–40°C to +85°C	2.2V to 3.6V
CY62158DVLL			

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2}(μA)	
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[6]	Max.		Typ.[6]	Max.	Typ.[6]	Max.	Typ.[6]	Max.
CY62158DVL	2.2	3.0	3.6	55	1.5	3	12	20	2	20
CY62158DVLL	2.2	3.0	3.6	55	1.5	3	12	15	2	8

Electrical Characteristics Over the Operating Range

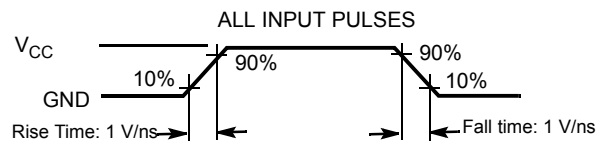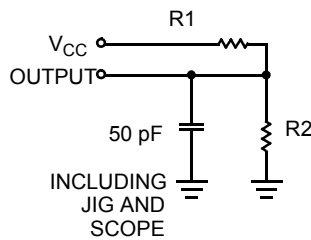| Parameter	Description	Test Conditions		CY62158DV-55			Unit
				Min.	Typ.[6]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V	2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V			0.4	V
		I_{OL} = 2.1mA	V_{CC} = 2.70V			0.4	V
V_{IH}[7]	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3V	V
		V_{CC}= 2.7V to 3.6V		2.2		V_{CC} + 0.3V	V
V_{IIL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V		–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	L		12	20	mA
				LL			15	mA
		f = 1 MHz		L		1.5	3	mA
				LL			3	mA
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC}– 0.2V, CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = 3.60V		L		2	20	μA
				LL		2	8	
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V		L		2	20	μA
				LL		2	8	

Notes:
4. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
5. Full device AC operation requires linear Vcc ramp from 0 to Vcc(min) >= 500 μs.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.
7. $V_{IH(max)}$= V_{CC}+0.75V for pulse duration less than 20ns.

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOP II	TSOP I	Unit
Θ_{JA}	Thermal Resistance[8] (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	55	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance[8] (Junction to Case)		16	TBD	TBD	°C/W

AC Test Loads and Waveforms
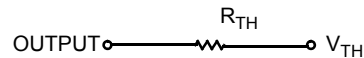
Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

| Parameter	Description	Conditions		Min.	Typ.[6]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5		2.2V	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.5V $\overline{CE_1} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			10	μA
			LL			4	μA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[9]	Operation Recovery Time			t_{RC}			ns

Notes:
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ μs or stable at $V_{CC(min.)} \geq 100$ μs.

Data Retention Waveform
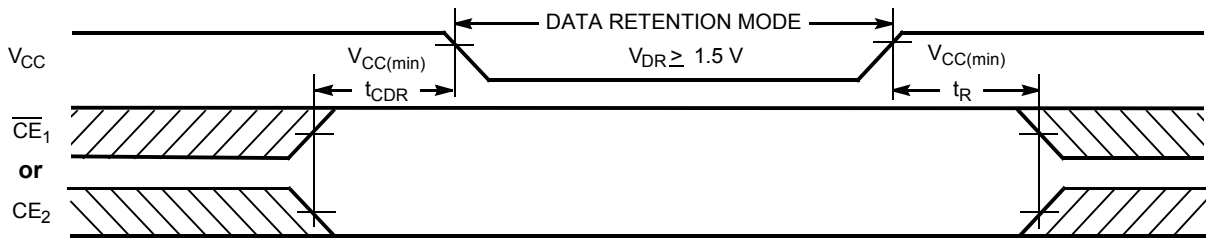
Switching Characteristics Over the Operating Range [10]

| Parameter	Description	55 ns Min.	55 ns Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[11]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[11]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[11, 12]		20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-Down		55	ns
Write Cycle[13]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	40		ns
t_{AW}	Address Set-Up to Write End	40		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[11, 12]		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[11]	10		ns

Notes:
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of $V_{CC(typ.)}$/2, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state. Transition is measured +/-200mV from steady state voltage.
13. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [14, 15]
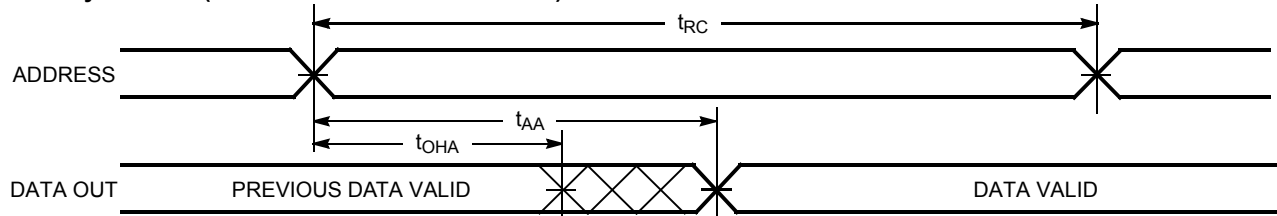
Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]
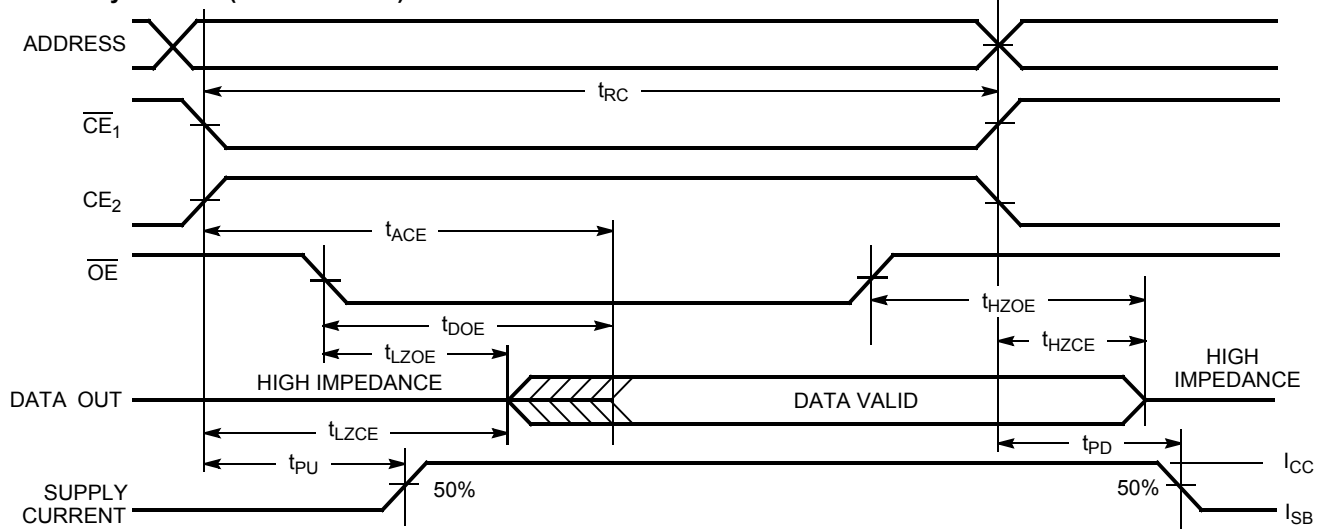
Write Cycle No. 1($\overline{WE}$ Controlled) [13, 17, 19]
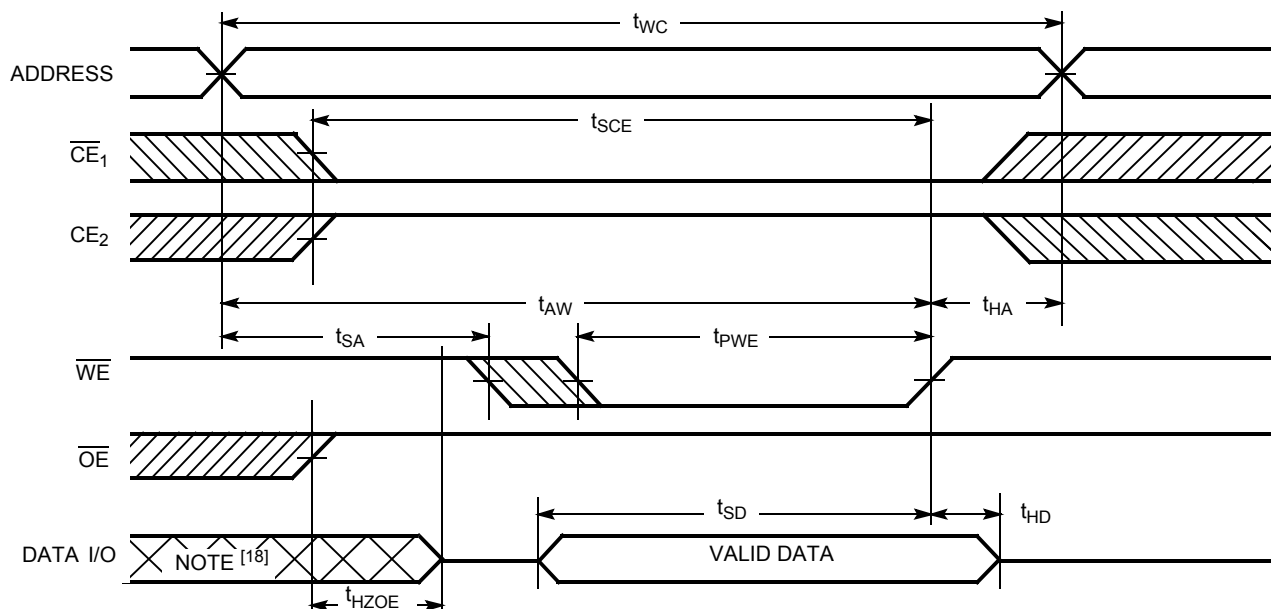
Notes:
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

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Switching Waveforms (continued)

Write Cycle No. 2($\overline{CE}_1$ or CE_2 Controlled) [13, 17, 19]
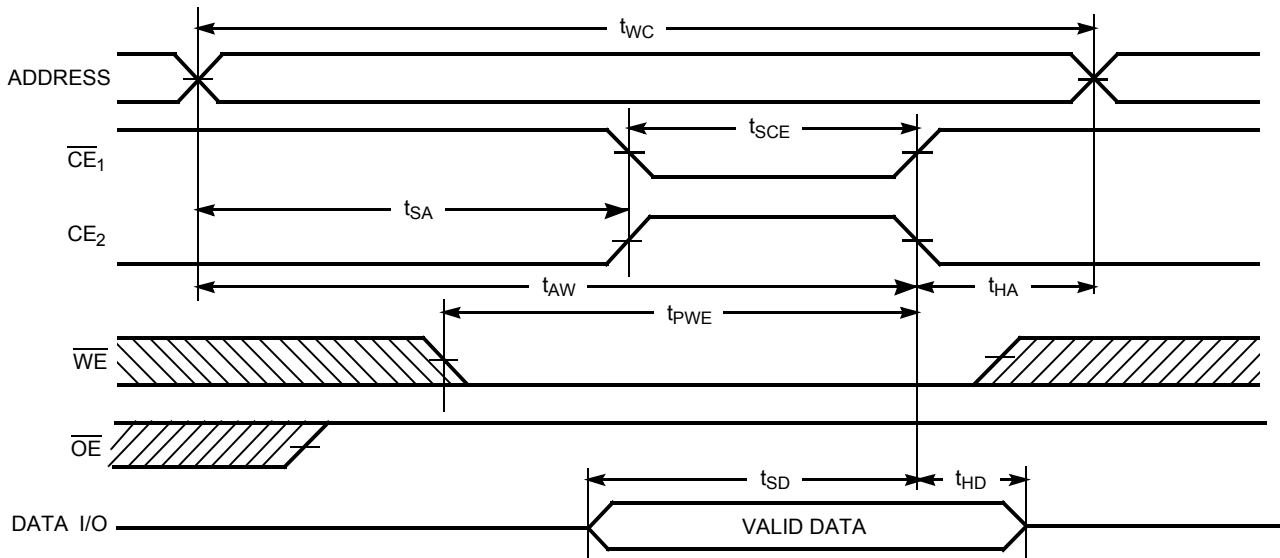
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [19]
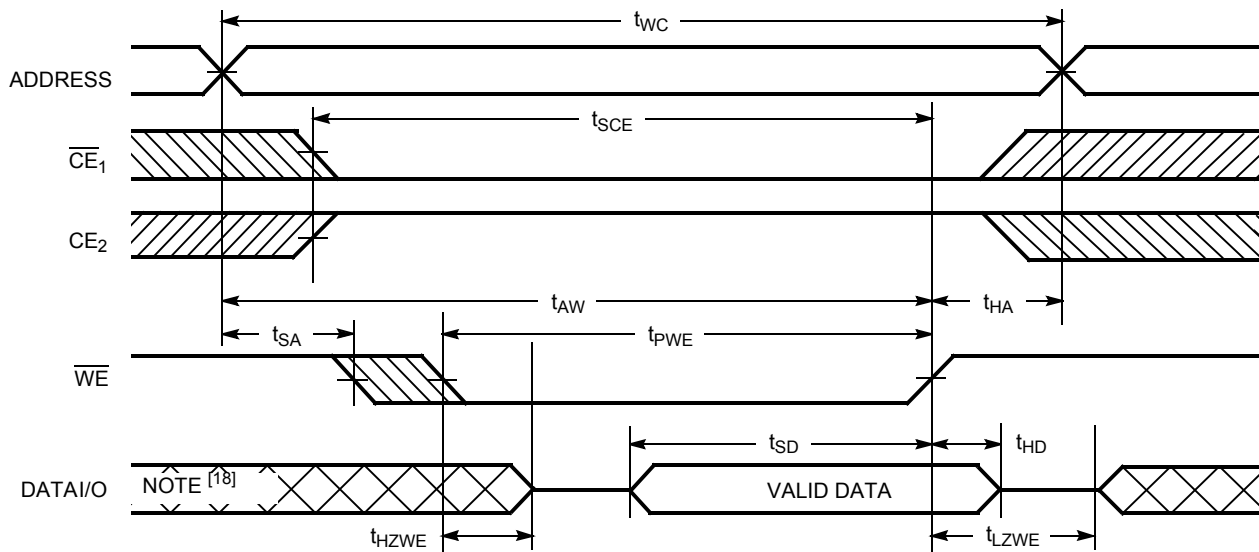
Truth Table

| $\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out (I/O$_0$-I/O$_7$)	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (Icc)
L	H	L	X	Data in (I/O$_0$-I/O$_7$)	Write	Active (Icc)

Notes:
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. During this period, the I/Os are in output state and input signals should not be applied.
19. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62158DVL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62158DVLL-55BVI			
55	CY62158DVL-55ZI	Z-48	48 Pin TSOP I	Industrial
	CY62158DVLL-55ZI			
55	CY62158DVL-55ZSI	ZS-44	44 Pin TSOP II	Industrial
	CY62158DVLL-55ZSI			

Package Diagrams

48-lead VFBGA (6 x 8 x 1 mm) BV48A

51-85150-*B
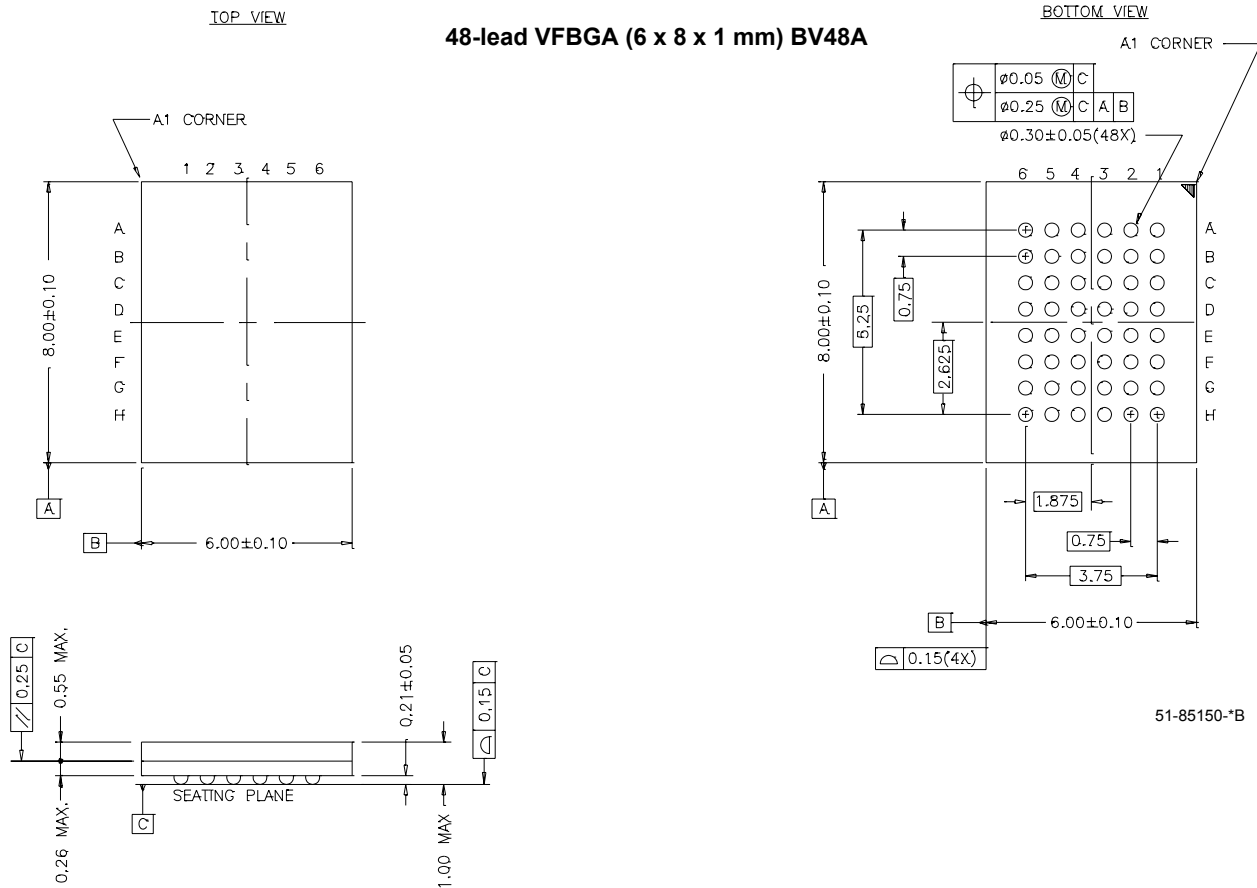
Package Diagrams (continued)

48-pin TSOP I Z48

DIMENSIONS IN INCHES[MM] MIN./MAX.

51-85183-*A
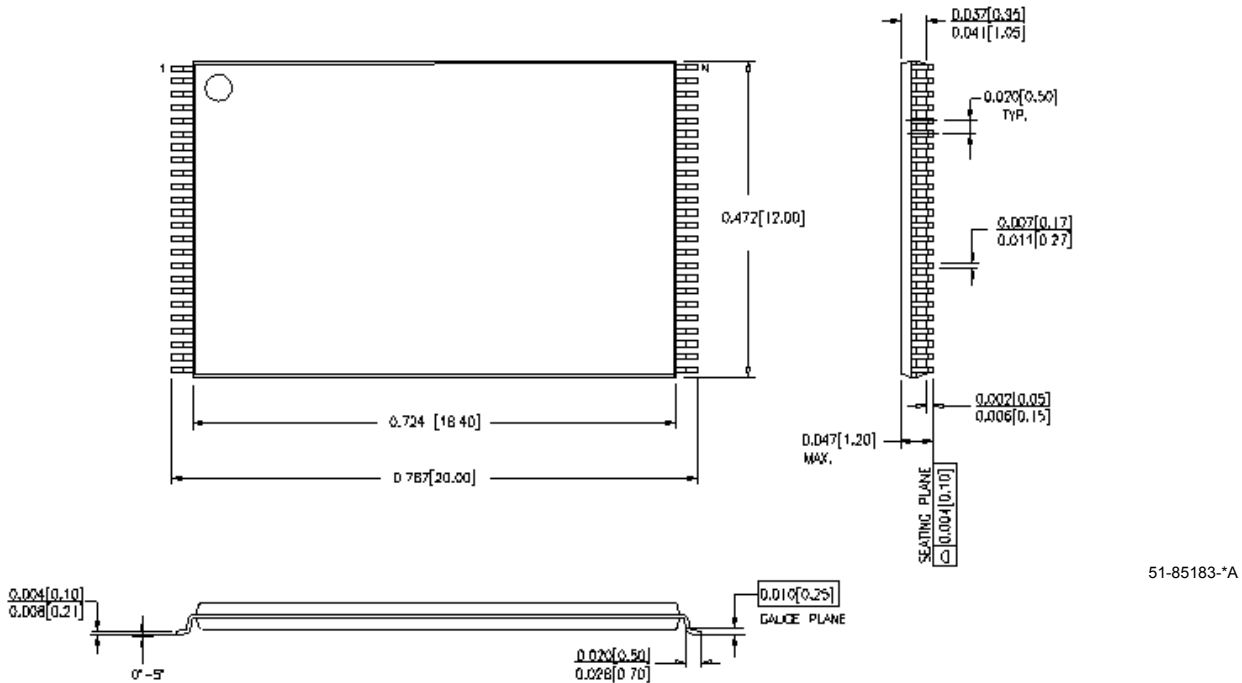
44-pin TSOP II ZS44

DIMENSION IN MM (INCH) MAX/MIN

TOP VIEW

BOTTOM VIEW

51-85087-*A
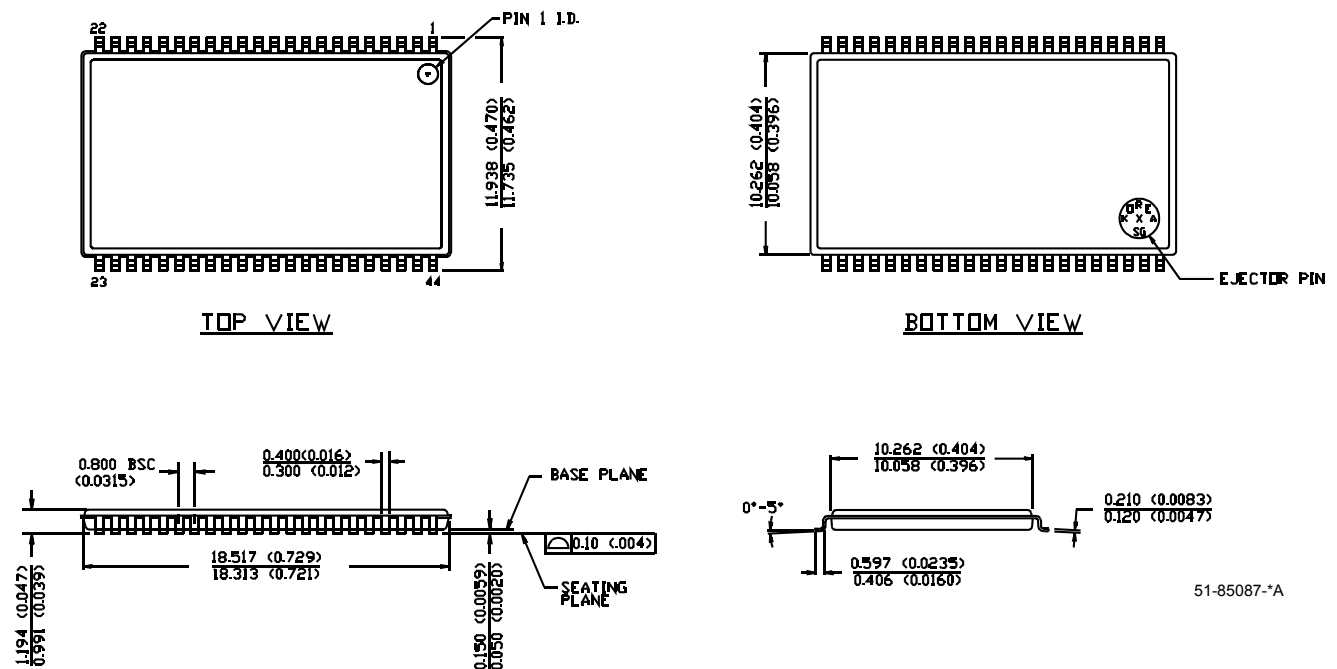
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Document History Page

Document Title:CY62158DV MoBL® 8 Mb (1024K x 8) MoBL® Static RAM
Document Number: 38-05391

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126293	05/22/03	HRT	New Data Sheet
*A	131014	11/25/03	CBD	Change from Advance to Preliminary
*B	133114	01/24/04	CBD	Minor Change: MPN change and upload