HEWLETT PACKARD

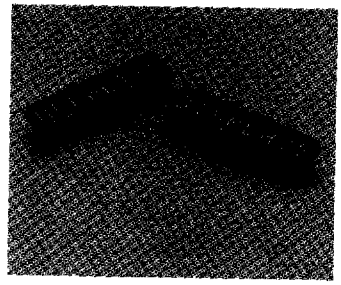
Eight Character 5.0 mm (0.2 inch) Hermetic Smart 5 X 7 Alphanumeric Displays For Military Applications

Technical Data

HDSP-2131/2131TXV/ 2131TXVB
HDSP-2132/2132TXV/ 2132TXVB
HDSP-2133/2133TXV/ 2133TXVB
HDSP-2179/2179TXV/ 2179TXVB

Features

- **Wide Operating Temperature Range -55°C to +85°C**
- **True Hermetic Package for Yellow, Orange and High Efficiency Red Displays[1]**
- **TXVB Version Conforms to MIL-D-87157 Quality Level A Test Tables**
- **Smart Alphanumeric Display**
  On-Board CMOS IC
  Built-In RAM
  ASCII Decoder
  LED Drive Circuitry
- **128 ASCII Character Set**
- **16 User Definable Characters**
- **Programmable Features**
  Individual Flashing Character
  Full Display Blinking
  Multi-Level Dimming and Blanking
  Self Test
  Clear Function
- **Read/Write Capability**
- **Full TTL Compatibility**
- **HDSP-2131/-2133/-2179 Useable in Night Vision Lighting Applications**
- **Categorized for Luminous Intensity**
- **HDSP-2131/2133 Categorized for Color**
- **Excellent ESD Protection**
- **Wave Solderable**
- **X-Y Stackable**



Description

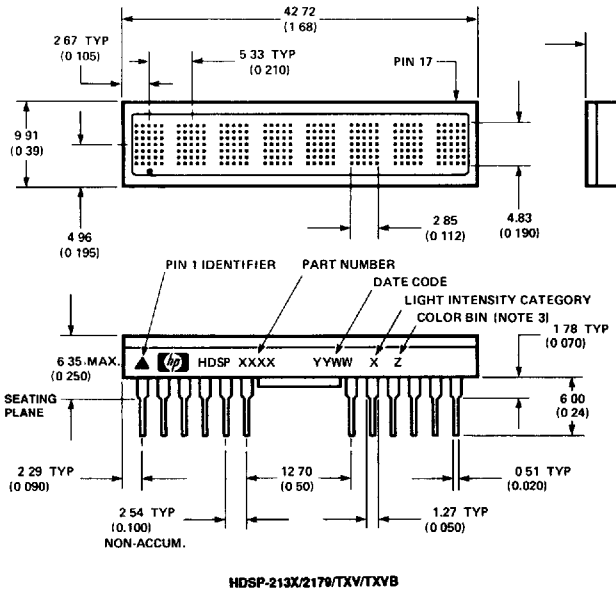
The HDSP-2131 (yellow), HDSP-2179 (orange), HDSP-2132 (high efficiency red) and the HDSP-2133 (green) are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0 mm (0.2 inch) high characters are packaged in a standard 7.64 mm (0.30 inch) 32 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in an on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-213X is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus. These features make the HDSP-213X ideally suited for applications where an hermetic, low power alphanumeric display is required.

Devices

Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-2131	HDSP-2132	HDSP-2133	HDSP-2179
HDSP-2131TXV	HDSP-2132TXV	HDSP-2133TXV	HDSP-2179TXV
HDSP-2131TXVB	HDSP-2132TXVB	HDSP-2133TXVB	HDSP-2179TXVB

Note: 1. The HDSP-2133 high peformance green displays conform to MIL-D-87157 hermeticity requirements.

Package Dimensions



HDSP-213X/2179/TXV/TXVB

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	CLS	17	GND (SUPPLY)
2	CLK	18	GND (LOGIC)
3	$\overline{WR}$	19	D4
4	$\overline{CE}$	20	D5
5	$\overline{RST}$	21	D6
6	$\overline{RD}$	22	D7
7	NO PIN	23	NO PIN
8	NO PIN	24	NO PIN
9	NO PIN	25	NO PIN
10	NO PIN	26	NO PIN
11	D0	27	$\overline{FL}$
12	D1	28	A0
13	D2	29	A1
14	D3	30	A2
15	NC	31	A3
16	V_{DD}	32	A4

Note:
1. All dimensions are in mm (inches).
2. Unless otherwise specified tolerance is ±0.30 mm (±0.015).
3. For green and yellow devices only.
4. Leads are copper alloy, solder dipped.

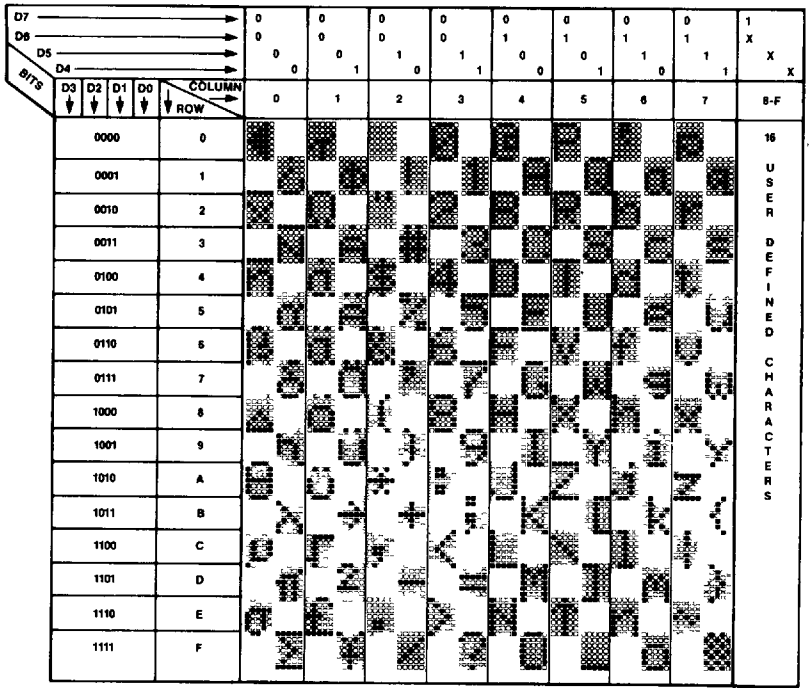
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A ..... -55°C to +85°C
Storage Temperature, T_S
HDSP-2131/-2132/-2179 ..... -65°C to +125°C
HDSP-2133 ..... -55°C to +100°C
CMOS IC Junction Temperature, T_J (IC) ..... +150°C
Maximum Solder Temperature
at Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDSP-2131, HDSP-2132, HDSP-2133, AND HDSP-2179.

Character Set



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

Parameter	Symbol	Min.	25°C Typ.[1]	25°C Max.[1]	Max.[2]	Units	Test Conditions
Input Leakage (Input without pullup)	I_I	-10.0			+10.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IP}	-30.0	11	18	30	µA	V_{IN} = 0 to V_{DD}, pins RST, CLS, WR, RD, CE, FL
I_{DD} Blank	I_{DD} (BLK)		0.5	1.5	2.0	mA	$V_{IN} = V_{DD}$
I_{DD} 8 digits 12 dots/character[3]	I_{DD}(V)		200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[3]	I_{DD}(#)		300	370	430	mA	"#" on in all 8 locations
Input Voltage High	V_{IH}	2.0			V_{DD} +0.3	V	V_{DD} = 5.5 V
Input Voltage Low	V_{IL}	GND -0.3 V			0.8	V	V_{DD} = 4.5 V
Output Voltage High	V_{OH}	2.4				V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK					0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-PIN	$R\theta_{J\text{-}PIN}$		11			°C/W	

Notes:
1. V_{DD} = 5.0 V.
2. Maximum I_{DD} occurs at -55°C.
3. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x Average I_{DD} (#).

Optical Characteristics at 25°C[4]

V_{DD} = 5.0 V at Full Brightness

High Efficiency Red HDSP-2132

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		635	nm
Dominant Wavelength	λ_d		626	nm

Orange HDSP-2179

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		600	nm
Dominant Wavelength	λ_d		602	nm

Yellow HDSP-2131

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		583	nm
Dominant Wavelength	λ_d		585	nm

High Performance Green HDSP-2133

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		568	nm
Dominant Wavelength	λ_d		574	nm

Note:
4. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5 to 5.5 V unless otherwise specified.

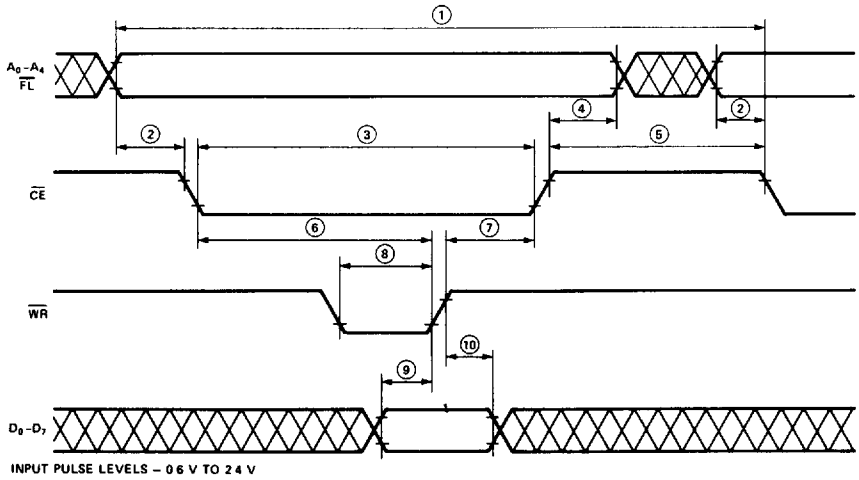
Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[1,2] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time[2,3]	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:
1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

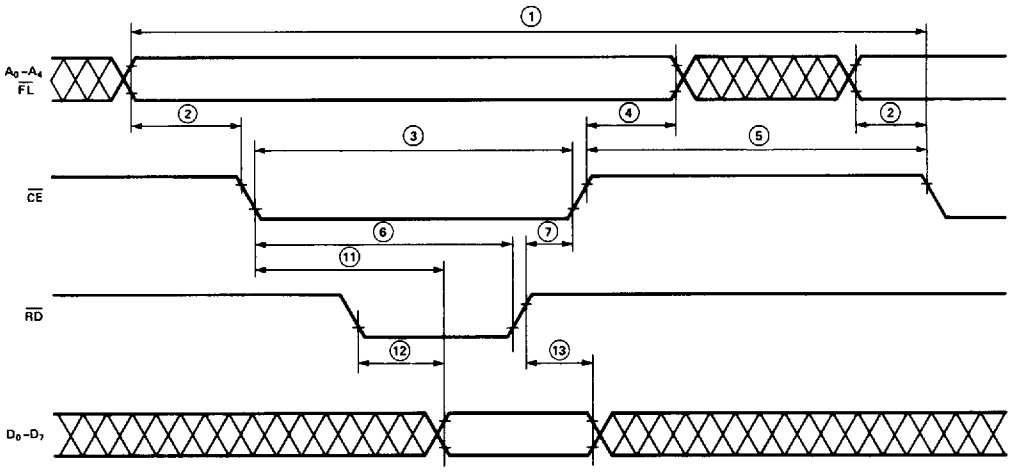
Symbol	Description	25°C Typical	Minimum[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[5]	Display Refresh Rate	256	128	Hz
F_{FL}[6]	Character Flash Rate	2	1	Hz
t_{ST}[7]	Self Test Cycle Time	4.6	9.2	Sec

Notes:
5. $F_{RF} = F_{OSC}/224$
6. $F_{FL} = F_{OSC}/28{,}672$
7. $t_{ST} = 262{,}144/F_{OSC}$

Write Cycle Timing Diagram



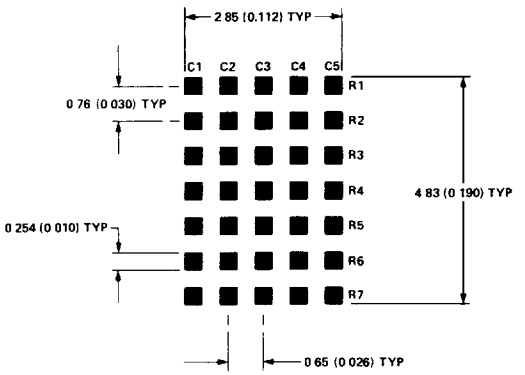
Read Cycle Timing Diagram



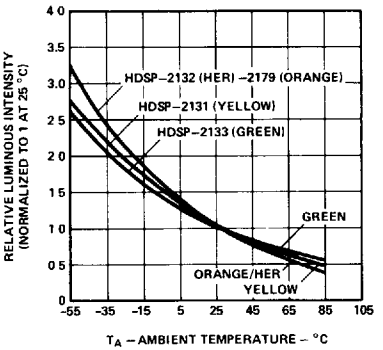
INPUT PULSE LEVELS 0 6 V TO 2 4 V
OUTPUT REFERENCE LEVELS. 0.8 V TO 2 2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pF

Character Font

(Not to Scale)



Relative Luminous Intensity vs. Temperature



HERMETIC DISPLAYS

Electrical Description

Pin Function

RESET ($\overline{RST}$, pin 5) — Reset initializes the display.

FLASH ($\overline{FL}$, pin 27) — $\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.

ADDRESS INPUTS (A_0-A_4, pins 28-32) — Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

$\overline{FL}$	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address Register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word Register	Don't Care
1	1	1	Character RAM	Character Address

CLOCK SELECT (CLS, pin 1) — This input is used to select either an internal or external clock source.

CLOCK INPUT/OUTPUT (CLK, pin 2) — Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.

WRITE ($\overline{WR}$, pin 3) — Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.

CHIP ENABLE ($\overline{CE}$, pin 4) — This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.

READ ($\overline{RD}$, pin 6) — Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.

DATA Bus (D_0-D_7, pins 11-14, 19-22) — The Data bus is used to read from or write to the display.

$GND_{(SUPPLY)}$ (pin 17) — This is the analog ground for the LED drivers.

$GND_{(LOGIC)}$ (pin 18) — This is the digital ground for internal logic.

$V_{DD(POWER)}$ (pin 16) — This is the positive power supply input.

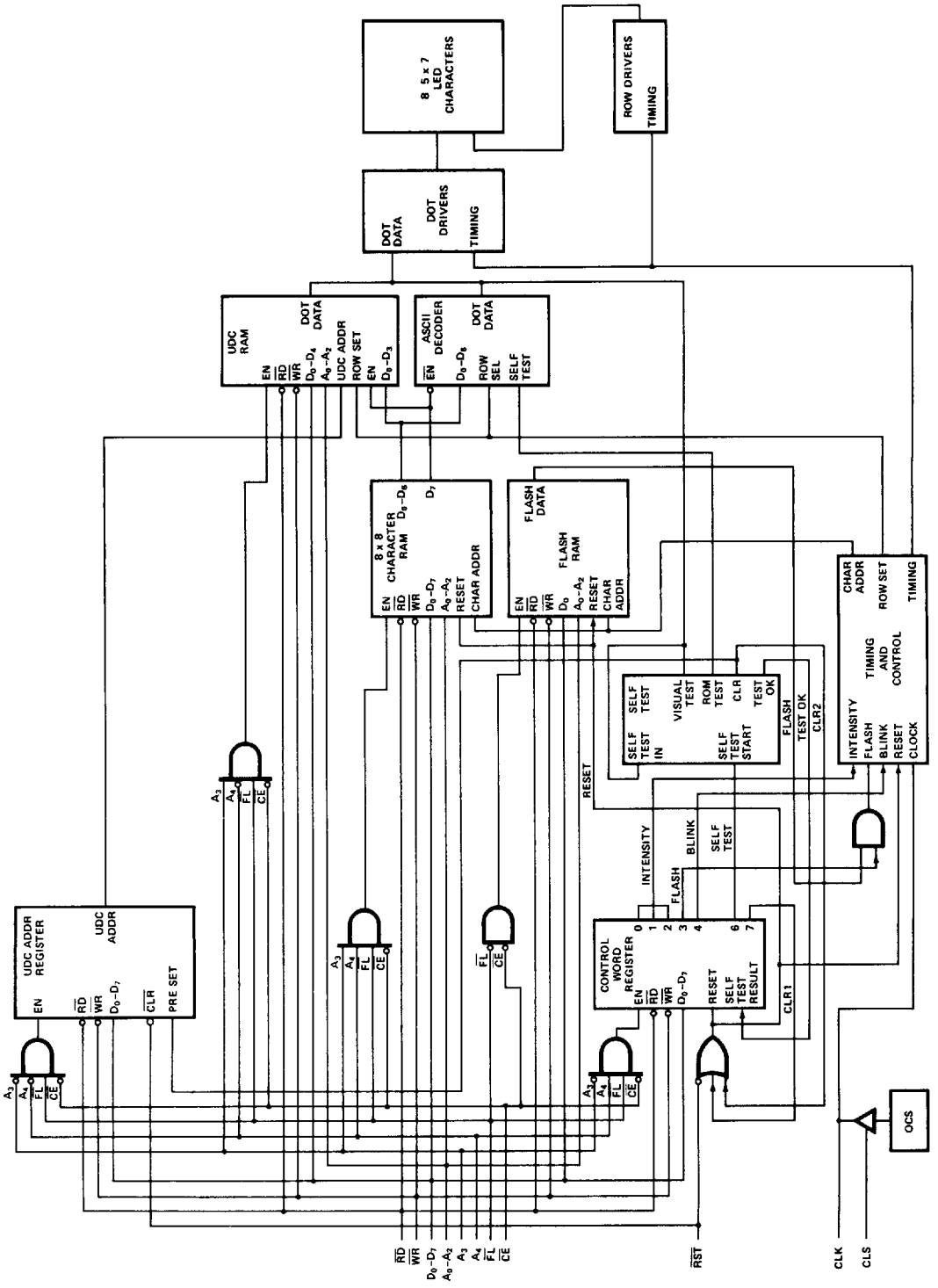


Figure 1. HDSP-213X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-213X display. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register, and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-213X Character RAM. During a normal access the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the Address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D_7 is used to differentiate between an ASCII character and a UDC RAM address. D_7 = 0 enables the ASCII decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII data and D_0-D_3 are used to input a UDC address.

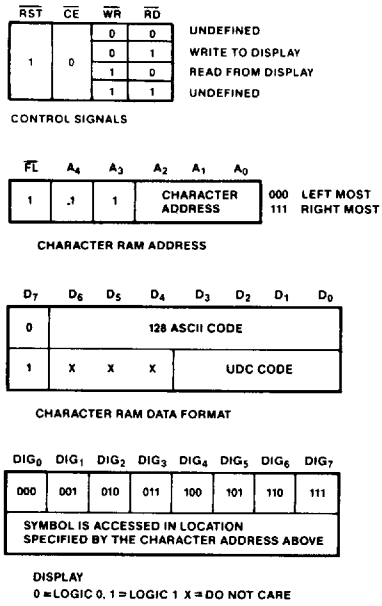


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

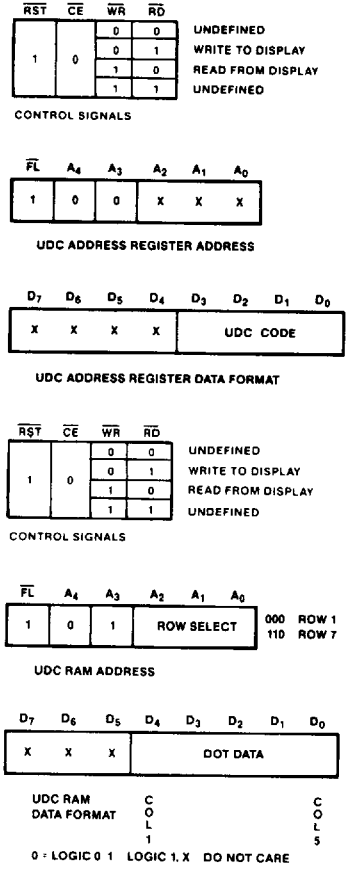


Figure 3. Logic Levels to Access a UDC Character.

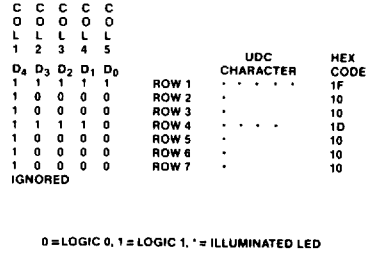
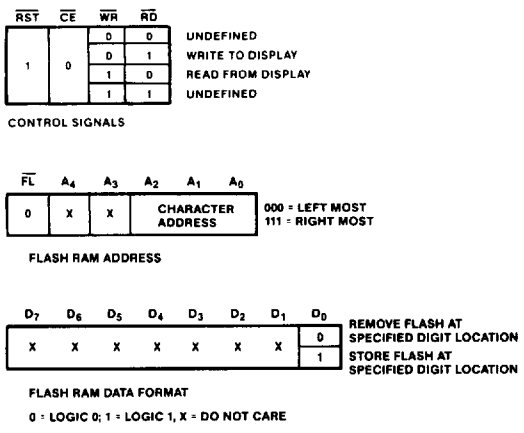


Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.



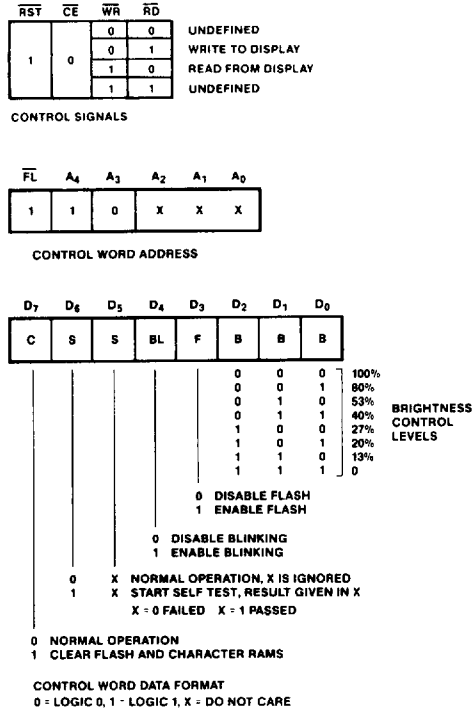


Figure 5. Logic Levels to Access the Flash RAM.

Figure 6. Logic Levels to Access the Control Word Register

Control Word Register

Figure 6 shows how to access the Control Word Register. This is an eight bit register which performs five functions. They are Brightness control, Flash RAM control, Blinking, Self Test and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels

Symbol	D_2	D_1	D_0	% Brightness	25°C Typical	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems see the Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see the Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercises major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF $\overline{RST}$, $\overline{CE}$ AND $\overline{WR}$ ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-213X is a 32 pin dual-in-line package with 24 external pins, which can be stacked horizontally and vertically to create arrays of any size. The HDSP-213X is designed to operate continuously from -55°C to +85°C with a maximum of 20 dots ON per character. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-213X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a ceramic substrate. A glass window is placed over the ceramic substrate creating an air gap over the LED wire bonds. A second glass window creates an air gap over the CMOS IC. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering and visual inspection of the IC.

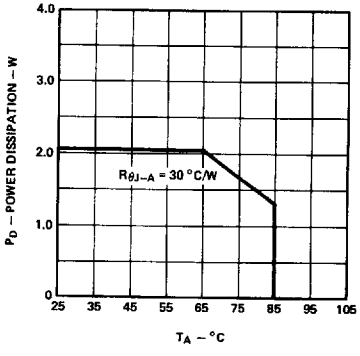


Figure 8. Maximum Power Dissipation vs. Ambient Temperature Derating Based on T_JMAX = 125°C.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-213X should be stored in antistatic packages or conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Thermal Considerations

The HDSP-213X has been designed to provide a low thermal resistance path from the CMOS IC to the 24 package pins. This heat is then typically conducted through the traces of the user's printed circuit board to free air. For most applications no additional heatsinking is required.

The maximum operating IC junction temperature is 150°C. The maximum IC junction temperature can be calculated using the following equation:

$$T_J(IC)\ MAX = T_A + (P_D MAX)\ (R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A})$$

Where

$$P_D MAX = (V_{DD} MAX)\ (I_{DD} MAX)$$

I_{DD}MAX = 370 mA with 20 dots ON in eight character locations at 25°C ambient. This value is from the Electrical Characteristics table.

$$P_D MAX = (5.5\ V)(0.370\ A) = 2.04\ W$$

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnects between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

ESD Susceptibility

These displays have ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C.

Soldering and Post Solder Cleaning Instructions for the HDSP-213X

The HDSP-213X may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling temperature is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

An aqueous cleaning process may be used. A saponifier, such as Kester Bio-Kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temper-

ature is 60°C (140°F). The maximum cumulative exposure of the HDSP-213X to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-213X series displays are readable daylight ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications* for information on contrast enhancement for daylight ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HDSP-2131, HDSP-2179 and HDSP-2133 may be used in night vision lighting applications. The HDSP-2131 (yellow), HDSP-2179 (orange) displays are used as master caution and warning indicators. The HDSP-2133 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting.* An external dimming circuit must be used to dim these displays to night vision lighting levels to meet NVIS radiance requirements. Refer to AN 1039 *Dimming HDSP-213X Displays to Meet Night Vision Lighting Levels.*

100% Screening
Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7512-52
2. High Temperature Storage	1032	T_A = 125°C[3], Time = 24 hours
3. Temperature Cycling	1051	Condition B[4], 10 cycles, 15 minute dwell
4. Constant Acceleration	2006	10,000 Gs at Y_1 & Y_2 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[5]
7. Interim Electrical/ Optical Tests[2]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{DD} = 5.5 V, cycle through character set 1 per second, T_A = +85°C, Time = 160 hours
9. Final Electrical Test[2]	—	Same as step 7
10. Delta Determinations	—	I_{DD}(V) & I_{DD}(#) = ±10%, I_V = -20%
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. T_A = +100°C for HDSP-2133.
4. T_A = -55°C to +100°C for HDSP-2133.
5. Fluid temperature = +100°C for HDSP-2133.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V, and function test	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B Electrical Tests – MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device 0 Failures
Subgroup 2[2,3] Solderability[7]	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock Temperature Cycle	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[8]	
Electrical/Optical Endpoints[5]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V & function, T_A = 25°C	
Subgroup 4 Operating Life Test 340 hrs	1027	T_A = +85°C @ V_{DD} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-Operating Storage Life Test 340 hrs	1032	T_A = +125°C[9]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

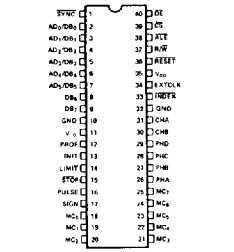
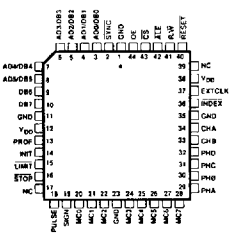
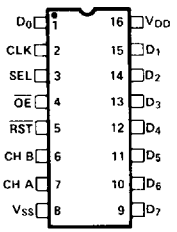
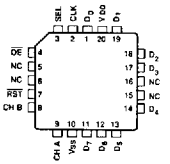
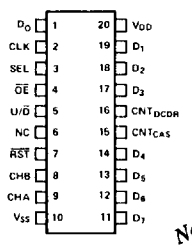
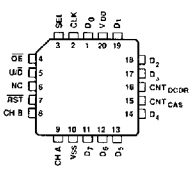
Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions as per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.
7. The steam aging is not performed on gold plated leads.
8. Fluid temperature = +100°C for HDSP-2133.
9. T_A = +100°C for HDSP-2133.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1[1] Physical Dimensions	2066		2 Devices 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3 Shock	2016	1500 G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1, Y_2 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function, T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 C = 0
Subgroup 6 Operating Life Test[6]	1026	T_A = +85°C at V_{DD} = 5.5 V	λ = 10
Electrical/Optical Endpoints[6]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for three cycles.
10. Fluid temperature = +100°C for HDSP-2133.

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61