HI-3182PSx-N, HI-3185PSx-N

ARINC 429 DIFFERENTIAL LINE DRIVER

August 2006

GENERAL DESCRIPTION

The HI-3182, and HI-3185 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications. In addition to being functional upgrades of Holt's HI-8382 product, they are also alternate sources for a variety of similar line driver products from other manufacturers.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-318X series of products to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

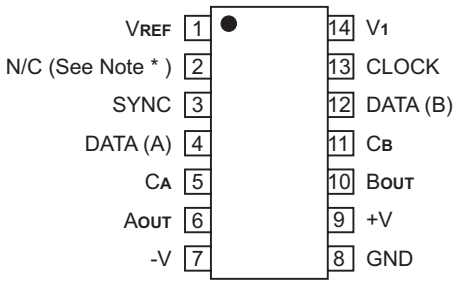
The differential outputs of the HI-318X series of products are programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. A 37.5 ohm resistor is in series with each ARINC output. In addition the HI-3182 product also has a fuse in series with each output.

The HI-318X series of line drivers are intended for use where logic signals must be converted to ARINC 429 levels such as when using an ASIC, the HI-8584/HI-3282/HI-8282A ARINC 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC Interface Device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information.

FEATURES

- Low power CMOS
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Operates at data rates up to 100 Kbits
- Overvoltage protection
- Industrial and Military temperature ranges

PIN CONFIGURATION (Top View)



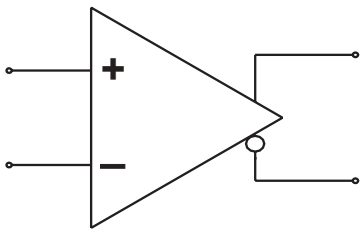
HI-3185PSx-N

14 - PIN PLASTIC SMALL OUTLINE (SOIC) NB

Note: * Pin 2 is internally not connected

(See Page 5 for HI-3182PSx-N package pin configurations)

FUNCTION



ARINC 429 DIFFERENTIAL LINE DRIVER

TRUTH TABLE

SYNC	CLOCK	DATA(A)	DATA(B)	AOUT	BOUT	COMMENTS
X	L	X	X	0V	0V	NULL
L	X	X	X	0V	0V	NULL
H	H	L	L	0V	0V	NULL
H	H	L	H	-VREF	+VREF	LOW
H	H	H	L	+VREF	-VREF	HIGH
H	H	H	H	0V	0V	NULL

FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input (figure 2). Each logic input is TTL/CMOS compatible.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-318X; typically +15V, -15V and +5V. The chip also works with ±12V supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal 2V**REF**. If a value of V**REF** other than +5V is needed, a separate +5V power supply is required for pin V**1**.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, A**OUT** will switch to the +V**REF** rail and B**OUT** will switch to the -V**REF** rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to 0V (ARINC NULL state).

The driver output impedance, R**OUT**, is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the C**A** and C**B** input pins. Typical values for high-speed operation (100KBPS) are C**A** = C**B** = 75pF and for low-speed operation (12.5 to 14KBPS) C**A** = C**B** = 500pF.

The C**A** and C**B** pins swing between +5V and ground allowing the switching of capacitor values with an external single-supply analog switch.

The ARINC outputs of the HI-3182, are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125μs).

The Vref pin has an internal pull-up resistor to V+, allowing the use of a simple external zener diode to set the reference voltage.

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.

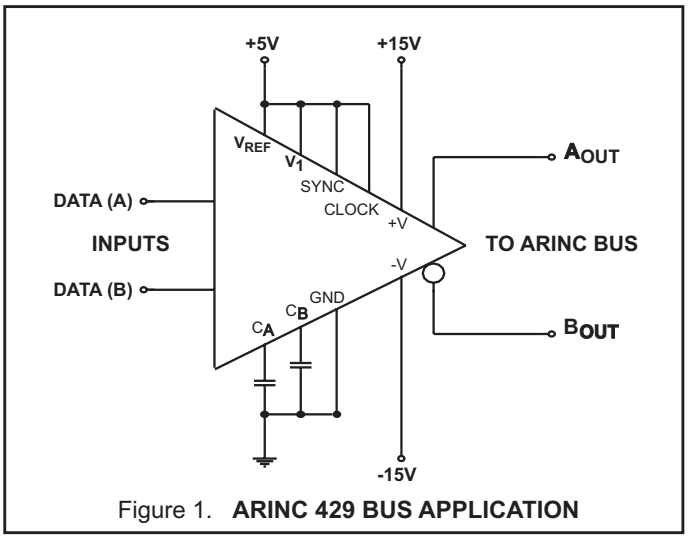


Figure 1. **ARINC 429 BUS APPLICATION**

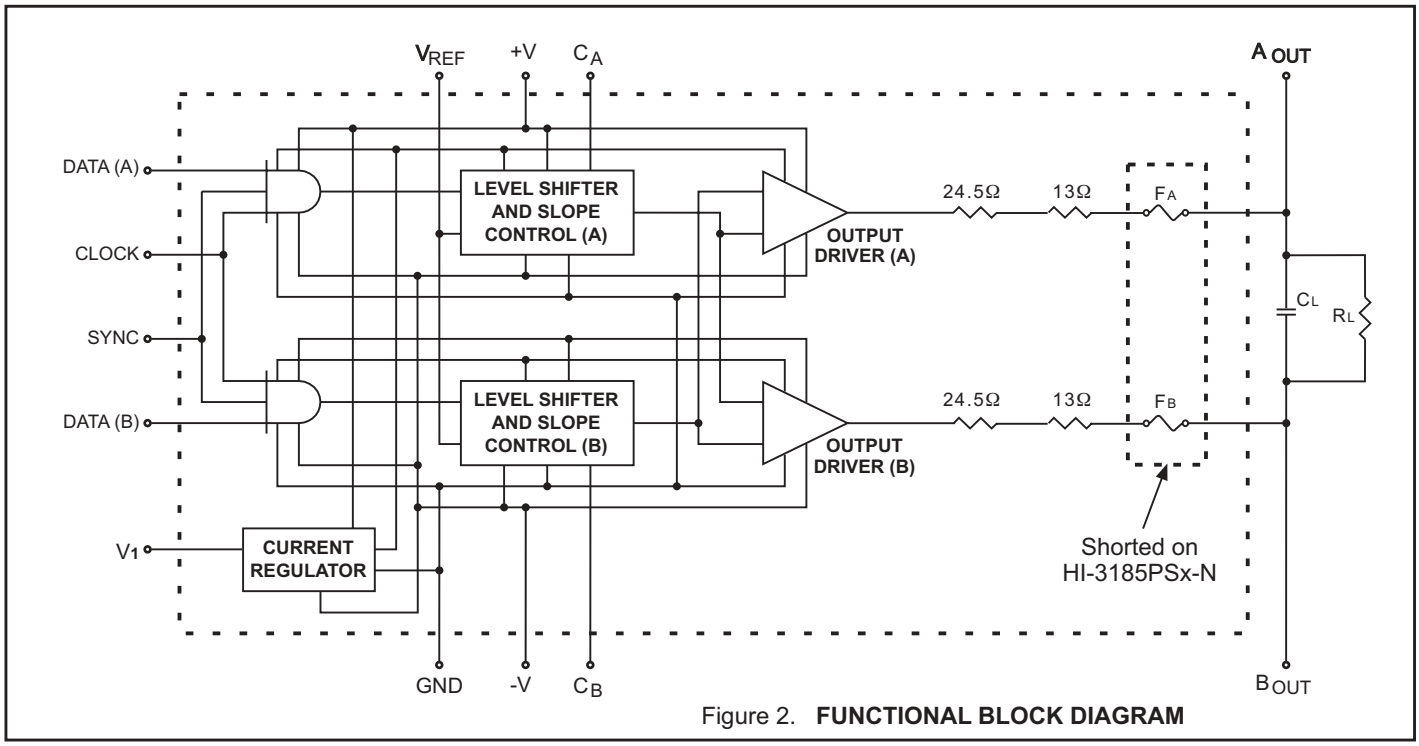


Figure 2. **FUNCTIONAL BLOCK DIAGRAM**

PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
V_{REF}	ANALOG	Ref. voltage used to determine output voltage swing. Pin sources current to allow use of a zener reference.
SYNC	INPUT	Synchronizes data inputs
DATA (A)	INPUT	Data input terminal A
C_A	INPUT	Connection for DATA (A) slew-rate capacitor
A_{OUT}	OUTPUT	ARINC output terminal A
-V	POWER	-12V to -15V
GND	POWER	0.0V
+V	POWER	+12V to +15V
B_{OUT}	OUTPUT	ARINC output terminal B
C_B	INPUT	Connection for DATA (B) slew-rate capacitor
DATA (B)	INPUT	Data input terminal B
CLOCK	INPUT	Synchronizes data inputs
V_1	POWER	+5V ±5%

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	V_{DIF}	Voltage between +V and -V terminals		40	V
Supply Voltage	+V -V V_1		+10.8 to +16.5 -10.8 to -16.5 +5 ±5%	 +7	V V V
Voltage Reference	V_{REF}	For ARINC 429 For Applications other than ARINC	+5 ±5% 1.5 to 6	6 6	V V
Input Voltage Range	V_{IN}			$\geq$ GND -0.3 $\leq$ V1 +0.3	V V
Output Short-Circuit Duration		See Note: 1			
Output Overvoltage Protection		See Note: 2			
Operating Temperature Range	T_A	High-temp & Military Industrial	-55 to +125 -40 to +85		°C °C
Storage Temperature Range	T_{STG}	Ceramic & Plastic	-65 to +150		°C
Lead Temperature		Soldering, 10 seconds		+275	°C
Junction Temperature	T_J			+175	°C

Note 1. Heatsinking may be required for continuous Output Short Circuit at +125°C and for 100KBPS at +125°C.
Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-3182 only)

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_1 = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Current +V (Operating)	I_{CCOP} (+V)	No Load (0 - 100KBPS)			+16	mA
Supply Current -V (Operating)	I_{CCOP} (-V)	No Load (0 - 100KBPS)	-16			mA
Supply Current V_1 (Operating)	I_{CCOP} (V_1)	No Load (0 - 100KBPS)			500	µA
Reference Pin Current V_{REF} (Operating)	I_{CCOP} (V_{REF})	No Load, VREF = 5V (0 - 100KBPS)	-1.0	-0.4	-0.15	mA
Supply Current +V (During Short Circuit Test)	I_{SC} (+V)	Short to Ground (See Note: 1)			150	mA
Supply Current -V (During Short Circuit Test)	I_{SC} (-V)	Short to Ground (See Note: 1)	-150			mA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to Ground V_{MIN}=0 (See Note: 2)			-80	mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to Ground V_{MIN}=0 (See Note: 2)	+80			mA
Input Current (Input High)	I_{IH}				1.0	µA
Input Current (Input Low)	I_{IL}		-1.0			µA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.5	V
Output Voltage High (Output to Ground)	V_{OH}	No Load (0 -100KBPS)	+V_{REF} -.25		+V_{REF} +.25	V
Output Voltage Low (Output to Ground)	V_{OL}	No Load (0 -100KBPS)	-V_{REF} -.25		-V_{REF} +.25	V
Output Voltage Null	V_{NULL}	No Load (0-100KBPS)	-250		+250	mV
Input Capacitance	C_{IN}	See Note 1		15		pF

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.
Note 2. Interchangeability of force and sense is acceptable.

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_1 = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Rise Time (A_{OUT}, B_{OUT})	t_R	C_A = C_B = 75pF See Figure 3.	1.0		2.0	µs
Fall Time (A_{OUT}, B_{OUT})	t_F	C_A = C_B = 75pF See Figure 3.	1.0		2.0	µs
Propagtion Delay Input to Output	t_{PLH}	C_A = C_B = 75pF See Figure 3.			3.0	µs
Propagtion Delay Input to Output	t_{PHL}	C_A = C_B = 75pF See Figure 3.			3.0	µs

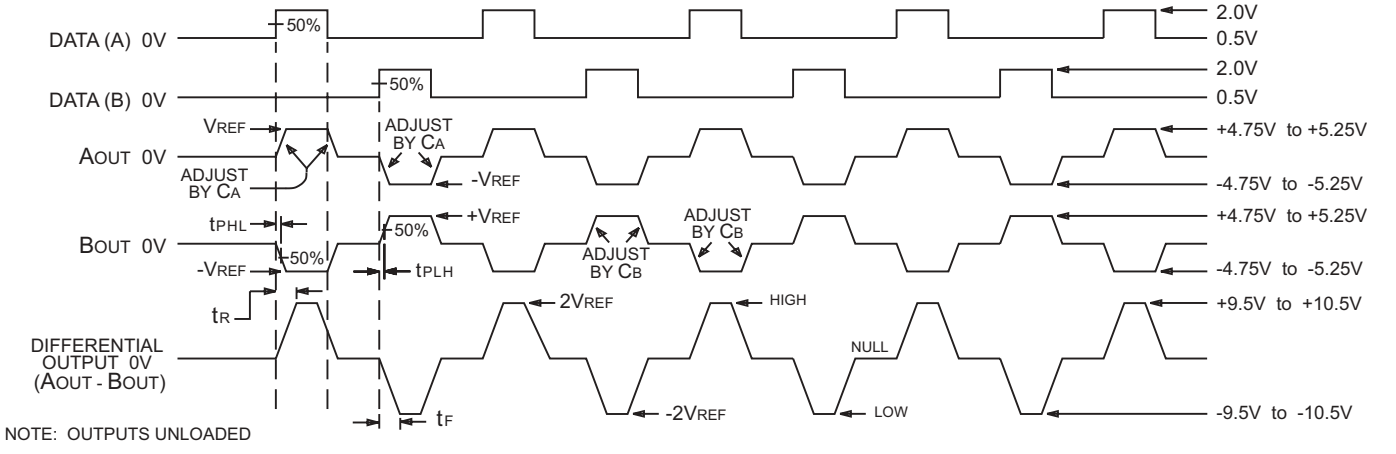
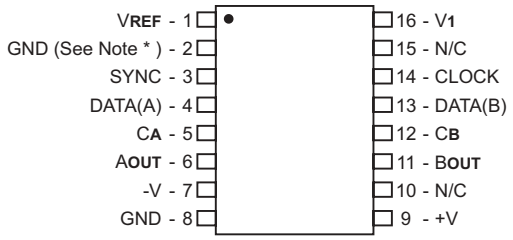


Figure 3. **SWITCHING WAVEFORMS**

ADDITIONAL PIN CONFIGURATIONS (See page 1 for 14-Pin Small Outline SOIC)

HI-3182PSx-N



Notes: * Pin 2 may be left floating

16 - PIN PLASTIC SMALL OUTLINE (SOIC)

ORDERING INFORMATION

HI - 318xPS x x - N

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

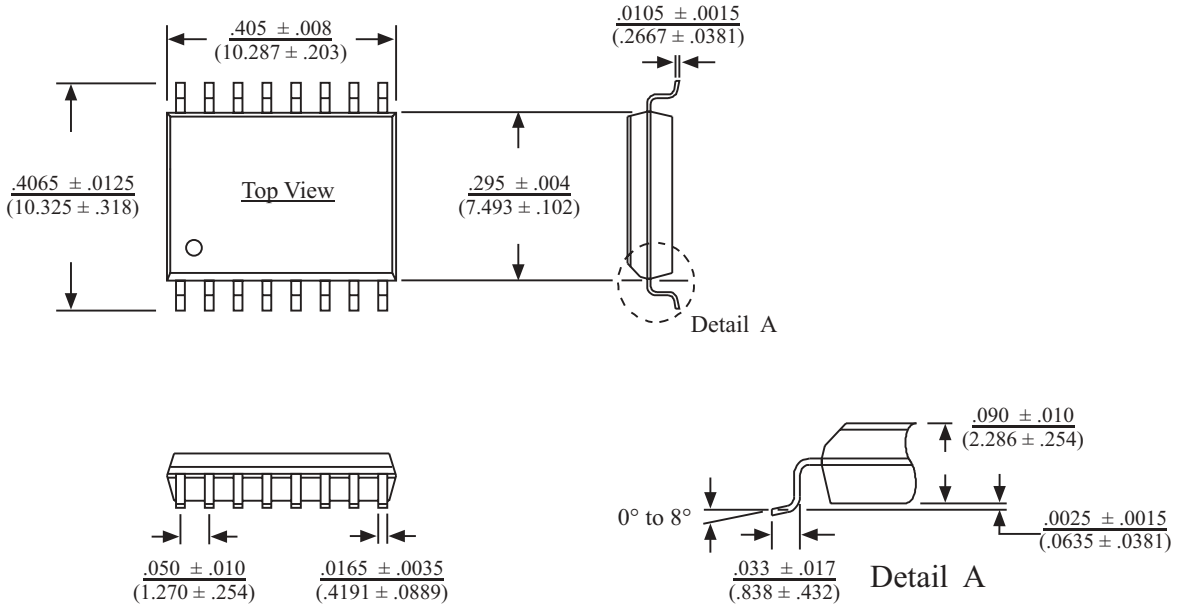
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION	OUTPUT SERIES	
		RESISTANCE	FUSE
3182PS	16 PIN PLASTIC SMALL OUTLINE - WB (SOIC)	37.5 Ohms	Yes
3185PS	14 PIN PLASTIC SMALL OUTLINE - NB (SOIC)	37.5 Ohms	No

Legend: NB - Narrow Body
WB - Wide Body

HI-3182PSx-N
16-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

Package Type: 16HW



HI-3185PSx-N
14-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

Package Type: 14HN