32186 Group

32-BIT RISC MICROCOMPUTER

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Description

The 32186 Group is a 32-bit single-chip RISC microcomputer with built-in flash memory. To accomplish high-precision arithmetic operations, it incorporates a fully IEEE754 compliant, single-precision FPU.
This microcomputer contains a variety of peripheral functions. With the software necessary to run these peripheral functions stored in its large-capacity flash memory, this microcomputer meets the needs of application systems for high functionality, high-performance arithmetic capability, and sophisticated control, thereby adaptation to the embedded applications can be easily configured.

Table 1.0.1 Product List

Type name	ROM capacity	RAM capacity	Frequency	Power supply voltage		Temperature range (Note 1)
				at single-supply	at double-supplies	
M32186F8VFP	1 Mbytes	64 Kbytes	80MHz	5V or 3.3V	5V, 3.3V	-40°C to +125°C

Note 1: This does not guarantee continuous operation and there is a limitation on the length of use (temperature profile).

Features

- CPU .... M32R-FPU core
  (M32R Family common instruction set + single-precision FPU / bit manipulation instructions)
- Pipeline structure .... 6-stage structure
- Instruction set .... 100 discrete instructions / 6 addressing modes
- Instruction format .... 6 bit/32-bit length
- Built-in multiplier-accumulator (DSP function instructions)
- Minimum instruction execution time .... 12.5ns (at f(CPUCLK) = 80 MHz operation)
- Built-in flash memory
- Built-in RAM
- Virtual-flash emulation function .... 8 Kbytes x 8 blocks
- Interrupt controller .... 41 interrupt sources, 8 priority levels
- Wait controller .... can be extended 0-15 wait cycles and external signal for each of 4 areas
- I/O port .... 97 ports (selectable from 3 input levels)
- External interrupt input pin .... 27 pins
- DMAC .... 10 channels
- Multijunction timers (MJT) .... 55 channels
- A/D converter .... 16 channels 10-bit converter (sample & hold x 2)
- Serial interface .... 4 channels (clock synchronous/asynchronous), 2 channels (clock synchronous)
- CAN (CAN Specification 2.0B active) .... 2 channels, each having 32 message slots
- Direct RAM Interface (DRI)
- Real-time debugger (RTD)
- Non-Break Debug (NBD)
- JTAG (boundary scan function)
- Debug interface common to the M32R Family (SDI: Scalable Debug Interface)
- Package .... 144 pin LQFP (0.5mm pitch)

Applications

Automobile equipment control (e.g., Engine, ABS, AT, CCD, and Radar sensing applications), industrial equipment system control, and high-function OA equipment (e.g., PPC)

Since this group is under development, its specifications are subject to change.

1.1 Outline of the 32186 Group

1.1.1 M32R Family CPU Core with Built-in FPU (M32R-FPU)

(1) Based on a RISC architecture

- The 32186 group (hereafter simply the 32186) is a 32-bit RISC single-chip microcomputer. The M32R-FPU incorporates a fully IEEE 754-compliant, single-precision FPU in order to materialize the common instruction set and the high-precision arithmetic operation of the M32R CPU. The 32186 products are built around the M32R-FPU and incorporates flash memory, RAM and various peripheral functions, all integrated into a single chip.
- The M32R-FPU is constructed based on a RISC architecture. Memory is accessed using load/store instructions, and various arithmetic/logic operations are executed using register-to-register operation instructions.
- The M32R-FPU internally contains sixteen 32-bit general-purpose registers. The instruction set consists of 100 discrete instructions in total (83 instructions common to the M32R family plus 17 FPU and extended instructions). These instructions are either 16 bits or 32 bits long.
- In addition to the ordinary load/store instructions, the M32R-FPU supports compound instructions such as Load & Address Update and Store & Address Update. These instructions help to speed up data transfers.

(2) Six-stage pipelined processing

- The M32R-FPU supports six-stage pipelined instruction processing. Not just load/store instructions and register-to-register operation instructions, but also floating-point arithmetic instructions and compound instructions such as Load & Address Update and Store & Address Update are executed in one CPUCLK period (which is equivalent to 12.5 ns when f(CPUCLK) = 80 MHz).
- Although instructions are supplied to the execution stage in the order in which they were fetched, it is possible that if the load/store instruction supplied first is extended by wait cycles inserted in memory access, the subsequent register-to-register operation instruction will be executed before that instruction. Using such a facility, which is known as the “out-of-order-completion” mechanism, the M32R-FPU is able to control instruction execution without wasting clock cycles.

(3) Compact instruction code

- The M32R-FPU supports two instruction formats: one 16 bits long, and one 32 bits long. Use of the 16-bit instruction format especially helps to suppress the code size of a program.
- Moreover, the availability of 32-bit instructions makes programming easier and provides higher performance at the same clock speed than in architectures where the address space is segmented. For example, some 32-bit instructions allow control to jump to an address 32 Mbytes forward or backward from the currently executed address in one instruction, making programming easy.

1.1.2 Built-in Multiplier/Accumulator

(1) Built-in high-speed multiplier

- The M32R-FPU contains a 32 bits × 16 bits high-speed multiplier which enables the M32R-FPU to execute a 32 bits × 32 bits integral multiplication instruction in three CPUCLK periods.

(2) DSP-comparable multiply-accumulate instructions

- The M32R-FPU supports the following four types of multiply-accumulate instructions (or multiplication instructions) which each can be executed in one CPUCLK period using a 56-bit accumulator.

(1) 16 high-order bits of register × 16 high-order bits of register
(2) 16 low-order bits of register × 16 low-order bits of register
(3) All 32 bits of register × 16 high-order bits of register
(4) All 32 bits of register × 16 low-order bits of register

- The M32R-FPU has some special instructions to round the value stored in the accumulator to 16 or 32 bits or shift the accumulator value before storing in a register to have its digits adjusted. Because these instructions too are executed in one CPUCLK period, when used in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update, they enable the M32R-FPU to exhibit superior data processing capability comparable to that of a DSP.

1.1.3 Built-in Single-precision FPU

- The M32R-FPU supports single-precision floating-point arithmetic fully compliant with IEEE 754 standards. Specifically, five exceptions specified in IEEE 754 standards (Inexact, Underflow, Division by Zero, Overflow and Invalid Operation) and four rounding modes (round to nearest, round toward 0, round toward + Infinity and round toward – Infinity) are supported. What's more, because general-purpose registers are used to perform floating-point arithmetic, the overhead associated with transferring the operand data can be reduced.

1.1.4 Built-in Flash Memory and RAM

- The 32186 contains a RAM that can be accessed with zero wait state, allowing to design a high-speed embedded system.

- The internal flash memory can be written to while mounted on a printed circuit board (on-board writing). Use of flash memory facilitates development work, because the chip used at the development stage can be used directly in mass-production, allowing for a smooth transition from prototype to mass-production without the need to change the printed circuit board.

- The internal flash memory can be rewritten as many as 100 times.

- The internal flash memory has a virtual flash emulation function, allowing the internal RAM to be superficially mapped into part of the internal flash memory. When combined with the internal Real-Time Debugger (RTD) and the M32R family's common debug interface (Scalable Debug Interface or SDI), this function makes the ROM table data tuning easy.

- The internal RAM can be accessed for reading or rewriting data from an external device independently of the M32R-FPU by using the Real-Time Debugger. The external device is communicated using the Real-Time Debugger's exclusive clock-synchronous serial interface.

1.1.5 Built-in Clock Frequency Multiplier

- The 32186 contains a clock frequency multiplier, which is schematically shown in Figure 1.1.1 below.

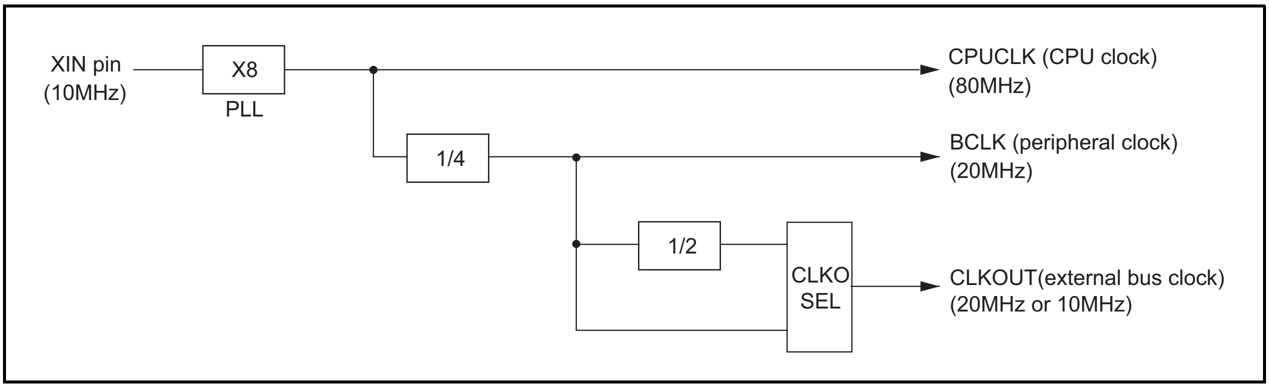

Figure 1.1.1 Conceptual Diagram of the Clock Frequency Multiplier

Table 1.1.1 Clock

Functional Block	Features
CPUCLK	• CPU clock: Defined as f(CPUCLK) when it indicates the operating clock frequency for the M32R-FPU core, internal flash memory and internal RAM.
BCLK	• Peripheral clock: Defined as f(BCLK) when it indicates the operating clock frequency for the internal peripheral I/O and external data bus.
Clock output	• BCLK pin output: A clock with the same frequency as f(BCLK) is output from this pin. • CLKOUT pin output: A clock with the same or half frequency as f(BCLK) is output from this pin.

1.1.6 Powerful Peripheral Functions Built-in

(1) 8-level interrupt controller (ICU)
(2) 10-channel DMAC
(3) 55-channel Multijunction timers (MJT)
(4) 16-channel A/D converter (ADC)
(5) 6-channel serial interface (SIO)
(6) 2-channel Full-CAN
(7) Direct RAM interface (DRI)
(8) Real-time debugger (RTD)
(9) Non-break debug (NBD)
(10) Wait controller
(11) M32R family's common debug function (Scalable Debug Interface or SDI)

1.2 Block Diagram

Figure 1.2.1 shows a block diagram of the 32186. The features of each block are described in Table 1.2.1.

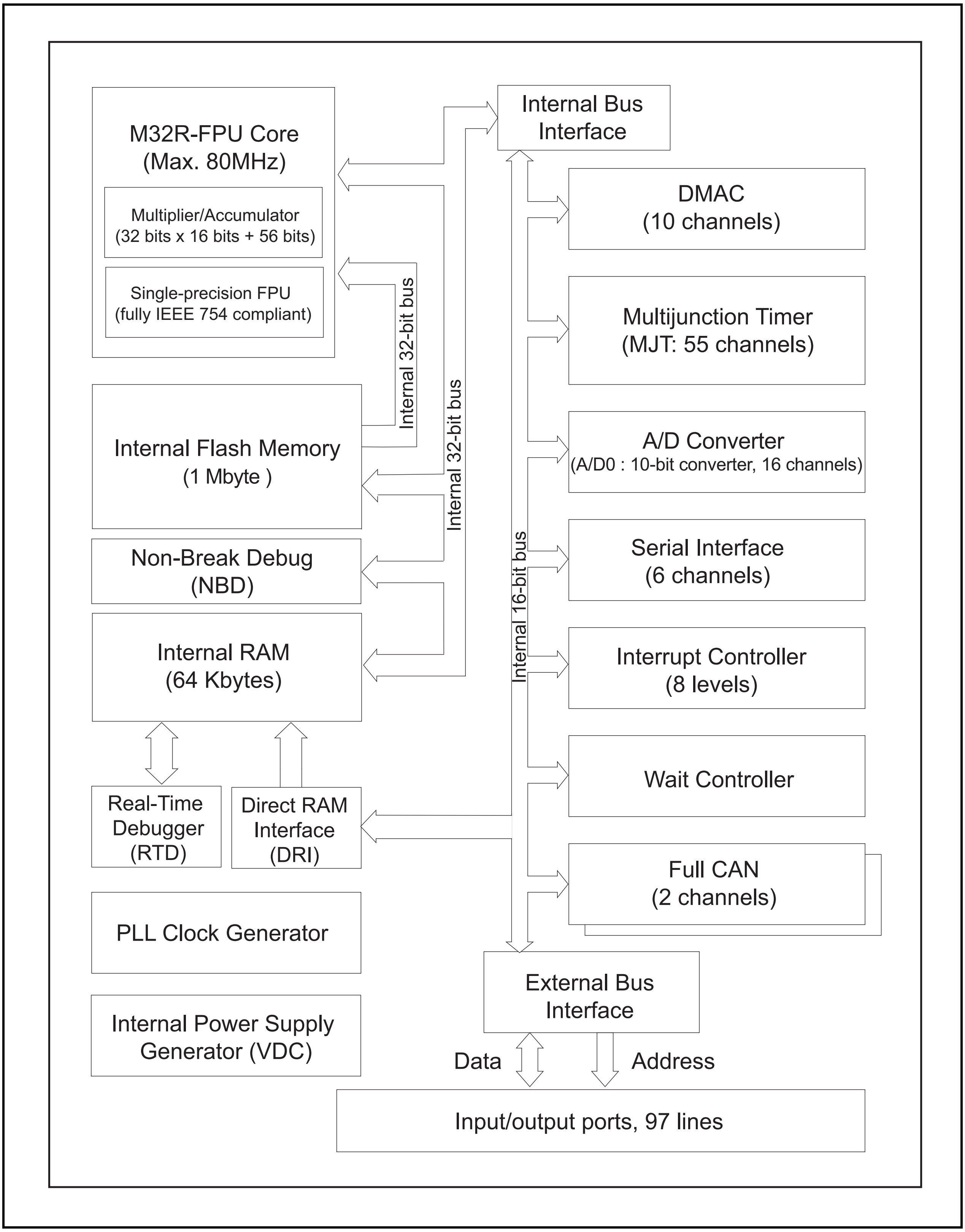

Figure 1.2.1 Block Diagram of the 32186

Table 1.2.1 Features of the 32186 (1 / 2)

Functional Block	Features
M32R-FPU CPU core	• Implementation: six-stage pipelined instruction processing • Internal 32-bit structure of the core • Register configuration General-purpose registers: 32 bits × 16 registers Control registers: 32 bits × 6 registers • Instruction set 16 and 32-bit instruction formats 100 discrete instructions and six addressing modes • Internal multiplier/accumulator (32 bits × 16 bits + 56 bits) • Internal single-precision floating-point arithmetic unit (FPU)
Internal flash memory	• Capacity: 1 Mbyte (1,024 Kbytes), accessible with one wait state • Durability: Rewritable 100 times
Internal RAM	• Capacity: 64 Kbytes, accessible with zero wait state • The internal RAM can be accessed for reading or rewriting data from the outside independently of the M32R-FPU by using the Real-Time Debugger, without ever causing the CPU performance to decrease.
Bus specification	• Fundamental bus cycle: 12.5 ns (when f(CPUCLK) = 80 MHz) • Logical address space: 4 Gbytes linear • Internal bus specification: Internal 32-bit data bus (for CPU <-> internal flash memory and RAM access)(or accessed in 64 bits when accessing the internal flash memory for instructions) : Internal 16-bit data bus (for internal peripheral I/O access) • External extension area: During processor mode: maximum 32 Mbytes During external extension mode: maximum 31 Mbytes (7 Mbytes + 8 Mbytes × 3 blocks) • External data address: 22-bit address • External data bus: 16-bit data bus • Shortest external bus access: 1 CLKOUT during read, 1 CLKOUT during write
Multijunction timer (MJT)	• 55-channel multi-functional timer 16-bit output related timer × 11 channels, 16-bit input/output related timer × 10 channels, 16-bit input related timer × 8 channels, 32-bit input related timer × 8 channels, 16-bit input related up/down timer × 2 channels, and 24-bit output related timer × 16 channels • Flexible timer configuration is possible by interconnecting these timer channels. • Interrupt request: Counter underflow or overflow and rising or falling or both edges or high or low level from the TIN pin (TIN pin can be used as external interrupt inputs irrespective of timer operation.) • DMA transfer request: Counter underflow or overflow and rising or falling or both edges or high or low level from the TIN pin (TIN pin can be used as DMA transfer request inputs irrespective of timer operation.)
DMAC	• Number of channels: 10 • Transfers between internal peripheral I/O's or internal RAM's or between internal peripheral I/O and internal RAM are supported. • Capable of advanced DMA transfers when used in combination with internal peripheral I/O • Transfer request: Software or internal peripheral I/O (A/D converter, MJT, serial interface or CAN) • DMA channels can be cascaded. (DMA transfer on a channel can be started by completion of a transfer on another channel.) • Interrupt request: DMA transfer counter register underflow
A/D converter (ADC)	• 16 channels: 10-bit resolution A/D converter × 1 blocks • Conversion modes: In addition to ordinary A/D conversion modes, the ADC incorporates comparator mode and 2-channel simultaneous sampling mode. • Operation modes: Single conversion mode and n-channel scan mode (n = 1–16) • Sample-and-hold function: Performs A/D conversion with the analog input voltages sampled at start of A/D conversion.

Table 1.2.1 Features of the 32186 (2 / 2)

Functional Block	Features
A/D converter (ADC)	• A/D disconnection detection assist function: Suppresses effects of the analog input voltage leakage from the preceding channel during A/D conversion. • An inflow current bypass circuit is built-in. • Can generate an interrupt or start DMA transfer upon completion of A/D conversion. • Either 8 or 10-bit conversion results can be read out. • Interrupt request: Completion of A/D conversion • DMA transfer request: Completion of A/D conversion
Serial interface (SIO)	• 6-channel serial interface • Can be chosen to be clock-synchronous serial interface or clock-asynchronous serial interface. • Data can be transferred at high speed (2 Mbits per second during clock-synchronous mode or 1.25 Mbits per second during clock-asynchronous mode when f(BCLK) = 20 MHz). • Interrupt request: Reception completed, receive error, transmit buffer empty or transmission completed • DMA transfer request: Reception completed or transmit buffer empty
CAN	• 32 message slots × 2 blocks • Compliant with CAN specification 2.0B active. • Interrupt request: Transmission completed, reception completed, bus error, error-passive, bus-off or single shot • DMA transfer request: Failed to send, transmission completed or reception completed
Real-Time Debugger (RTD)	• Internal RAM can be rewritten or monitored independently of the CPU by entering a command input from the outside. • Comes with exclusive clock-synchronous serial ports. • Interrupt request: RTD interrupt command input
Non-Break Debug (NBD)	• Can access to all resources on the address map from the outside • Clock-synchronous parallel interface (4-bit) • Event output function • RAM monitor function
Direct RAM Interface (DRI)	• Can control capture of clock-synchronous parallel data to the internal RAM independently of the CPU • Clock-synchronous parallel input (8, 16 or 32-bit) • Maximum transfer rate: 20 Mbytes/sec (when f(CPUCLK) = 80 MHz).
Interrupt Controller (ICU)	• Controls interrupt requests from the internal peripheral I/O. • Supports 8-level interrupt priority including an interrupt disabled state. • External interrupt: 27 sources (SBI#, TIN0, TIN3–TIN11, TIN16–TIN27, TIN30–TIN33) • TIN pin input sensing: Rising, falling or both edges or high or low level
Wait Controller	• Controls wait states for access to the external extension area. • Insertion of 0–15 wait states by setting up in software + wait state extension by entering WAIT# signal
PLL	• A multiply-by-8 clock generating circuit
Clock	• External input clock frequency (XIN) is 10.0 MHz. • CPUCLK: Operating clock for the M32R-FPU core, internal flash memory and internal RAM The CPU clock is 80 MHz (when f(XIN) = 10 MHz). • BCLK: Operating clock for the internal peripheral I/O and external data bus The peripheral clock is 20 MHz (peripheral module access when f(XIN) = 10 MHz). • BCLK pin output: A clock with the same frequency as f(BCLK) is output from this pin. • CLKOUT pin output: A clock with the same or half frequency as f(BCLK) is output from this pin.
JTAG	• Boundary scan function
VDC	• Internal power supply generating circuit: Generates the internal power supply from an external power supply (5 or 3.3 V).
Ports	• Input/output pins: 97 pins • The port input threshold can be set in a program to one of three levels individually for each port group (with or without Schmitt circuit, selectable).

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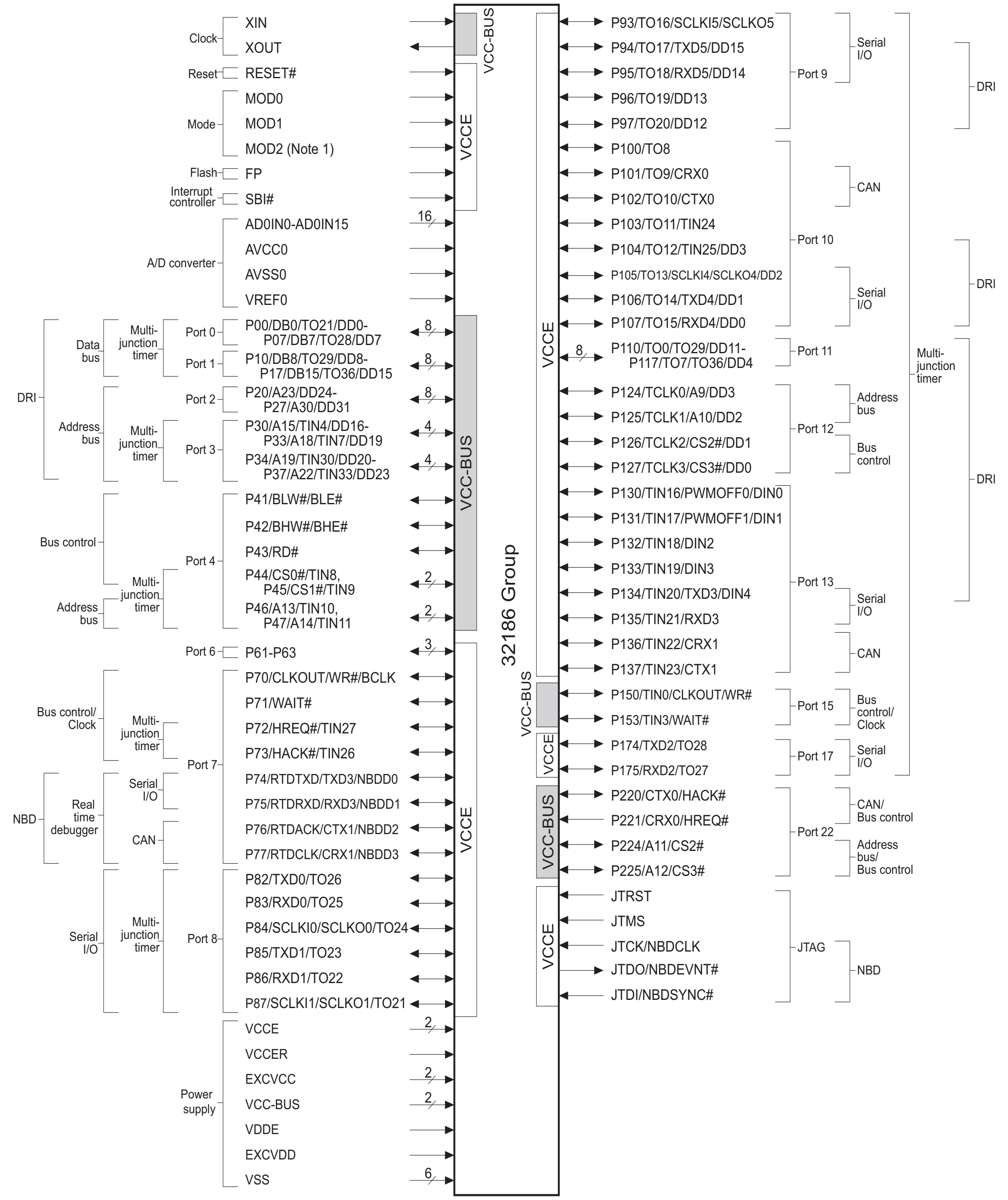
1.3 Pin Functions

Figure 1.3.1 shows the 32186's pin function diagram. Pin functions are described in Table 1.3.1.



Note 1: MOD2 must be connected to the ground (GND).

Notes: · The pin (signal) with "#" at the end of the pin name (signal name) indicates it is a low active pin (signal).

· VCCE : operates with VCCE power supply

VCC-BUS : operates with VCC-BUS power supply

Figure 1.3.1 Pin Function Diagram

Table 1.3.1 Description of Pin Functions (1 / 3)

<table>
<tr><th>Type</th><th>Pin Name</th><th>Signal Name</th><th>Input/Output</th><th>Description</th></tr>
<tr><td>Power supply</td><td>VCCER</td><td>Internal power supply input</td><td>–</td><td>Power supply input for the internal voltage generator circuit (5.0 V ± 0.5 V or 3.3 V ± 0.3 V)</td></tr>
<tr><td></td><td>VCCE</td><td>Port/internal peripheral I/O pin power supply input</td><td>–</td><td>Power supply input for the port and internal peripheral I/O pins (5.0 V ± 0.5 V or 3.3 V ± 0.3 V).
Apply same voltage to the all VCCE pins.</td></tr>
<tr><td></td><td>VCC-BUS</td><td>Port/bus interface pin power supply input</td><td>–</td><td>Power supply input for the port and bus interface pins (5.0 V ± 0.5 V or 3.3 V± 0.3 V).
Apply same voltage to the all VCC-BUS pins.</td></tr>
<tr><td></td><td>VDDE</td><td>RAM power supply</td><td>–</td><td>Backup power supply input for the internal RAM (5.0 V ± 0.5 V or 3.3 V ± 0.3 V).</td></tr>
<tr><td></td><td>VSS</td><td>Ground</td><td>–</td><td>Connect all VSS pins to ground (GND).</td></tr>
<tr><td></td><td>EXCVCC</td><td>VCCER control</td><td>–</td><td>This pin connects an external capacitor for the internal voltage generator circuit.</td></tr>
<tr><td></td><td>EXCVDD</td><td>VDDE control</td><td>–</td><td>This pin connects an external capacitor for the internal power supply of the internal RAM.</td></tr>
<tr><td>Clock</td><td>XIN,
XOUT</td><td>Clock input
Clock output</td><td>Input
Output</td><td>These are clock input/output pins. A PLL-based × 8 frequency multiplier is included, which accepts as input a clock whose frequency is 1/8 of the internal CPU clock frequency. (XIN input is 10 MHz when f(CPUCLK) = 80 MHz.)</td></tr>
<tr><td></td><td>CLKOUT,
BCLK</td><td>System clock</td><td>Output</td><td>The CLKOUT pin outputs a clock that is equal to the external input clock frequency, XIN (i.e., CLKOUT output is 10 MHz when f(CPUCLK) = 80 MHz), or two times of XIN (i.e.,CLKOUT output is 20 MHz when f(CPUCLK) = 80 MHz). This clock is used when operations are synchronous external to the chip.
The BCLK pin outputs a clock that is two times the external input clock frequency, XIN (i.e., BCLK output is 20 MHz when f(CPUCLK) = 80 MHz).</td></tr>
<tr><td>Reset</td><td>RESET#</td><td>Reset</td><td>Input</td><td>Reset input pin for the internal circuit.</td></tr>
<tr><td>Mode</td><td>MOD0 –
MOD2</td><td>Mode</td><td>Input</td><td>Set the microcomputer’s operation mode.
<table>
<tr><th>MOD0</th><th>MOD1</th><th>MOD2</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Single-chip mode</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>External extension mode</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Processor mode (boot mode) (Note 1)</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>(Settings inhibited)</td></tr>
<tr><td>X</td><td>X</td><td>H</td><td>(Settings inhibited)</td></tr>
</table>
X: Don’t care</td></tr>
<tr><td>Flash</td><td>FP</td><td>Flash protect</td><td>Input</td><td>This special pin protects the flash memory against rewrites in hardware.</td></tr>
<tr><td>Address bus</td><td>A9–A30</td><td>Address bus</td><td>Output</td><td>Twenty-two address lines (A9–A30) are included, allowing four blocks each up to 8 MB memory space to be connected external to the chip. A31 is not output.</td></tr>
</table>

Note 1: Boot mode requires that the FP pin should be at the high level.

Table 1.3.1 Description of Pin Functions (2 / 3)

Type	Pin Name	Signal Name	Input/Output	Description
Data bus	DB0–DB15	Data bus	Input/output	This 16-bit data bus is used to connect external devices. When writing in byte units during a write cycle, the output data at the invalid byte position is undefined. During a read cycle, data on the entire 16-bit bus is always read in. However, only the data at the valid byte position is transferred into the internal circuit.
Bus control	CS0#–CS3#	Chip select	Output	These are chip select signals for external devices.
	RD#	Read	Output	This signal is output when reading an external device.
	WR#	Write	Output	This signal is output when writing to an external device.
	BHW#/BLW#	Byte high/low write	Output	When writing to an external device, this signal indicates the valid byte position to which data is transferred. BHW# and BLW# correspond to the upper address side (bits 0–7 are valid) and the lower address side (bits 8–15 are valid), respectively.
	BHE#	Byte high enable	Output	During an external device access, this signal indicates that the high-order data (bits 0–7) is valid.
	BLE#	Byte low enable	Output	During an external device access, this signal indicates that the low-order data (bits 8–15) is valid.
	WAIT#	Wait	Input	When accessing an external device, a low-level input on WAIT# pin extends the wait cycle.
	HREQ#	Hold request	Input	This input pin is used by an external device to request control of the external bus. A low-level input on HREQ# pin places the CPU in a hold state.
	HACK#	Hold acknowledge	Output	This signal notifies that the CPU has entered a hold state and relinquished control of the external bus.
Multijunction timer	TIN0, TIN3–TIN11, TIN16–TIN27, TIN30–TIN33	Timer input	Input	Input pins for the multijunction timer.
	TO0–TO36	Timer output	Output	Output pins for the multijunction timer.
	TCLK0 –TCLK3	Timer clock	Input	Clock input pins for the multijunction timer.
A/D converter	AVCC0	Analog power supply input	–	AVCC0 is the power supply input for the A/D0 converter. Connect AVCC0 to the power supply rail.
	AVSS0	Analog ground	–	AVSS0 is the analog ground for the A/D0 converter. Connect AVSS0 to ground.
	AD0IN0 –AD0IN15	Analog input	Input	16-channel analog input pins for the A/D0 converter.
	VREF0	Reference voltage input	Input	VREF0 is the reference voltage input pin for the A/D0 converter.
Interrupt controller	SBI#	System break interrupt	Input	This is the system break interrupt (SBI) input pin for the interrupt controller.
Serial interface	SCLKI0/SCLKO0, SCLKI1/SCLKO1, SCLKI4/SCLKO4, SCLKI5/SCLKO5	UART transmit/ receive clock output or CSIO transmit/ receive clock input/ output	Input/output	When in UART mode: This pin outputs a clock derived from BRG output by dividing it by 2. When in CSIO mode: This pin accepts as input a transmit/receive clock when external clock is selected or outputs a transmit/receive clock when internal clock is selected.
	TXD0–TXD5	Transmit data	Output	Transmit data output pin for serial interface.
	RXD0–RXD5	Received data	Input	Received data input pin for serial interface.

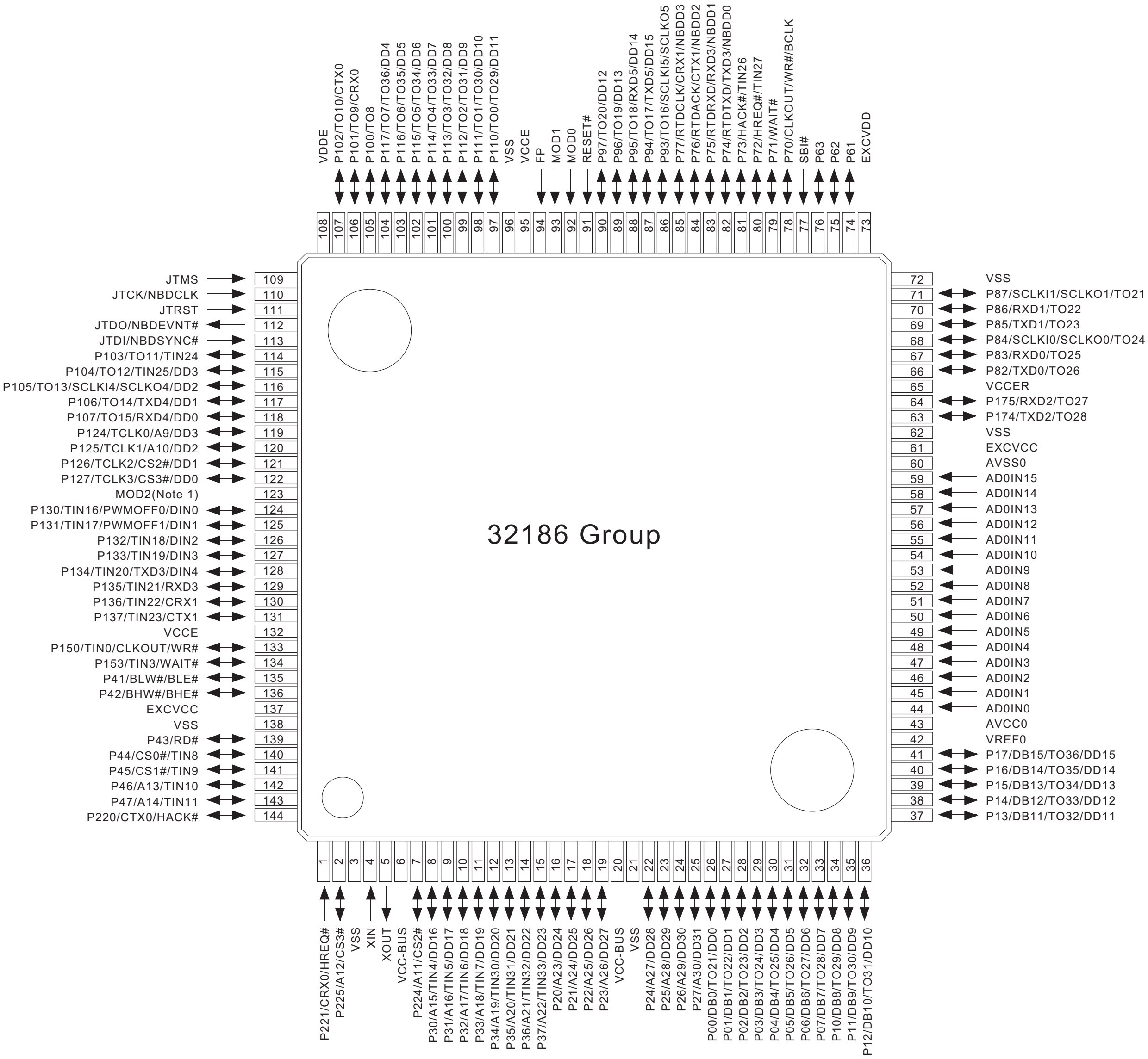
Table 1.3.1 Description of Pin Functions (3 / 3)

Type	Pin Name	Signal Name	Input/Output	Description
Real-time debugger (RTD)	RTDTXD	RTD transmit data	Output	Serial data output pin for the real-time debugger.
	RTDRXD	RTD received data	Input	Serial data input pin for the real-time debugger.
	RTDCLK	RTD clock input	Input	Serial data transmit/receive clock input pin for the real-time debugger.
	RTDACK	RTD acknowledge	Output	A low-level pulse is output from this pin synchronously with the start clock for the real-time debugger's serial data output word. The low-level pulse width indicates the type of command/data received by the real-time debugger.
CAN	CTX0, CTX1	Transmit data	Output	This pin outputs data from the CAN module.
	CRX0, CRX1	Received data	Input	This pin accepts as input the data for the CAN module.
JTAG	JTMS	Test mode select	Input	Test mode select input to control the state transition of the test circuit.
	JTCK	Test clock	Input	Clock input for the debug module and test circuit.
	JTRST	Test reset	Input	Test reset input to initialize the test circuit asynchronously with device operation.
	JTDI	Test data input	Input	This pin accepts as input the test instruction code or test data that is serially received.
	JTDO	Test data output	Output	This pin outputs the test instruction code or test data serially.
NBD	NBDD0 –NBDD3	Command/Address/ Data	Input/output	NBD command, address, and data input/output pins.
	NBDCLK	Synchronizing clock input	Input	NBD synchronizing clock input pin.
	NBDSYNC#	Top of data input	Input	This pin controls the start position of NBD data.
	NBDEVNT#	Event output	Output	This pin is used for event output when an NBD event occurs.
DRI	DD0–DD31	DD input	Input	DRI data input pin.
	DIN0–DIN4	DIN input	Input	DRI event input pin.
Input/output ports (Note 1)	P00–P07	Input/output port 0	Input/output	Programmable input/output port.
	P10–P17	Input/output port 1	Input/output	
	P20–P27	Input/output port 2	Input/output	
	P30–P37	Input/output port 3	Input/output	
	P41–P47	Input/output port 4	Input/output	
	P61–P63	Input/output port 6	Input/output	
	P70–P77	Input/output port 7	Input/output	
	P82–P87	Input/output port 8	Input/output	
	P93–P97	Input/output port 9	Input/output	
	P100–P107	Input/output port 10	Input/output	
	P110–P117	Input/output port 11	Input/output	
	P124–P127	Input/output port 12	Input/output	
	P130–P137	Input/output port 13	Input/output	
	P150, P153	Input/output port 15	Input/output	
	P174, P175	Input/output port 17	Input/output	
	P220, P221 (Note 2), P224, P225	Input/output port 22	Input/output	

Note 1: Input/output ports 5, 14, 16 and 18–21 are nonexistent.
Note 2: P221 is input-only port.

1.4 Pin Assignments

Figure 1.4.1 shows the 32186’s pin assignment diagram.



Package: 144P6Q-A(0.5-mm pitch)

Note 1: MOD2 must be connected to the ground (GND).
Note: • The symbol "#" suffixed to the pin (or signal) names means that the pins (or signals) are active-low.

Figure 1.4.1 **Pin Assignment Diagram (Top View)**

2.1 Outline of the Address Space

The logical addresses of the M32R are always handled in 32 bits, providing a linear address space of up to 4 Gbytes. The address space of the M32R/ECU consists of the following:

(1) User space

- Internal ROM area
- External extension area
- Internal RAM area
- SFR (Special Function Register) area

The 2 Gbytes from the address H’0000 0000 to the address H’7FFF FFFF comprise the user space. Located in this space are the internal ROM area, an external extension area, the internal RAM area and the SFR (Special Function Register) area (in which a set of internal peripheral I/O registers exist). Of these, the internal ROM and external extension areas are located differently depending on mode settings as will be described later.

(2) System space (not open to the user)

The 2 Gbytes from the address H’8000 0000 to the address H’FFFF FFFF comprise the system space. This space (except for SFR area for NBD control) is reserved for use by development tools such as an in-circuit emulator and debug monitor.

2.2 Operation Modes

The microcomputer is placed in one of the following modes depending on how CPU operation mode is set by MOD0 and MOD1 pins.

Table 2.2.1 Operation Mode Settings

MOD0	MOD1	MOD2 (Note 1)	Operation mode
VSS	VSS	VSS	Single-chip mode
VSS	VCCE	VSS	External extension mode
VCCE	VSS	VSS	Processor mode (FP = VSS)
VCCE	VCCE	VSS	(Settings inhibited)
–	–	VCCE	(Settings inhibited)

Note 1: Connect VCCE and VSS to the VCCE input power supply and ground, respectively.

The internal ROM and external extension areas are located differently depending on how operation mode is set. (All other areas in the address space are located the same way.) The following diagram shows how the internal ROM and external extension areas are mapped into the address space in each operation mode.

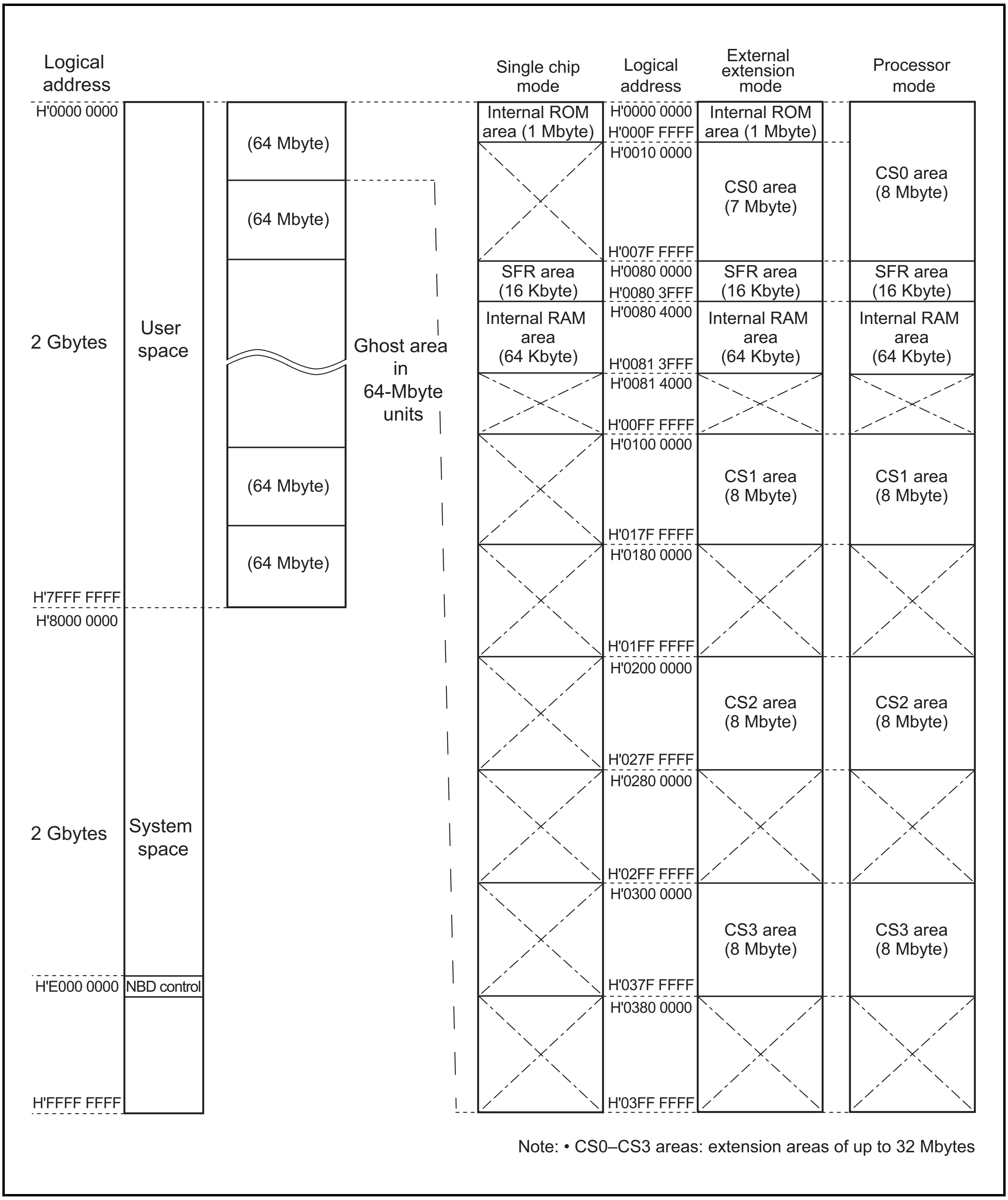


Figure 2.2.1 Address Space

3.1 Outline of the Interrupt Controller

The Interrupt Controller (ICU) manages maskable interrupts from internal peripheral I/Os and a system break interrupt (SBI). The maskable interrupts from internal peripheral I/Os are sent to the M32R CPU as external interrupts (EI).

The maskable interrupts from internal peripheral I/Os are managed by assigning them one of eight priority levels including an interrupt-disabled state. If two or more interrupt requests with the same priority level occur at the same time, their priorities are resolved by predetermined hardware priority. The source of an interrupt request generated in internal peripheral I/Os is identified by reading the relevant interrupt status register provided for internal peripheral I/Os.

On the other hand, the system break interrupt (SBI) is recognized when a low-going transition occurs on the SBI# signal input pin. This interrupt is used for emergency purposes such as when power outage is detected or a fault condition is notified by an external watchdog timer, so that it is always accepted irrespective of the PSW register IE bit status. When the CPU has finished servicing an SBI, shut down or reset the system without returning to the program that was being executed when the interrupt occurred.

Specifications of the Interrupt Controller are outlined below.

Table 3.1.1 Outline of the Interrupt Controller (ICU)

Item	Specification
Interrupt request source	Maskable interrupt requests from internal peripheral I/Os: 40 sources (Note 1) System break interrupt request: 1 source (entered from SBI# pin)
Priority management	8 priority levels including an interrupt-disabled state (However, interrupts with the same priority level have their priorities resolved by fixed hardware priority.)

Note 1: There are actually 256 interrupt request resources in total when counted individually, which are grouped into 40 interrupt request resources.

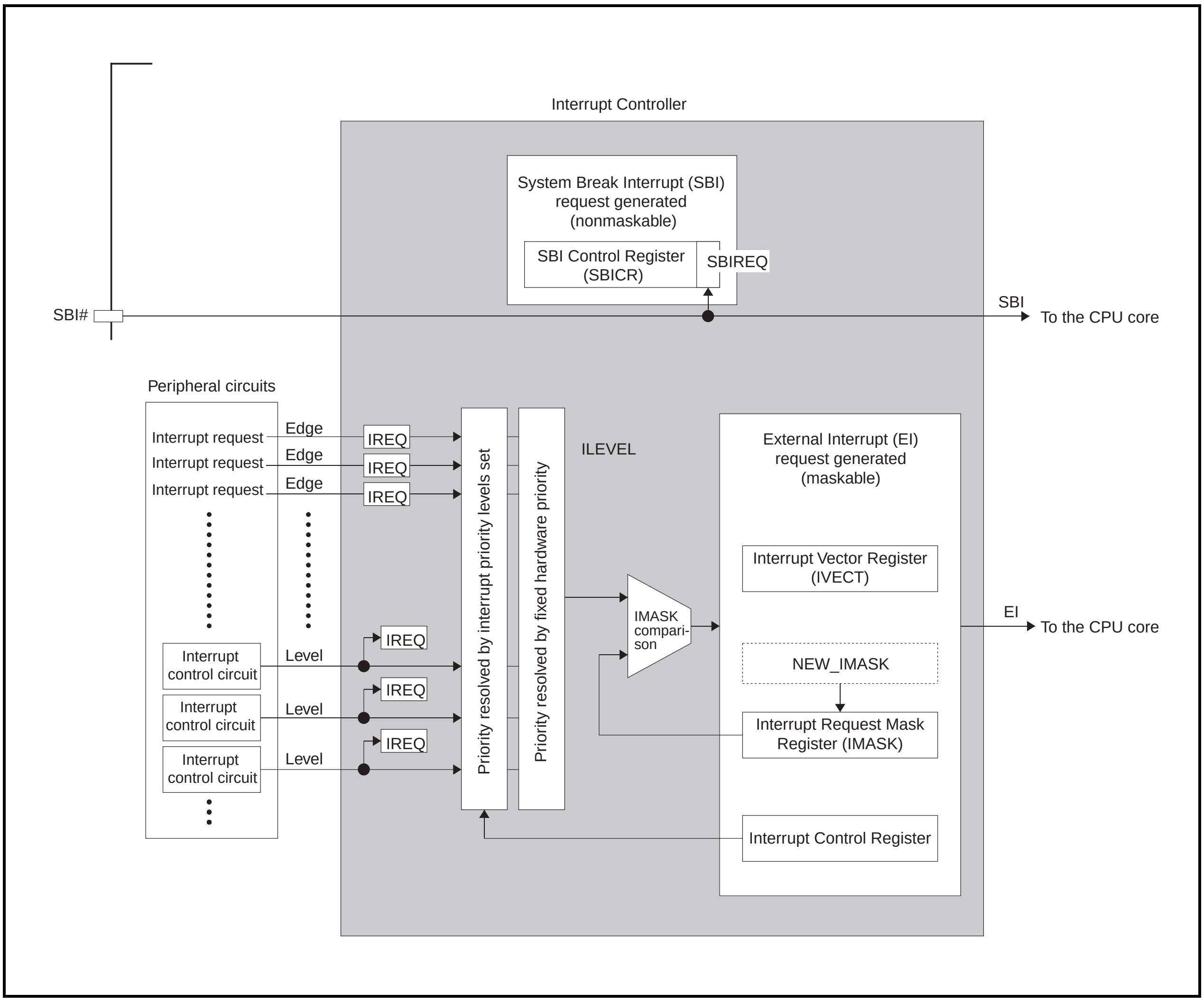


Figure 3.1.1 Block Diagram of the Interrupt Controller

4.1 Outline of Input/Output Ports

The 32186 has a total of 97 input/output ports from P0–P13, P15, P17 and P22 (except P5, which is reserved for future use). These input/output ports can be used as input or output ports by setting the respective direction registers.

Each input/output port has double or triple functions shared with other internal peripheral I/O or external bus interface related signal lines, or multiple functions shared with multi-function peripheral I/Os. Pin functions are selected depending on the operation mode of the CPU or by setting the operation mode register and peripheral function select register for the input/output port. (If any internal peripheral I/O has still another function, it is also necessary to set the register provided for that internal peripheral I/O.)

Abundant port functions are incorporated, including a port input level switching function, port output drive capability setting function, and noise canceller control function.

Note that before any ports can be used in input mode, this port input function enable bit must be set accordingly.

The input/output ports are outlined below.

Table 4.1.1 Outline of Input/Output Ports

Item	Specification
Number of ports	Total 97 ports P0 : P00–P07 (8 ports) P1 : P10–P17 (8 ports) P2 : P20–P27 (8 ports) P3 : P30–P37 (8 ports) P4 : P41–P47 (7 ports) P6 : P61–P63 (3 ports) P7 : P70–P77 (8 ports) P8 : P82–P87 (6 ports) P9 : P93–P97 (5 ports) P10 : P100–P107 (8 ports) P11 : P110–P117 (8 ports) P12 : P124–P127 (4 ports) P13 : P130–P137 (8 ports) P15 : P150, P153 (2 ports) P17 : P174, P175 (2 ports) P22 : P220, P221, P224, P225 (4 ports)
Port function	The input/output ports can individually be set for input or output mode using the direction control register provided for each input/output port. (However, P221 is an input-only port.)
Pin function	Shared with peripheral I/O or external bus interface signals to serve dual-functions (or shared with two or more peripheral I/O functions to serve multiple functions)

Note : • P5, P14, P16, P18-P21 are nonexist.

4.2 Selecting Pin Functions

Each input/output port serves dual functions sharing the pin with other internal peripheral I/O or external bus interface signal lines (or multiple functions sharing the pin with two or more peripheral I/O functions). Pin functions are selected depending on the operation mode of the CPU or by setting the operation mode register and peripheral function select register for the input/output port.

P0–P4, P124, P125, P224 and P225, when the CPU is set to operate in processor mode, all are switched to serve as signal pins for external access. The CPU operation mode is determined depending on how the MOD0 and MOD1 pins are set (see the table below).

Table 4.2.1 CPU Operation Modes and P0–P4, P124, P125, P224 and P225 Pin Functions

MOD0	MOD1	Operation Mode	P0–P4, P124, P125, P224 and P225 Pin Function
VSS	VSS	Single-chip mode	Input/output port pin
VSS	VCCE	External extension mode	Input/output port or external bus interface signal pin (Note 1)
VCCE	VSS	Processor mode	External bus interface signal pin
VCCE	VCCE	(Settings inhibited)	–

Note 1: P41–P43 only function as external bus interface signal pins.

Note : • VCCE and VSS are connected to main power supply and GND, respectively.

Each input/output port has their functions switched between input/output port pins and internal peripheral I/O pins by setting the respective port operation mode and peripheral function select registers. If any internal peripheral I/O has two or more pin functions, use the register provided for that internal peripheral I/O to select the desired pin function.

Note that FP and MOD1 pin operations during internal flash memory programming do not affect the pin functions.

P0–P4: Pin functions are selected by the settings for the port operation mode and port peripheral function select registers

P6–P22: Pin functions are selected by the settings for the port operation mode, port peripheral function select and NBD function select registers

	0	1	2	3	4	5	6	7
P0	TO21 / DD0	TO22 / DD1	TO23 / DD2	TO24 / DD3	TO25 / DD4	TO26 / DD5	TO27 / DD6	TO28 / DD7
P1	TO29 / DD8	TO30 / DD9	TO31 / DD10	TO32 / DD11	TO33 / DD12	TO34 / DD13	TO35 / DD14	TO36 / DD15
P2	DD24	DD25	DD26	DD27	DD28	DD29	DD30	DD31
P3	TIN4 / DD16	TIN5 / DD17	TIN6 / DD18	TIN7 / DD19	TIN30 / DD20	TIN31 / DD21	TIN32 / DD22	TIN33 / DD23
P4		P41 (Port only)	P42 (Port only)	P43 (Port only)	TIN8	TIN9	TIN10	TIN11
P5								
P6		P61 (Port only)	P62 (Port only)	P63 (Port only)	SBI# (Note 1)			
P7	CLKOUT / WR# / BCLK(Note 2)	WAIT#	HREQ# / TIN27	HACK# / TIN26	RTDTXD / TXD3 / NBDD0	RTDRXD / RXD3 / NBDD1	RTDACK / CTX1 / NBDD2	RTDCLK / CRX1 / NBDD3
P8	MOD0 (Note 1)	MOD1 (Note 1)	TXD0 / TO26	RXD0 / TO25	SCLKI0 / SCLKO0 / TO24	TXD1 / TO23	RXD1 / TO22	SCLKI1 / SCLKO1 / TO21
P9				TO16 / SCLKI5 / SCLKO5	TO17 / TXD5 / DD15	TO18 / RXD5 / DD14	TO19 / DD13	TO20 / DD12
P10	TO8	TO9 / CRX0	TO10 / CTX0	TO11 / TIN24	TO12 / TIN25 / DD3	TO13 / SCLKI4 / SCLKO4 / DD2	TO14 / TXD4 / DD1	TO15 / RXD4 / DD0
P11	TO0 / TO29 / DD11	TO1 / TO30 / DD10	TO2 / TO31 / DD9	TO3 / TO32 / DD8	TO4 / TO33 / DD7	TO5 / TO34 / DD6	TO6 / TO35 / DD5	TO7 / TO36 / DD4
P12					TCLK0 / DD3	TCLK1 / DD2	TCLK2 / DD1	TCLK3 / DD0
P13	TIN16 / PWMOFF0 / DIN0	TIN17 / PWMOFF1 / DIN1	TIN18 / DIN2	TIN19 / DIN3	TIN20 / TXD3 / DIN4	TIN21 / RXD3	TIN22 / CRX1	TIN23 / CTX1
P14								
P15	TIN0 / CLKOUT / WR#(Note 2)			TIN3 / WAIT#				
P16								
P17					TXD2 / TO28	RXD2 / TO27		
P18								
P19								
P20								
P21								
P22	CTX0 / HACK#	CRX0 / HREQ#			P224 (Port only)	P225 (Port only)		

Note 1: These ports cannot be used for input/output port function. The SBI#, MOD0 and MOD1 pin input levels can be read from these ports.
Note 2: Respective functions are selected by the Bus Mode Control Register.
Note : • P5, P14, P16, P18, P19, P20 and P21 are not provided.

Figure 4.2.1 Input/Output Ports and Pin Function Assignments during Single Chip Mode

Pin functions are selected by the settings for the port operation mode and port peripheral function select registers (P0–P4)

Pin functions are selected by the settings for the port operation mode, port peripheral function select and NBD function select registers (P6–P22)

	0	1	2	3	4	5	6	7
P0	DB0 / TO21 / DD0	DB1 / TO22 / DD1	DB2 / TO23 / DD2	DB3 / TO24 / DD3	DB4 / TO25 / DD4	DB5 / TO26 / DD5	DB6 / TO27 / DD6	DB7 / TO28 / DD7
P1	DB8 / TO29 / DD8	DB9 / TO30 / DD9	DB10 / TO31 / DD10	DB11 / TO32 / DD11	DB12 / TO33 / DD12	DB13 / TO34 / DD13	DB14 / TO35 / DD14	DB15 / TO36 / DD15
P2	A23 / DD24	A24 / DD25	A25 / DD26	A26 / DD27	A27 / DD28	A28 / DD29	A29 / DD30	A30 / DD31
P3	A15 / TIN4 / DD16	A16 / TIN5 / DD17	A17 / TIN6 / DD18	A18 / TIN7 / DD19	A19 / TIN30 / DD20	A20 / TIN31 / DD21	A21 / TIN32 / DD22	A22 / TIN33 / DD23
P4		BLW# / BLE# (Note 1, 3)	BHW# / BHE# (Note 1, 3)	RD# (Note 1)	CS0# / TIN8	CS1# / TIN9	A13 / TIN10	A14 / TIN11
P5								
P6		P61 (Port only)	P62 (Port only)	P63 (Port only)	SBI# (Note 2)			
P7	CLKOUT / WR# / BCLK(Note 3)	WAIT#	HREQ# / TIN27	HACK# / TIN26	RTDTXD / TXD3 / NBDD0	RTDRXD / RXD3 / NBDD1	RTDACK / CTX1 / NBDD2	RTDCLK / CRX1 / NBDD3
P8	MOD0 (Note 2)	MOD1 (Note 2)	TXD0 / TO26	RXD0 / TO25	SCLKI0 / SCLKO0 / TO24	TXD1 / TO23	RXD1 / TO22	SCLKI1 / SCLKO1 / TO21
P9				TO16 / SCLKI5 / SCLKO5	TO17 / TXD5 / DD15	TO18 / RXD5 / DD14	TO19 / DD13	TO20 / DD12
P10	TO8	TO9 / CRX0	TO10 / CTX0	TO11 / TIN24	TO12 / TIN25 / DD3	TO13 / SCLKI4 / SCLKO4 DD2	TO14 / TXD4 / DD1	TO15 / RXD4 / DD0
P11	TO0 / TO29 / DD11	TO1 / TO30 / DD10	TO2 / TO31 / DD9	TO3 / TO32 / DD8	TO4 / TO33 / DD7	TO5 / TO34 / DD6	TO6 / TO35 / DD5	TO7 / TO36 / DD4
P12					TCLK0 / A9 / DD3	TCLK1 / A10 / DD2	TCLK2 / CS2# / DD1	TCLK3 / CS3# / DD0
P13	TIN16 / PWMOFF0 / DIN0	TIN17 / PWMOFF1 / DIN1	TIN18 / DIN2	TIN19 / DIN3	TIN20 / TXD3 / DIN4	TIN21 / RXD3	TIN22 / CRX1	TIN23 / CTX1
P14								
P15	TIN0 / CLKOUT / WR#(Note 3)			TIN3 / WAIT#				
P16								
P17					TXD2 / TO28	RXD2 / TO27		
P18								
P19								
P20								
P21								
P22	CTX0 / HACK#	CRX0 / HREQ#			A11 / CS2#	A12 / CS3#		

Note 1: These ports cannot be used for input/output port function, function as external bus interface related signals.
Note 2: These ports cannot be used for input/output port function. The SBI#, MOD0 and MOD1 pin input levels can be read from these ports.
Note 3: Respective functions are selected by the Bus Mode Control Register.
Note : • P5, P14, P16, P18, P19, P20 and P21 are not provided.

Figure 4.2.2 Input/Output Ports and Pin Function Assignments during External Extension Mode

		0	1	2	3	4	5	6	7
	P0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
	P1	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15
(Note 1)	P2	A23	A24	A25	A26	A27	A28	A29	A30
	P3	A15	A16	A17	A18	A19	A20	A21	A22
	P4		BLW# / BLE#(Note 3)	BHW# / BHE#(Note 3)	RD#	CS0#	CS1#	A13	A14
	P5								
	P6		P61 (Port only)	P62 (Port only)	P63 (Port only)	SBI# (Note 2)			
	P7	CLKOUT / WR# / BCLK(Note 3)	WAIT#	HREQ# / TIN27	HACK# / TIN26	RTDTXD / TXD3 / NBDD0	RTDRXD / RXD3 / NBDD1	RTDACK / CTX1 / NBDD2	RTDCLK / CRX1 / NBDD3
	P8	MOD0 (Note 2)	MOD1 (Note 2)	TXD0 / TO26	RXD0 / TO25	SCLKI0 / SCLKO0 / TO24	TXD1 / TO23	RXD1 / TO22	SCLKI1 / SCLKO1 / TO21
	P9				TO16 / SCLKI5 / SCLKO5	TO17 / TXD5 / DD15	TO18 / RXD5 / DD14	TO19 / DD13	TO20 / DD12
	P10	TO8	TO9 / CRX0	TO10 / CTX0	TO11 / TIN24	TO12 / TIN25 / DD3	TO13 / SCLKI4 / SCLKO4 DD2	TO14 / TXD4 / DD1	TO15 / RXD4 / DD0
	P11	TO0 / TO29 / DD11	TO1 / TO30 / DD10	TO2 / TO31 / DD9	TO3 / TO32 / DD8	TO4 / TO33 / DD7	TO5 / TO34 / DD6	TO6 / TO35 / DD5	TO7 / TO36 / DD4
	P12					A9 (Note 1)	A10 (Note 1)	TCLK2 / CS2# / DD1	TCLK3 / CS3# / DD0
	P13	TIN16 / PWMOFF0 / DIN0	TIN17 / PWMOFF1 / DIN1	TIN18 / DIN2	TIN19 / DIN3	TIN20 / TXD3 / DIN4	TIN21 / RXD3	TIN22 / CRX1	TIN23 / CTX1
Pin functions are selected by the settings for the port operation mode, port peripheral function select and NBD function select registers	P14								
	P15	TIN0 / CLKOUT / WR#(Note 3)			TIN3 / WAIT#				
	P16								
	P17					TXD2 / TO28	RXD2 / TO27		
	P18								
	P19								
	P20								
	P21								
	P22	CTX0 / HACK#	CRX0 / HREQ#			A11/CS2# (Note 1)	A12/CS3# (Note 1)		

Note 1: These ports cannot be used for input/output port function, function as external bus interface related signals.
Note 2: These ports cannot be used for input/output port function. The SBI#, MOD0 and MOD1 pin input levels can be read from these ports.
Note 3: Respective functions are selected by the Bus Mode Control Register.
Note : • P5, P14, P16, P18, P19, P20 and P21 are not provided.

Figure 4.2.3 Input/Output Ports and Pin Function Assignments during Processor Mode

4.3 Port Input Level Switching Function

The port input level switching function allows the port threshold to be switched to one of three voltage levels (with or without Schmitt as selected) in units of the following port group. This can be set to the following registers in units of group.
Note that port inputs are used for the DD input of DRI.

Port Group 0: P00–P07, P10–P17, P20–P27, P30–P37, P41–P47, P70–P73, P224, P225
Port Group 1: P82–P87, P174, P175
Port Group 3: P93–P97, P110–P117
Port Group 4: P124–P127
Port Group 5: P61–P63, SBI#
Port Group 6: P74–P77, P100–P107
Port Group 7: P220, P221
Port Group 8: P130–P137, P150, P153

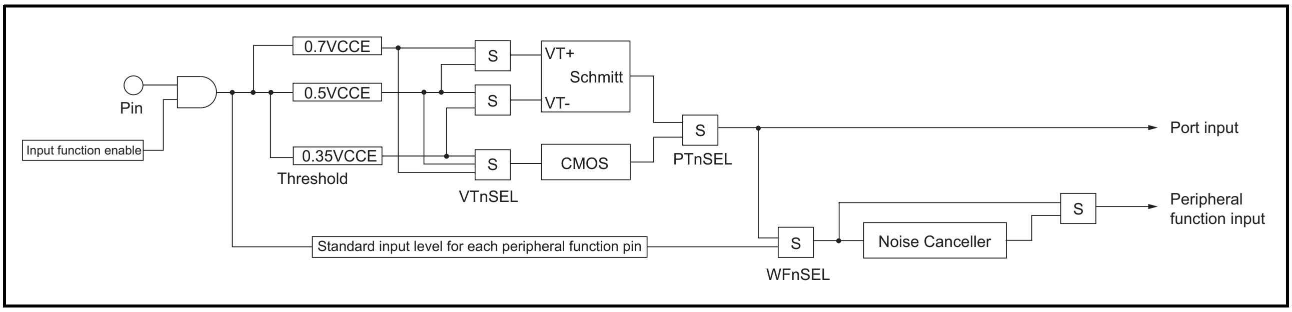


Figure 4.3.1 Port Input Level Switching Function

5.1 Outline of the DMAC

The microcomputer internally contains a 10-channel DMAC (Direction Memory Access Controller). It allows data to be transferred at high speed between internal peripheral I/Os, between internal RAM and internal peripheral I/O, or between internal RAMs, as initiated by a software trigger or requested from an internal peripheral I/O.

Table 5.1.1 Outline of the DMAC

Item	Description
Number of channels	10 channels
Transfer request sources	• Software trigger • Request from internal peripheral I/Os: A/D converter, multijunction timer, serial interface (reception completed, transmit buffer empty), CAN or DRI • DMA channels can be cascaded (Note 1)
Maximum number of times transferred	65,536 times
Transferable address space (Note 2)	• 64 Kbytes + 16 Kbytes (address space from H’0080 0000 to H’0081 3FFF) • Transfers between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs are supported.
Transfer data size	16 or 8 bits
Transfer method	Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual address transfer
Transfer mode	Single transfer mode
Direction of transfer	One of three modes can be selected for the source and destination: • Address fixed • Address incremental • Ring buffered (can be selected from 32, 16, 8, 4 or 2 times)
Channel priority	DMA0 > DMA1 > DMA2 > DMA3 > DMA4 > DMA5 > DMA6 > DMA7 > DMA8 > DMA9 (Priority is fixed)
Maximum transfer rate	13.3 Mbytes per second (when internal peripheral clock BCLK = 20 MHz)
Interrupt request	Group interrupt request can be generated when each transfer count register underflows.
Transfer area (Note 2)	64 Kbytes +16 Kbytes from H’0080 0000 to H’0081 3FFF (Transferable in the entire RAM/SFR area)

Note 1: The DMA channels can be cascaded in the manner described below.

- Start DMA transfer on DMA1 upon completion of one DMA transfer on DMA0
- Start DMA transfer on DMA5 upon completion of all DMA transfers on DMA0 (upon underflow of the transfer count register)
- Start DMA transfer on DMA2 upon completion of one DMA transfer on DMA1
- Start DMA transfer on DMA0 upon completion of one DMA transfer on DMA2
- Start DMA transfer on DMA3 upon completion of one DMA transfer on DMA2
- Start DMA transfer on DMA4 upon completion of one DMA transfer on DMA3
- Start DMA transfer on DMA6 upon completion of one DMA transfer on DMA5
- Start DMA transfer on DMA7 upon completion of one DMA transfer on DMA6
- Start DMA transfer on DMA5 upon completion of one DMA transfer on DMA7
- Start DMA transfer on DMA8 upon completion of one DMA transfer on DMA7
- Start DMA transfer on DMA9 upon completion of one DMA transfer on DMA8

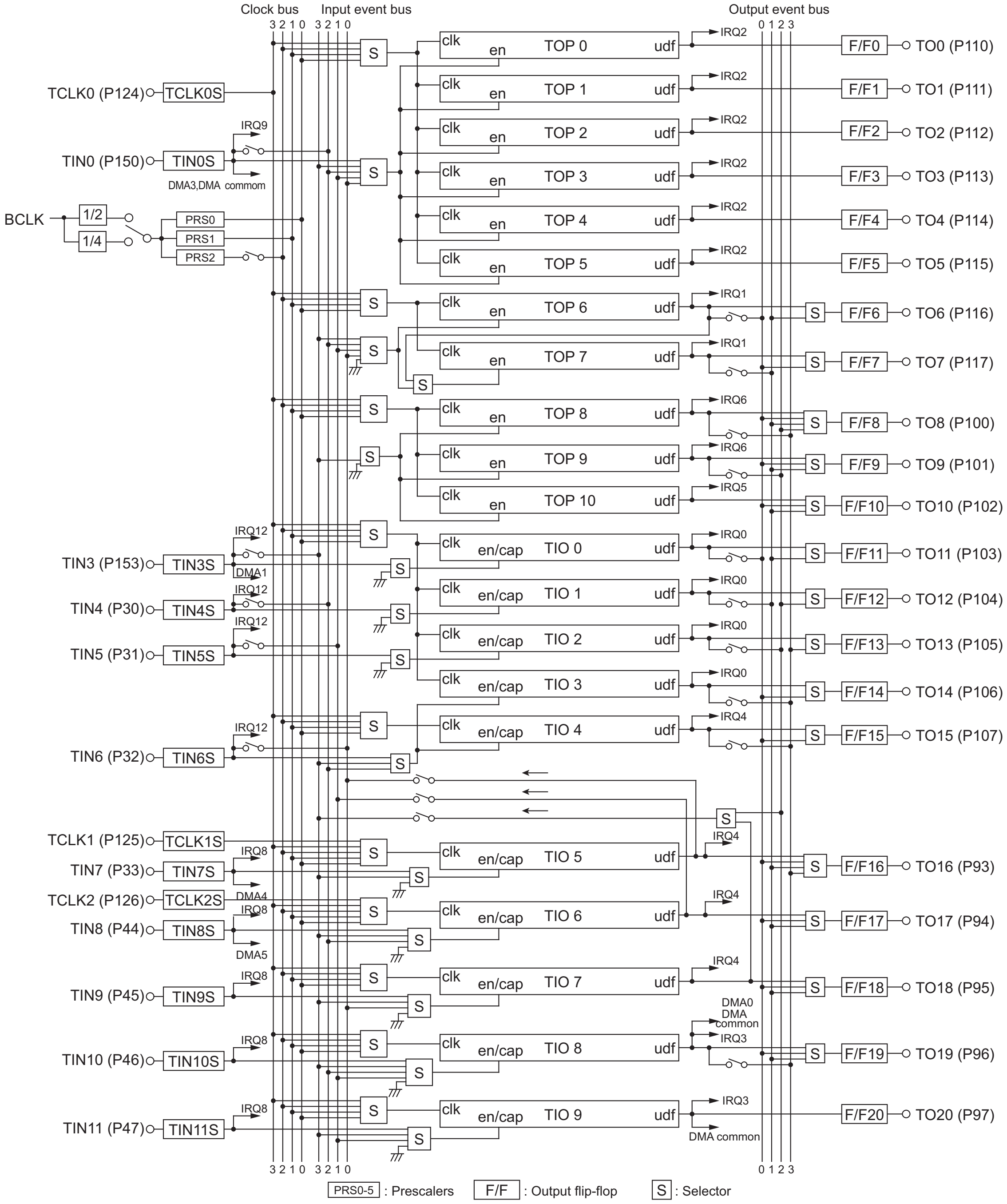
Note 2: The source address and destination address cannot go over the bank, which can be only transferred to the same bank or another one from a certain bank.

6.1 Outline of Multijunction Timers

The multijunction timers (abbreviated MJT) have input event and output event buses. Therefore, in addition to being used as a single unit, the timers can be internally connected to each other. This capability allows for highly flexible timer configuration, making it possible to meet various application needs. It is because the timers are connected to the internal event buses at multiple points that they are called the “multijunction” timers.
The 32186 has six types of MJT as listed in the table below, providing a total of 55-channel timers.

Table 6.1.1 Outline of MJT

Name	Type	No. of Channels	Description
TOP (Timer OutPut)	Output-related 16-bit timer (down-counter)	11	One of three output modes can be selected by software. <With correction function> • Single-shot output mode • Delayed single-shot output mode <Without correction function> • Continuous output mode
TIO (Timer Input OutPut)	Input/output-related 16-bit timer (down-counter)	10	One of three input modes or four output modes can be selected by software. <Input modes> • Measure clear input mode • Measure free-run input mode • Noise processing input mode <Output modes without correction function> • PWM output mode • Single-shot output mode • Delayed single-shot output mode • Continuous output mode
TMS (Timer Measure Small)	Input-related 16-bit timer (up-counter)	8	16-bit input measure timer
TML (Timer Measure Large)	Input-related 32-bit timer (up-counter)	8	32-bit input measure timer
TID (Timer Input Derivation)	Input-related 16-bit timer (up/down-counter)	2	One of four input modes can be selected by software. • Fixed period mode • Event count mode • Multiply-by-4 event count mode • Up/down event count mode
TOU (Timer Output Unification)	Output-related 24-bit timer (down-counter) (16-bit timer during PWM output and single-shot PWM output modes)	16	One of five output modes can be selected by software. <Without correction function> • PWM output mode • Single-shot PWM output mode • Delayed single-shot output mode • Single-shot output mode • Continuous output mode



Notes: • IRQ0-18 denotes interrupt signals, of which the same number represents the same group of interrupts.
• DMA0-9 and DMA common denote DMA request signals to the DMAC.
• AD0TRG denotes trigger signal to the A/D0 converter.

Figure 6.1.1 Block Diagram of MJT (1/4)

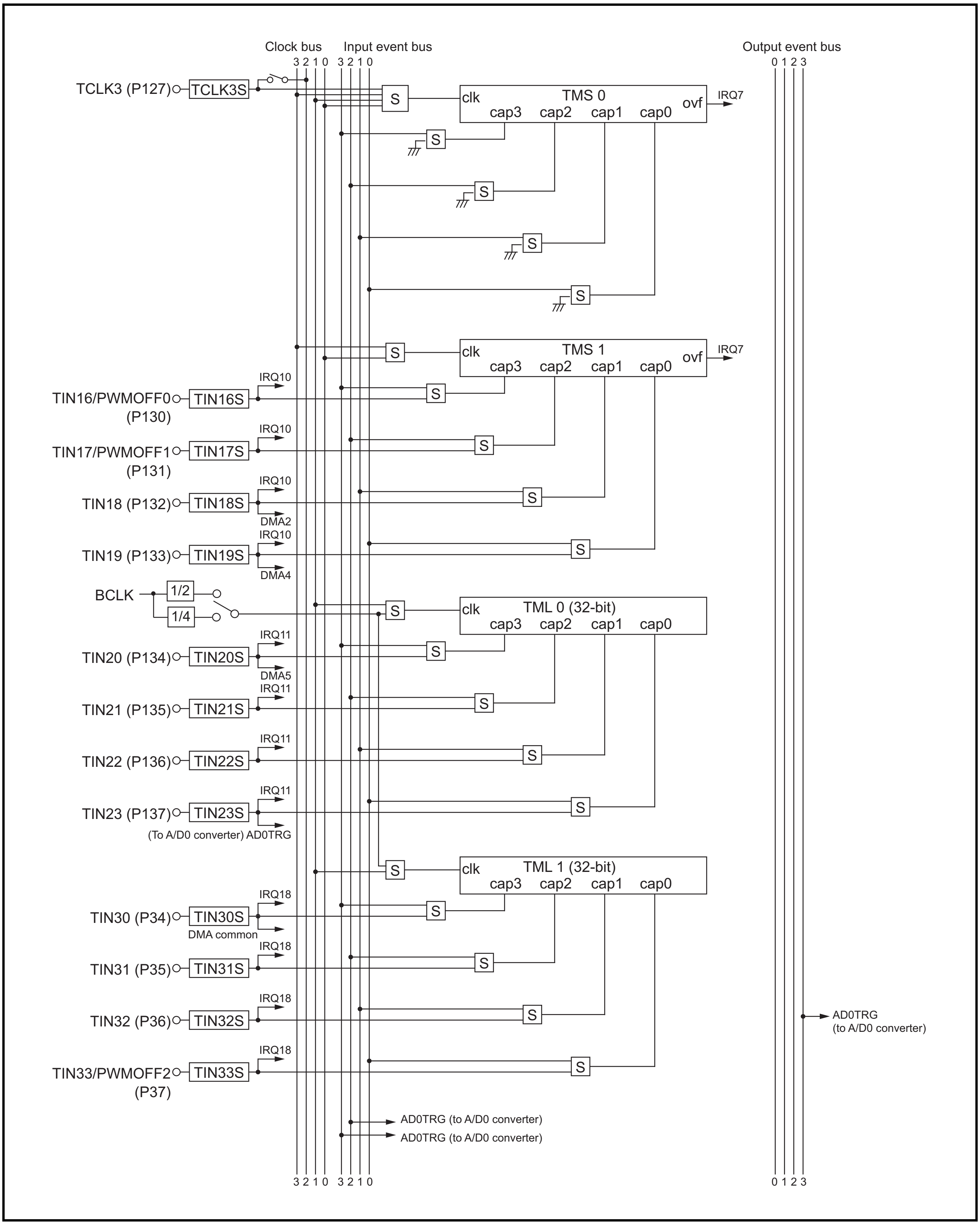


Figure 6.1.2 Block Diagram of MJT (2/4)

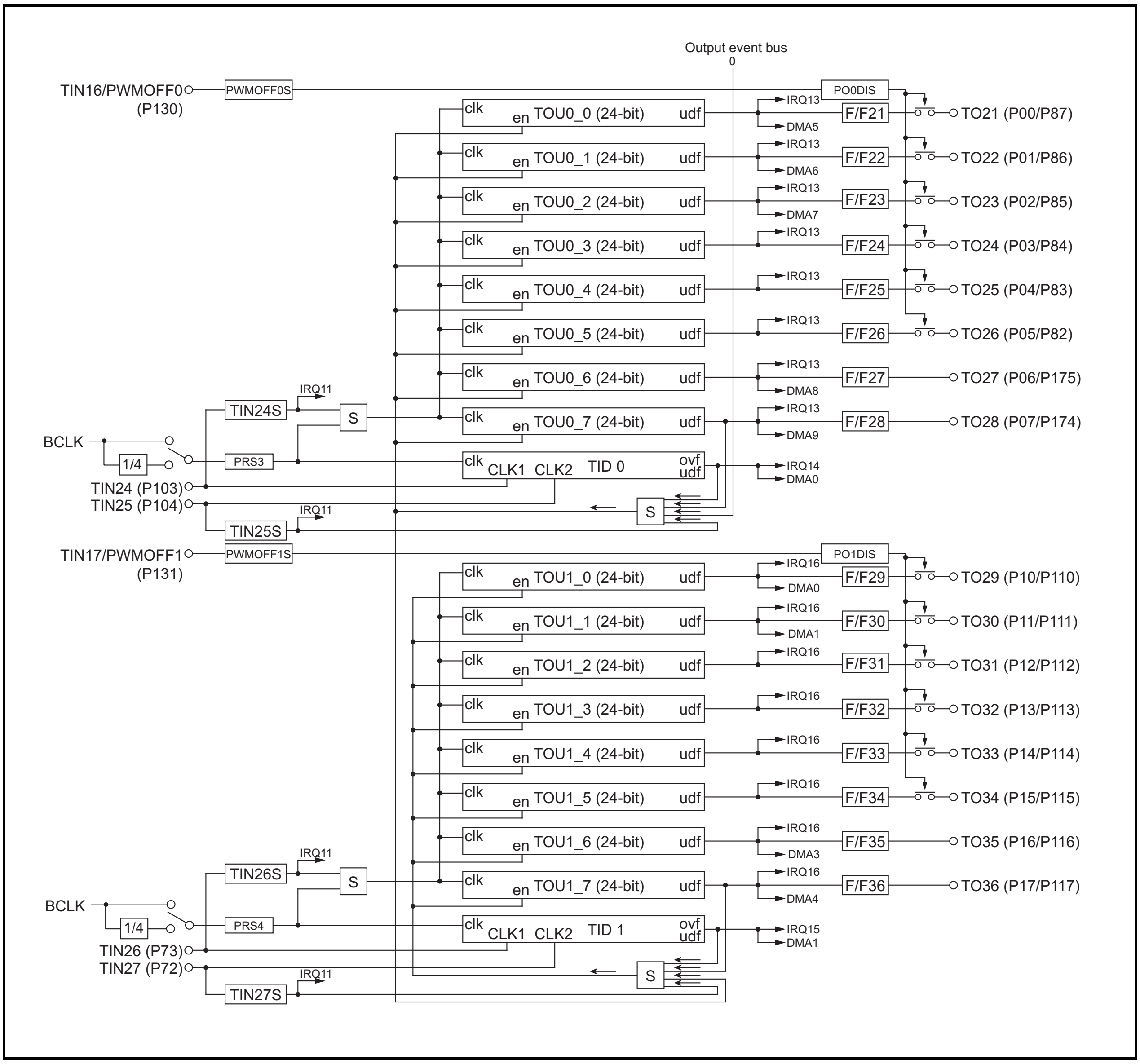
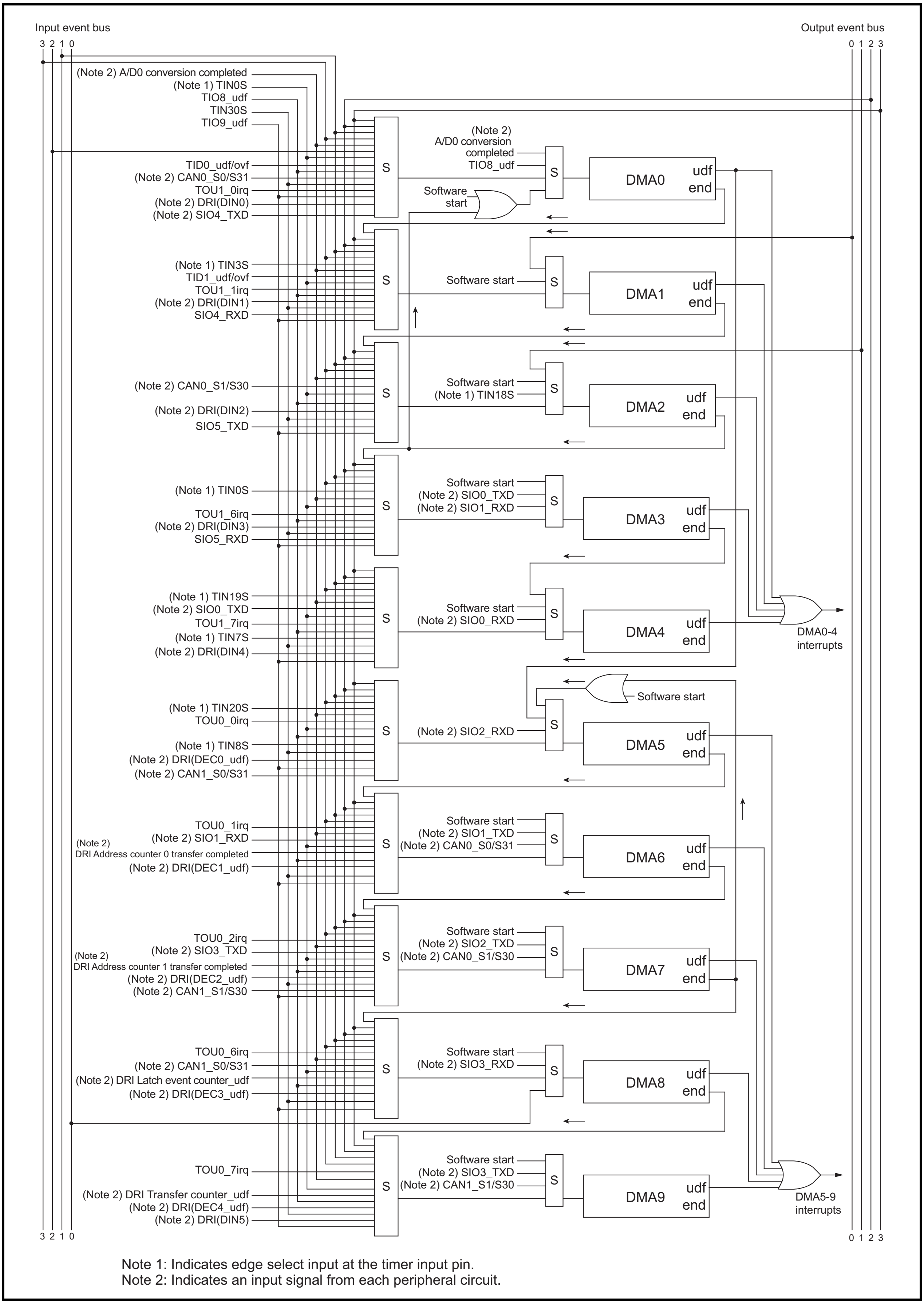


Figure 6.1.3 Block Diagram of MJT (3/4)



Note 1: Indicates edge select input at the timer input pin.
Note 2: Indicates an input signal from each peripheral circuit.

Figure 6.1.4 Block Diagram of MJT (4/4)

7.1 Outline of A/D Converter

The 32186 contains 10-bit resolution A/D Converter of the successive approximation type. The A/D converter has 16 analog input pins (channels) AD0IN0–AD0IN15. In addition to performing conversion individually on each channel, the A/D Converter can perform conversion successively on all of N channels (N = 1–16) as a single group. The conversion result can be read out in either 10 or 8 bits.
There are following conversion and operation modes for the A/D conversion:

(1) Conversion Modes

- A/D conversion mode: Ordinary mode in which analog input voltages are converted into digital quantities.
- Comparator mode (Note 1): A mode in which analog input voltage is compared with a preset comparison voltage to find only the relative magnitude of two quantities. (Useful in only single operation mode)

(2) Operation Modes

- Single mode: Analog input voltage on one channel is A/D converted once or comparated (Note 1) with a given quantity.
- Scan mode: Analog input voltages on two or more selected channels (in N channel units, N = 1–16) are sequentially A/D converted.

  Single-shot scan mode: Scan operation is performed for one cycle.

  Continuous scan mode: Scan operation is repeated until stopped.

(3) Special Operation Modes

- Forcible single mode execution during scan mode: Conversion is forcibly executed in single mode (comparator mode) during scan operation.
- Scan mode start after single mode execution: Scan operation is started subsequently after executing conversion in single mode.
- Conversion restart: A/D conversion being executed in single or scan mode is restarted.

(4) Sample-and-Hold Function

The analog input voltage is sampled when starting A/D conversion, and A/D conversion is performed on the sampled voltage. This function can be enabled or disabled as necessary.

(5) Simultaneous Sampling Function

Optional two channels are sampled at the same time, and 2-channel continuous A/D conversion is carried out for the sampled voltage.

(6) A/D Disconnection Detection Assist Function

To suppress influences of the analog input voltage leakage from any preceding channel during scan mode operation, a function is incorporated that helps to fix the electric charge on the chopper amp capacitor to the given state (AVCC or GND) before starting A/D conversion. This function provides a sure and reliable means of detecting a disconnection in the wiring patterns connecting to the analog input pins.

(7) Inflow Current Bypass Circuit

If an overvoltage or negative voltage is applied to any analog input channel which is currently inactive, a current flows into or out of the analog input channel currently being A/D converted via the internal circuit, causing the conversion accuracy to degrade. To solve this problem, the A/D Converter incorporates a circuit that bypasses such inflow current. This circuit is always enabled.

(8) Conversion Speed

The A/D conversion and comparate speed can be selected from among 8 types: BCLK mode & 2BCLK mode/each slow mode & each fast mode/each normal mode & each double speed mode.

(9) Interrupt Request and DMA Transfer Request Generation Functions

An A/D conversion interrupt or DMA transfer request can be generated each time A/D conversion or comparate operation in single mode is completed, as well as when a single-shot scan operation or one cycle of continuous scan operation is completed.

Note 1: To discriminate between the comparison performed internally by the successive approximation type A/D Converter and that performed in comparator mode using the same A/D Converter as a comparator, the comparison in comparator mode is referred to in this data sheet as “comparate.”

Table 7.1.1 outlines the A/D Converter and Figure 7.1.1 shows block diagram of A/D Converter.

Table 7.1.1 Outline of the A/D Converter

Item	Description					
Analog input	16 channels x 1					
A/D conversion method	Successive approximation method					
Resolution	10 bits (Conversion result can be read out in either 8 or 10 bits)					
Absolute accuracy (Note 1) Conditions: Ta = 25°C, AVCC0 = 5.12 V, VREF0 = 5.12 V	2BCLK mode (Note 4)		Slow mode	Normal speed	±2LSB (±3LSB) (Note 2)	
				Double speed	±2LSB (±3LSB) (Note 2)	
			Fast mode	Normal speed	±3LSB (±3LSB) (Note 2)	
				Double speed	±3LSB (T.B.D) (Note 2)	
	BCLK mode		Slow mode	Normal speed	±2LSB (±3LSB) (Note 2)	
				Double speed	±2LSB (±3LSB) (Note 2)	
			Fast mode	Normal speed	±3LSB (±3LSB) (Note 2)	
				Double speed	±3LSB (T.B.D) (Note 2)	
Conversion mode	A/D conversion mode and comparator mode					
Operation mode	Single mode, single-shot scan mode and continuous scan mode					
Conversion start trigger	Software start	Started by setting the A/D conversion start bit to "1"				
	Hardware start	A/D0 Converter	MJT (input event bus 2), MJT (input event bus 3), MJT (output event bus 3) and MJT (TIN23)			
Conversion speed (Note 3) BCLK peripheral clock	2BCLK	During single mode (When sample-and-hold disabled/ When normal sample-and-hold enabled)	Slow mode	Normal speed	598 x BCLK	29.9 µs
				Double speed	346 x BCLK	17.3 µs
			Fast mode	Normal speed	262 x BCLK	13.1 µs
				Double speed	178 x BCLK	8.9 µs
		During single mode (When fast sample-and-hold enabled)	Slow mode	Normal speed	382 x BCLK	19.1 µs
				Double speed	202 x BCLK	10.1 µs
			Fast mode	Normal speed	190 x BCLK	9.5 µs
				Double speed	106 x BCLK	5.3 µs
		During comparator mode	Slow mode	Normal speed	94 x BCLK	4.7 µs
				Double speed	58 x BCLK	2.9 µs
			Fast mode	Normal speed	46 x BCLK	2.3 µs
				Double speed	34 x BCLK	1.7 µs
	BCLK	During single mode (When sample-and-hold disabled/ When normal sample-and-hold enabled)	Slow mode	Normal speed	299 x BCLK	14.95 µs
				Double speed	173 x BCLK	8.65 µs
			Fast mode	Normal speed	131 x BCLK	6.55 µs
				Double speed	89 x BCLK	4.45 µs
		During single mode (When fast sample-and-hold enabled)	Slow mode	Normal speed	191 x BCLK	9.55 µs
				Double speed	101 x BCLK	5.05 µs
			Fast mode	Normal speed	95 x BCLK	4.75 µs
				Double speed	53 x BCLK	2.65 µs
		During comparator mode	Slow mode	Normal speed	47 x BCLK	2.35 µs
				Double speed	29 x BCLK	1.45 µs
			Fast mode	Normal speed	23 x BCLK	1.15 µs
				Double speed	17 x BCLK	0.85 µs
Sample-and-hold function	Sample-and-hold function can be enabled or disabled as necessary.					
A/D disconnection detection assist function	Influences of the analog input voltage leakage from any preceding channel during scan mode operation are suppressed.					
Interrupt request generation function	Generated when A/D conversion (single mode operation, single-shot scan operation or one cycle of continuous scan operation) or comparate operation is completed.					
DMA transfer request generation function	Generated when A/D conversion (single mode operation, single-shot scan operation or one cycle of continuous scan operation) or comparate operation is completed.					

Note 1: The conversion accuracy stipulated here refers to that of the microcomputer alone, with influences of the power supply wiring and noise on the board not taken into account.

Note 2: The parenthesis ( ) indicates the value when the fast sample-and-hold function is effective.

Note 3: Conversion time when f(XIN) = 10 MHz (1BCLK = 50 ns).

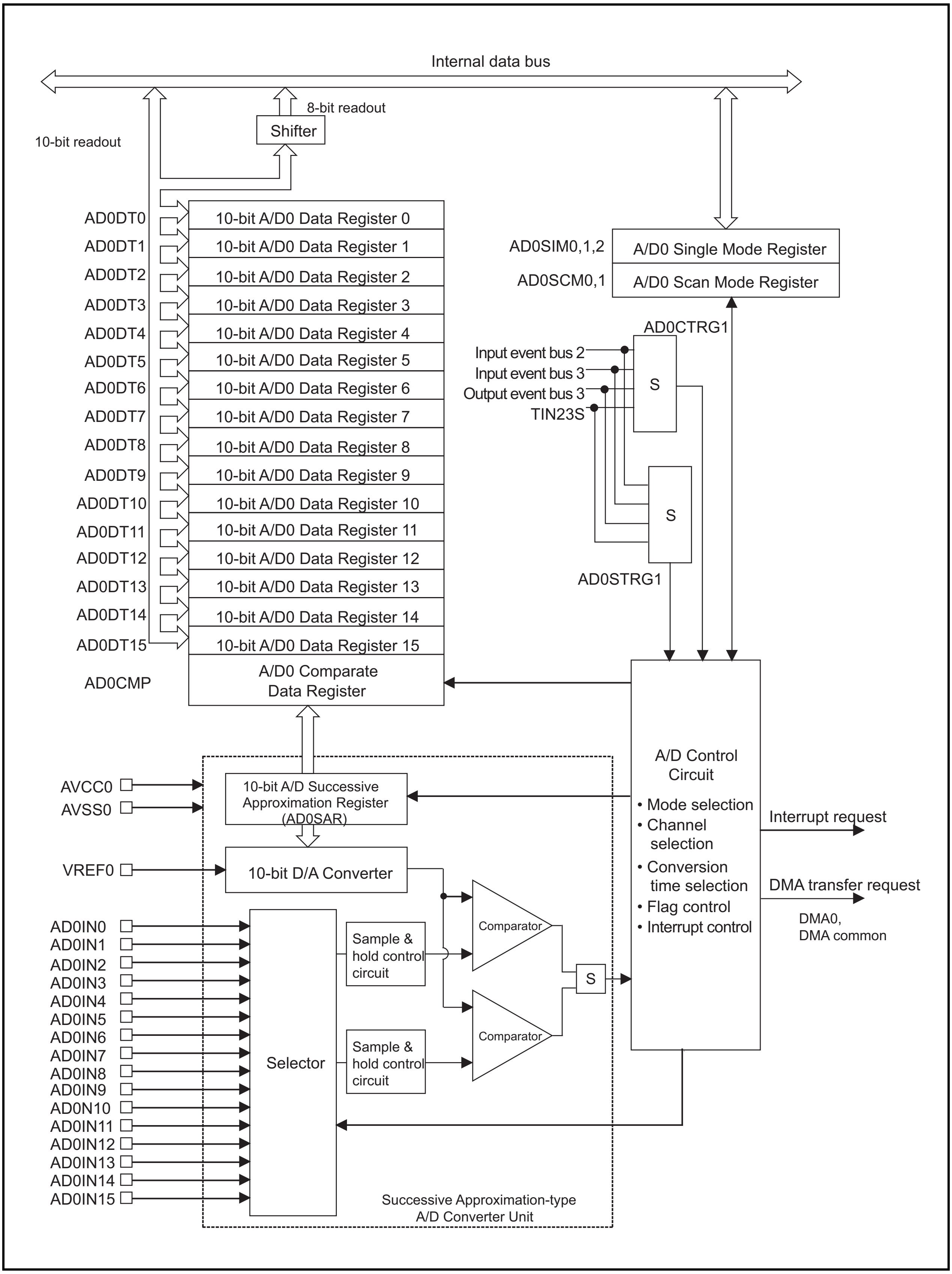


Figure 7.1.1 Block Diagram of the A/D Converter

8.1 Outline of Serial Interface

The 32186 contains a total of six serial interface channels, SIO0–SIO5. Channels SIO0, SIO1, SIO4 and SIO5 can be selected between CSIO mode (clock-synchronous serial interface) and UART mode (clock-asynchronous serial interface). Channels SIO2 and SIO3 are UART mode only.

- **CSIO mode (clock-synchronous serial interface)**

Communication is performed synchronously with a transfer clock, using the same clock on both transmit and receive sides. The transfer data length can be selected within the range from 8 to 16 bits long.

- **UART mode (clock-asynchronous serial interface)**

Communication is performed at any transfer rate in any transfer data format. The transfer data length can be selected from 7, 8 and 9 bits.

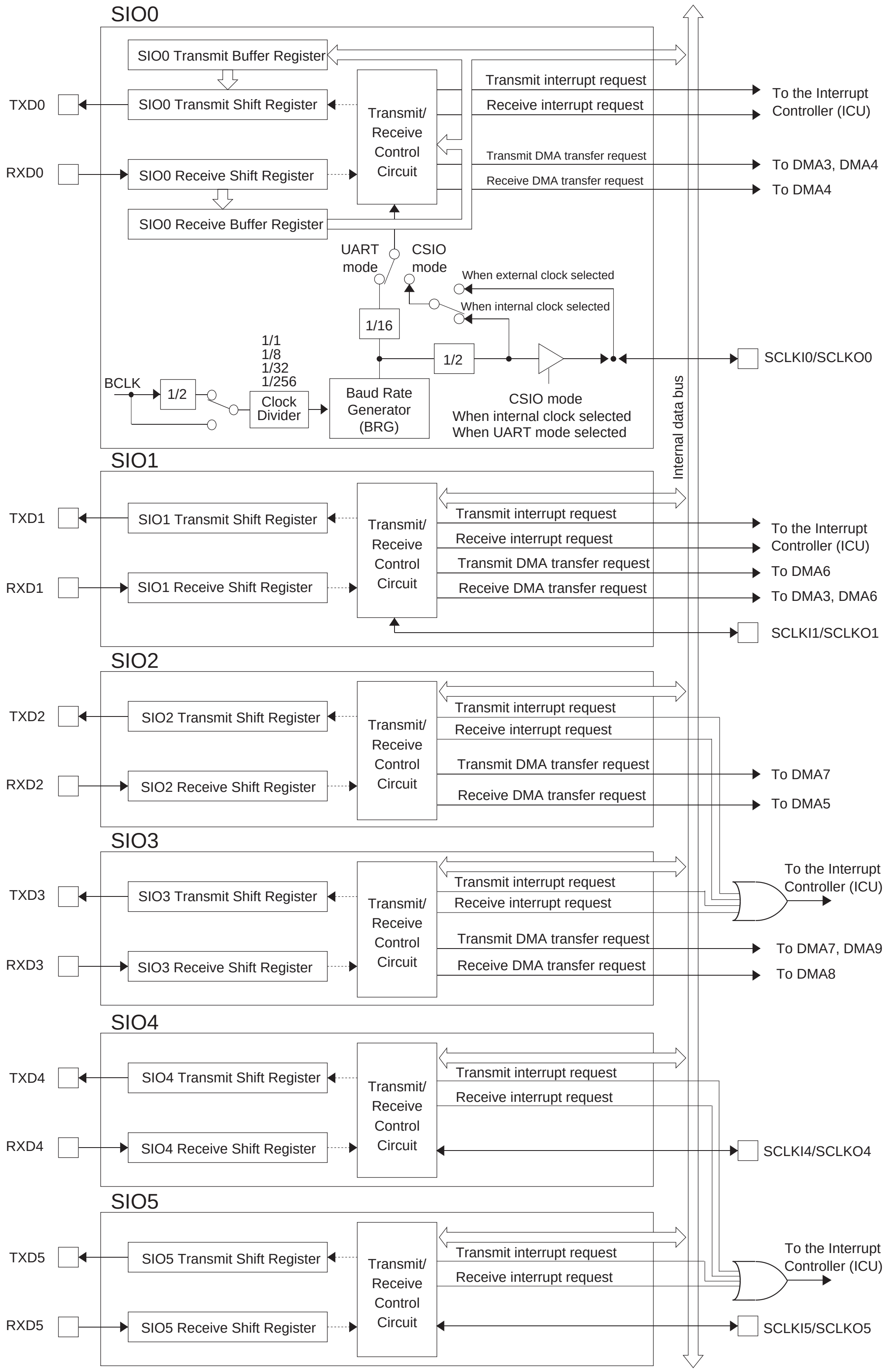
Channels SIO0–SIO3 each have a transmit DMA transfer and a receive DMA transfer request. These serial interfaces, when combined with the internal DMA Controller (DMAC), allow serial communication to be performed at high speed, as well as reduce the data communication load of the CPU.

Serial interface is outlined below.

Table 8.1.1 Outline of Serial Interface

Item	Description	
Number of channels	CSIO mode/UART mode:	4 channels (SIO0, SIO1, SIO4, SIO5)
	UART only:	2 channels (SIO2, SIO3)
Clock	During CSIO mode:	Internal clock or external clock as selected (Note 1), clock polarity can be selected
	During UART mode:	Internal clock only
Transfer mode	Transmit half-duplex, receive half-duplex, transmit/receive full-duplex	
BRG count source (when internal clock selected)	f(BCLK), f(BCLK)/8, f(BCLK)/32, f(BLCK)/256 (Note 2) f(BCLK)/2, f(BCLK)/16, f(BCLK)/64, f(BCLK)/512 f(BCLK): Peripheral clock operating frequency	
Data format	CSIO mode:	Data length = selectable in the range of 8–16 bits Order of transfer = selectable from LSB first or MSB first
	UART mode:	Start bit = 1 bit Character length = 7, 8 or 9 bits Parity bit = Added (odd, even) or not added Stop bit = 1 or 2 bits Order of transfer = selectable from LSB first or MSB first
Baud rate	CSIO mode: (Note 1)	76 bits/sec to 2 Mbits/sec (when f(BCLK) = 20 MHz/internal clock selected) Max 1.25 Mbits/sec (when f(BCLK) = 20 MHz/external clock selected)
	UART mode:	9.5 bits/sec to 1.25 Mbits/sec (when f(BCLK) = 20 MHz)
Error detection	CSIO mode:	Overrun error only
	UART mode:	Overrun, parity and framing errors (Occurrence of any of these errors is indicated by an error sum bit)
Fixed period clock output function	When using SIO0, SIO1, SIO4 and SIO5 as UART, this function outputs a divided-by-2 BRG clock from the SCLK pin.	

Note 1: The maximum input frequency of an external clock during CSIO mode is f(BCLK)/16.
Note 2: If f(BCLK) is selected as the count source, the BRG set value is subject to limitations.



Notes: • When BCLK is selected, the BRG set value is subject to limitations.
• SIO2 and SIO3 do not have the SCLKI/SCLKO function.

Figure 8.1.1 Block Diagram of Serial Interfaces

9.1 Outline of the CAN Module

The 32186 contains two-channel Full CAN modules compliant with CAN (Controller Area Network) Specification V2.0B Active. These CAN modules each have 32 message slots and four mask registers, effective use of which helps to reduce the data processing load of the CPU.
The CAN modules are outlined below.

Table 9.1.1 Outline of the CAN Module

Item	Description
Protocol	CAN Specification V2.0B Active
Number of message slots	Total 32 slots (30 global slots, two local slots)
Polarity	0: Dominant 1: Recessive
Acceptance filter (Function to receive only a range of IDs specified by receive ID filter)	Global mask: 2 Local mask: 2
Baud rate	1 time quantum (Tq) = (BRP + 1) / (CPUCLK/4 or CPUCLK/2) (Note 2) (BRP: Baud Rate Prescaler set value) $\text{Baud rate} = \dfrac{1}{\text{Tq period x number of Tq's for one bit}}$ . . . Max 1 Mbps (Note 1) BRP: 1–255 (0: inhibited) Number of Tq's for one bit = Synchronization Segment + Propagation Segment + Phase Segment 1 + Phase Segment 2 Synchronization Segment: 1Tq Propagation Segment: 1–8Tq Phase Segment 1: 1–8Tq Phase Segment 2: 1–8Tq (IPT = 1)
Remote frame automatic response function	The slot that received a remote frame responds by automatically sending a data frame.
Timestamp function	This function is implemented using a 16-bit counter. The count period is derived from the CAN bus bit period by dividing it by 1, 2, 3 or 4.
BasicCAN mode	Double buffer function is materialized using two local slots.
Transmit abort function	Transmit requests can be canceled.
Loopback function	The CAN module receives the data transmitted by the module itself.
Return bus off function	Error active mode is forcibly entered into after clearing the error counter.
Single shot function	Transmission is not retried even when it failed due to arbitration-lost or a transmit error.
DMA transfer function	DMA transfer request is generated when transmission failed or transmit/receive operation finished.
Self-diagnostic function	Communication module is diagnosed by communicating internally in the CAN module.

Note 1: The maximum allowable error of oscillation depends on the system configuration (e.g., bus length, clock error, CAN bus transceiver, sampling position and bit configuration).
Note 2: It depends on a clock to be supplied to the protocol engine block in the CAN module.

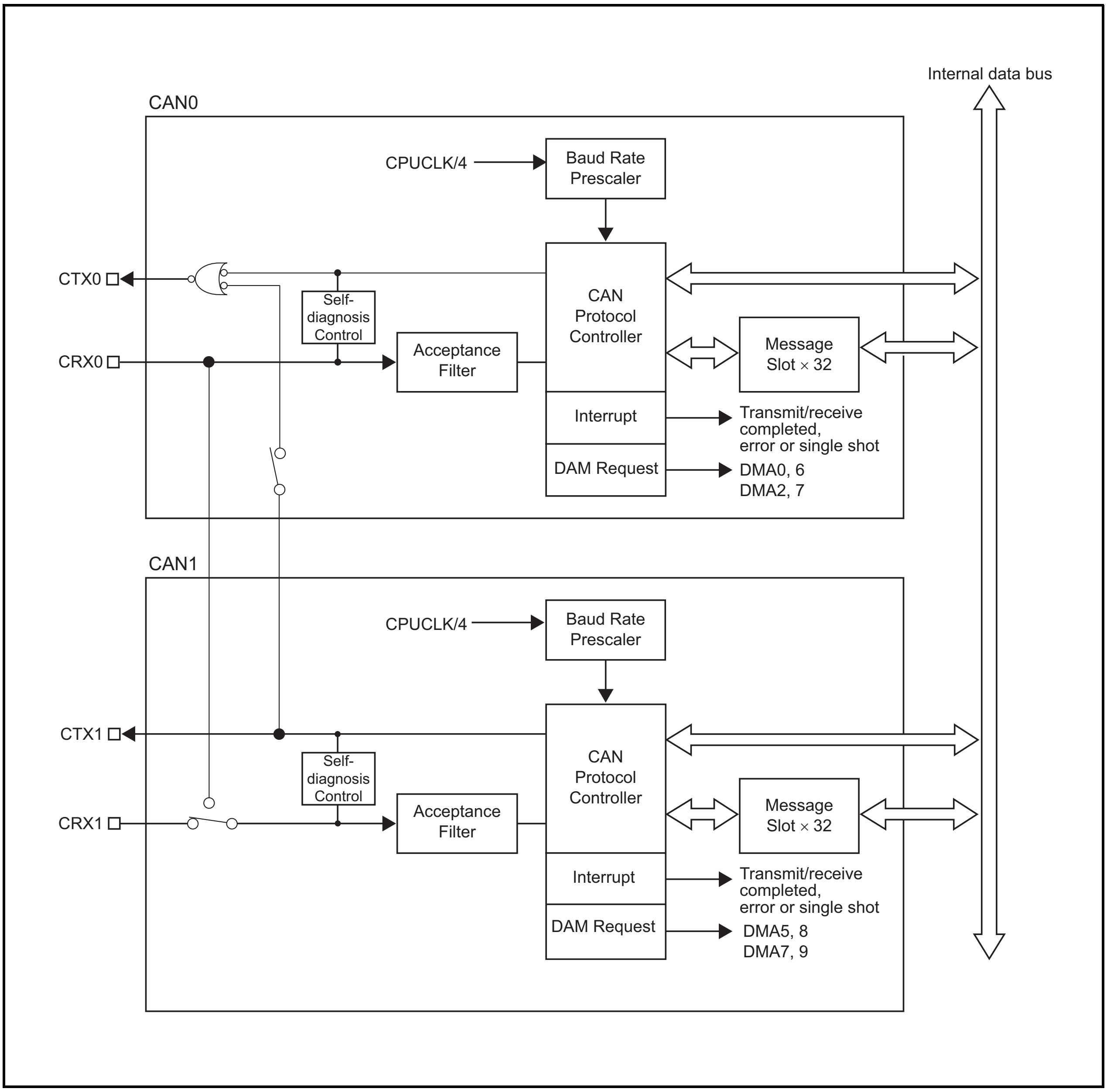


Figure 9.1.1 Block Diagram of the CAN Modules

10.1 Outline of the Direct RAM Interface (DRI)

The Direct RAM Interface (DRI) is a parallel interface used to take in parallel data into the internal RAM as it is input to the microcomputer synchronously with the clock. Since a dedicated bus provided separately from the M32R-FPU is used to write data from the DRI to the internal RAM, data can be taken in without having to stop operation of the M32R-FPU. Furthermore, a selective data capture function is supported that makes use of the internal event counter of the DRI.

Table 10.1.1 Outline of the Direct RAM Interface (DRI)

Item	Function
Transfer method	Clock synchronous parallel input
RAM access area	Entire 64 Kbytes area of the internal RAM
Received data width	Selectable from 32, 16 and 8 bits
Maximum transfer rate	20 Mbytes/sec
Minimum data capture cycle	200ns (when the special mode not selected, with input data bus width 32 bits), 175ns (when the special mode not selected, with input data bus width 16/8 bits), 100ns (when the special mode selected)
Data capture bus width	32/16/8 bits (when the special mode not selected), 16/8 bits (when the special mode selected)
Event counter	16 bits x 5 counters (DEC0–DEC4)
Bank switch function	Two banks in RAM specifiable as data storage destination
Data capture edge	Selectable from rising or falling edge or both edges
Capture timing adjust function	Timing from data capture edge detection to data sampling can be set
Selective data capture function	Data can be captured selectively using an internal event counter

Note : • When f(BCLK) = 80MHz.

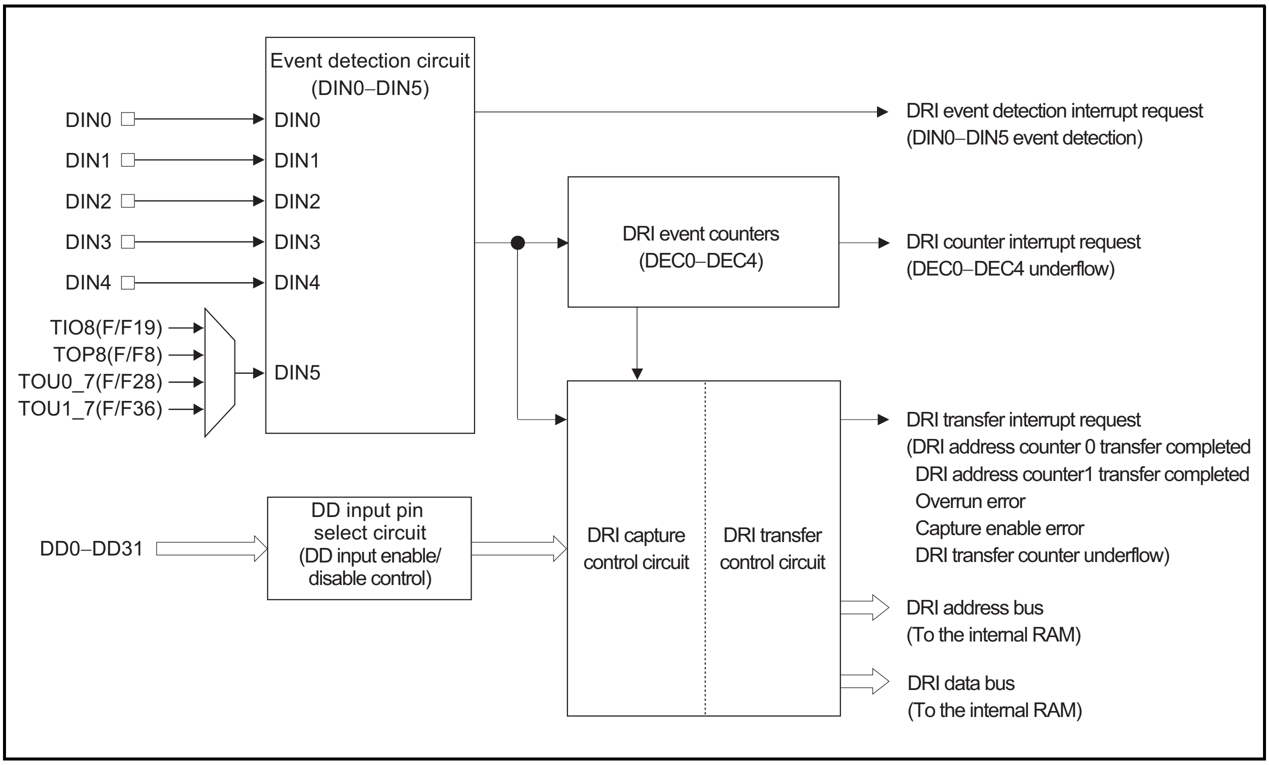


Figure 10.1.1 Block Diagram of the Direct RAM Interface (DRI)

11.1 Outline of the Real-Time Debugger (RTD)

The Real-Time Debugger (RTD) is a serial interface through which to read or write to any location in the entire area of the internal RAM by using commands from outside the microcomputer. Because data transfers between the RTD and internal RAM are performed via a dedicated internal bus independently of the M32R-FPU, RTD operation can be controlled without the need to stop the M32R-FPU.

Table 11.1.1 Outline of the Real-Time Debugger (RTD)

Item	Description
Transfer method	Clock-synchronous serial interface
Generation of transfer clock	Generated by external host
RAM access area	Entire area of the internal RAM (controlled by A14–A29)
Transmit/receive data length	32 bits (fixed)
Bit transfer sequence	LSB first
Maximum transfer rate	2 Mbits/second
Input/output pins	4 pins (RTDTXD, RTDRXD, RTDACK, RTDCLK)
Number of commands	Following five functions • Monitor continuously • Output real-time RAM content • Forcibly rewrite RAM content (with verify) • Recover from runaway condition • Request RTD interrupt

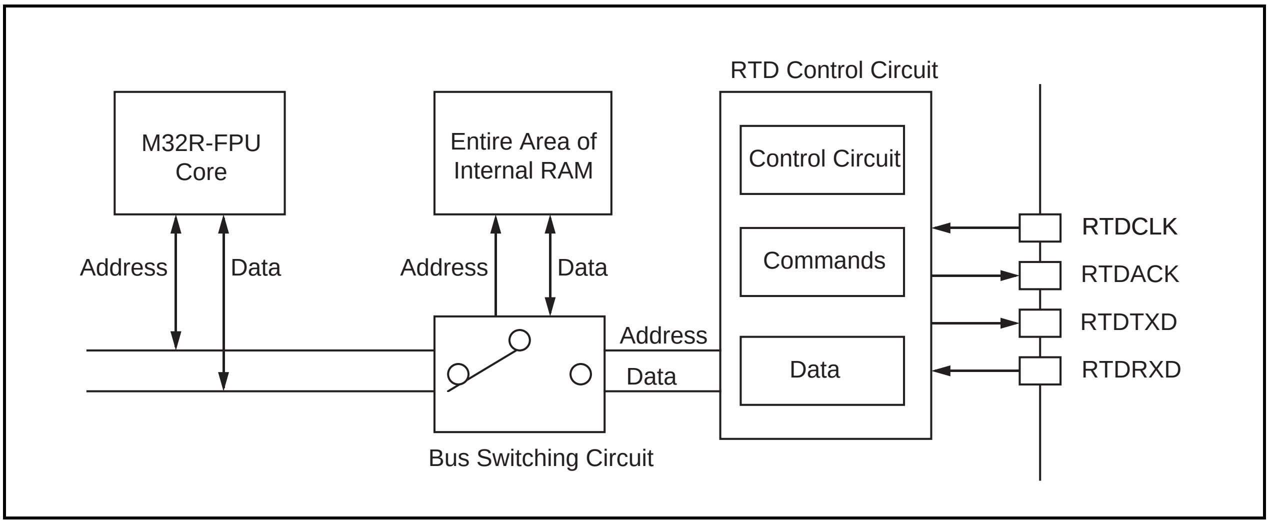


Figure 11.1.1 Block Diagram of the Real-Time Debugger (RTD)

12.1 Outline of the Non-Break Debug (NBD)

Non-Break Debug (NBD) has the RAM monitor and event output functions. A dedicated DMA is incorporated in NBD, so that accesses to the internal RAM, etc. are accomplished using this DMA.

(1) RAM monitor function

This function is provided for reading and writing to and from all resources connected to the internal/external buses mapped in the address space. It allows the RAM data, etc. to be referenced and altered. Furthermore, accesses to the address space used exclusively for NBD (i.e., NBD space) are accomplished using this function.

(2) Event output function

Upon detecting access to a preset address, this function outputs a low-level signal from the NBDEVNT# pin. A specific address and read/write access can be specified as the event occurrence condition.

Table 12.1.1 Outline of the Non-Break Debug (NBD)

Item	Content
Transfer method	Clock-synchronous parallel interface (4 bits)
Transfer clock generation	Generated by external host
Access area	All areas in the address map and NBD space
Access size	8, 16 or 32 bits (for NBD space, fixed to 8 bits)
Maximum transfer rate	12.5MHz
Input/output pins	7 pins (NBDD3–NBDD0, NBDCLK, NBDSYNC#, NBDEVNT#)
Functions	• RAM monitor function • Event output function
Number of events set	1 event

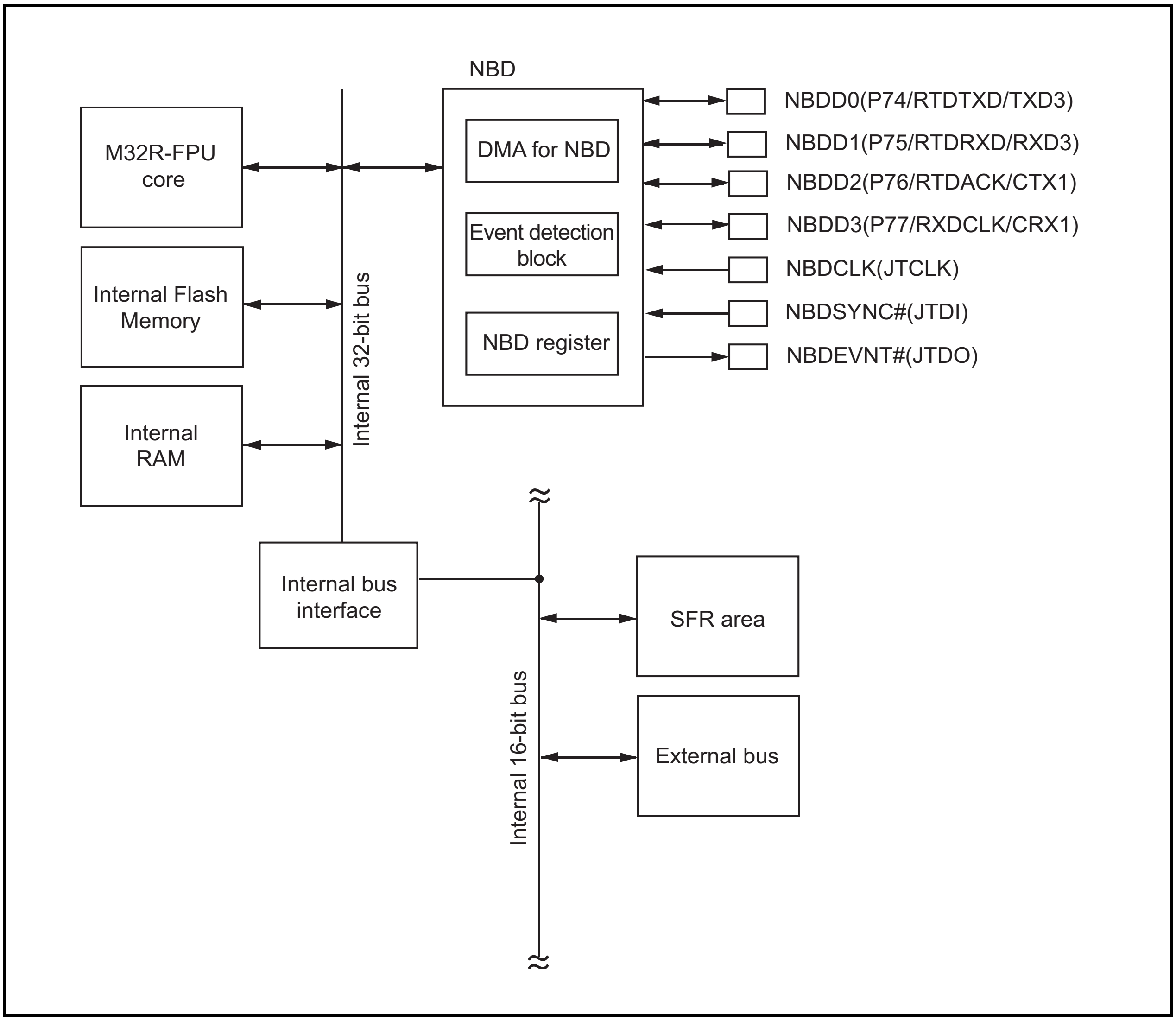


Figure 12.1.1 Block Diagram of the Non-Break Debug (NBD)

13.1 Virtual Flash Emulation Function

The microcomputer has the function to map 8-Kbyte memory blocks of the internal RAM (max. 8 blocks) into areas (L banks) of the internal flash memory that are divided in 8-Kbyte units. This functions is referred to as the Virtual Flash Emulation Function.

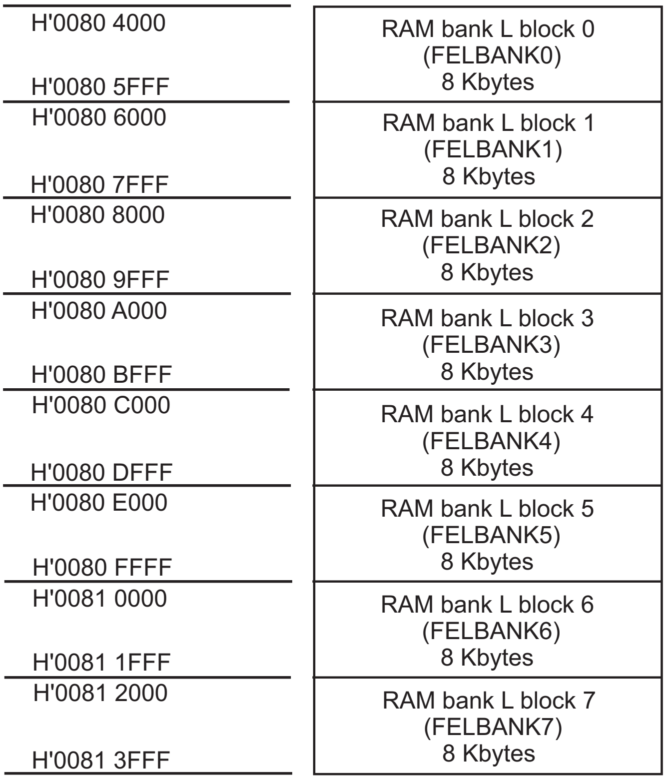
This function allows the data located in 8-Kbyte blocks of the internal RAM to be changed with the contents of internal flash memory at the addresses specified by the Virtual Flash L Bank Register. That way, the relevant RAM data can read out by reading the content of internal flash memory.

For applications that require modifying the contents of internal flash memory (e.g., data table) during operation, this function enables dynamic data modification by modifying the relevant RAM data.

The RAM blocks allocated for virtual flash emulation can be accessed for read and write the same way as in usual RAM.

This function, when used in combination with the microcomputer's internal Real-Time Debugger (RTD), allows the data table, etc. created in the internal flash memory to be referenced or rewritten from the outside, thereby facilitating data table tuning from an external device.

Note: • Before programming/erasing the internal flash memory, always be sure to exit this virtual flash emulation mode.



H'0080 4000 H'0080 5FFF	RAM bank L block 0 (FELBANK0) 8 Kbytes
H'0080 6000 H'0080 7FFF	RAM bank L block 1 (FELBANK1) 8 Kbytes
H'0080 8000 H'0080 9FFF	RAM bank L block 2 (FELBANK2) 8 Kbytes
H'0080 A000 H'0080 BFFF	RAM bank L block 3 (FELBANK3) 8 Kbytes
H'0080 C000 H'0080 DFFF	RAM bank L block 4 (FELBANK4) 8 Kbytes
H'0080 E000 H'0080 FFFF	RAM bank L block 5 (FELBANK5) 8 Kbytes
H'0081 0000 H'0081 1FFF	RAM bank L block 6 (FELBANK6) 8 Kbytes
H'0081 2000 H'0081 3FFF	RAM bank L block 7 (FELBANK7) 8 Kbytes

Figure 13.1.1 Internal RAM Bank Configuration of the 32186

14.1 Outline of the Wait Controller

The Wait Controller controls the number of wait states inserted in bus cycles when accessing an external extension area. The Wait Controller is outlined in the table below.

Table 14.1.1 Outline of the Wait Controller

Item	Description
Target space	Control is applied to the following address spaces depending on operation mode: Single-chip mode: No target space (Settings of the Wait Controller have no effect) External extension mode: CS0 area (7 Mbytes), CS1 area (8 Mbytes), CS2 area (8 Mbytes), CS3 area (8 Mbytes) Processor mode: CS0 area (8 Mbytes), CS1 area (8 Mbytes), CS2 area (8 Mbytes), CS3 area (8 Mbytes)
Number of wait states	0–15 wait states set by software + any number of wait states set from the WAIT# pin that can be inserted

During external extension and processor modes, four chip select signals (CS0# to CS3#) are output, each corresponding to one of the four external extension areas referred to as CS0 through CS3.

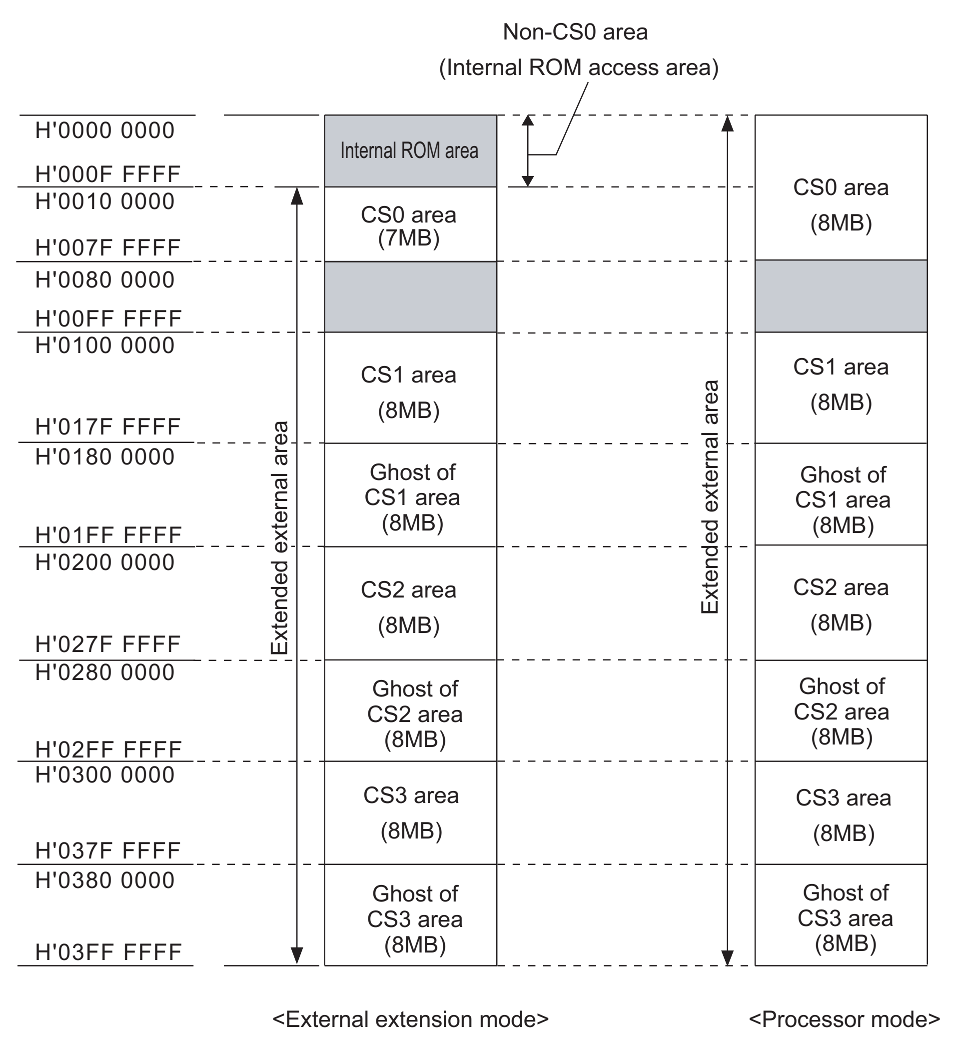


Figure 14.1.1 CS0–CS3 Area Address Map

When accessing the external extension area, the Wait Controller controls the number of wait states inserted in bus cycles based on the number of wait states set by software and the input signal entered from the WAIT# pin.
The number of wait states that can be controlled in software is 0 to 15.
When the input signal on the WAIT# pin is sampled low in the last cycle of internal wait state, the wait state is extended as long as the WAIT# input signal is held low. Then when the WAIT# input signal is released back high, the wait state is terminated and the next new bus cycle is entered into.

Table 14.1.2 Number of Wait States that Can Be Set by the Wait Controller

External extension Area	Address	Number of Wait States Inserted
CS0 area	H'0010 0000 to H'007F FFFF (external extension mode) H'0000 0000 to H'007F FFFF (processor mode)	Zero to 15 wait states set by software + any number of wait states entered from the WAIT# pin (However, software settings have priority.)
CS1 area (Note 1)	H'0100 0000 to H'017F FFFF (external extension and processor modes)	Zero to 15 wait states set by software + any number of wait states entered from the WAIT# pin (However, software settings have priority.)
CS2 area (Note 2)	H'0200 0000 to H'027F FFFF (external extension and processor modes)	Zero to 15 wait states set by software + any number of wait states entered from the WAIT# pin (However, software settings have priority.)
CS3 area (Note 3)	H'0300 0000 to H'037F FFFF (external extension and processor modes)	Zero to 15 wait states set by software + any number of wait states entered from the WAIT# pin (However, software settings have priority.)

Note 1: A ghost (8 Mbytes) of the CS1 area will appear in the H'0180 0000 to H'01FF FFFF area.
Note 2: A ghost (8 Mbytes) of the CS2 area will appear in the H'0280 0000 to H'02FF FFFF area.
Note 3: A ghost (8 Mbytes) of the CS3 area will appear in the H'0380 0000 to H'03FF FFFF area.

15.1 Instruction Set

CPU Instruction Set

The M32R employs a RISC architecture, supporting a total of 100 discrete instructions.

(1) Load/store instructions

Perform data transfer between memory and registers

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

(2) Transfer instructions

Perform register to register transfer or register to immediate transfer

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

(3) Branch instructions

Used to change the program flow

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

(4) Arithmetic/logic instructions

Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers

• Comparison

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• Logical operation

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

• Arithmetic operation

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add (with overflow checking)
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract (with overflow checking)
SUBX	Subtract with borrow

• Multiplication/division

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

• Shift

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

(5) Instructions for the DSP function

Perform 32-bit x 16-bit or 16-bit x 16-bit multiplication or sum-of-products calculation

These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order halfword
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

(6) EIT related instructions

Start trap or return from EIT processing

RTE	Return from EIT
TRAP	Trap

(7) Instructions for the FPU function

The microcomputer supports fully IEEE754 compliant, single-precision floating-point arithmetic.

FADD	Floating-point add
FSUB	Floating-point subtract
FMUL	Floating-point multiply
FDIV	Floating-point divide
FMADD	Floating-point multiply and add
FMSUB	Floating-point multiply and subtract
ITOF	Integer to float
UTOF	Unsigned to float
FTOI	Float to integer
FTOS	Float to short
FCMP	Floating-point compare
FCMPE	Floating-point compare with exception if unordered

(8) Extended instructions

STH	Store halfword (@R+ addressing added)
BSET	Bit set
BCLR	Bit clear
BTST	Bit test
SETPSW	Set PSW
CLRPSW	Clear PSW

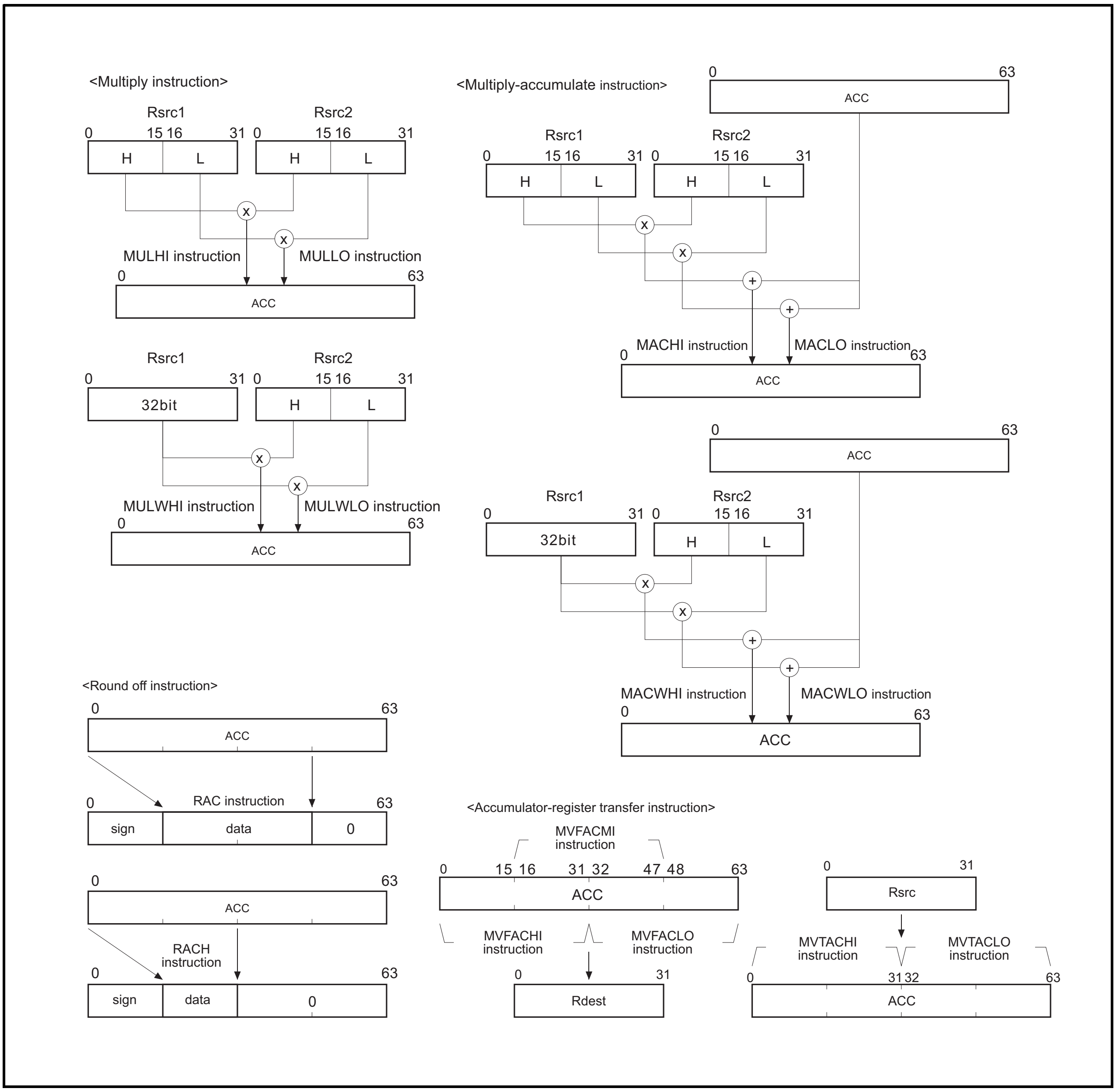
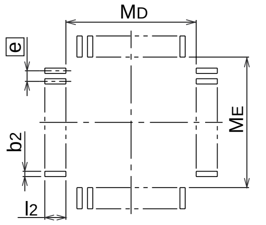


Figure 15.1.1 Instructions for the DSP Function

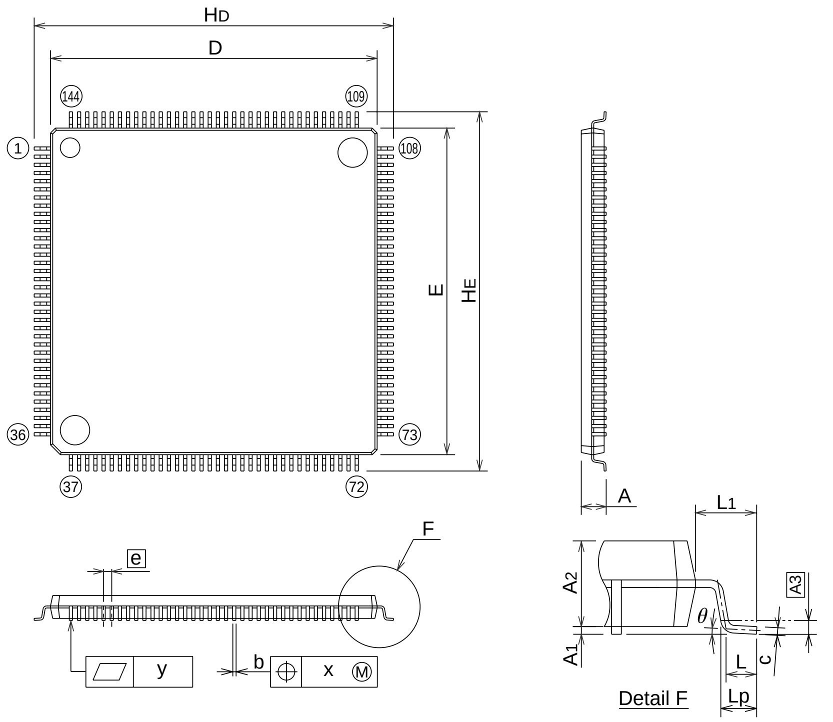
16.1 Package Dimensions

144P6Q-A Recommended **Plastic 144pin 20×20mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy



Recommended Mount Pad



Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.125	0.2
A_2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
L	0.35	0.5	0.65
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A_3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.225	–
l_2	0.95	–	–
M_D	–	20.4	–
M_E	–	20.4	–

REVISION HISTORY	32186 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 01, 2004	–	First edition issued

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