Main Features

- **8-bit Resolution**
- **500 Msps (min) Sampling Rate**
- **Power Consumption: 3.8W Typ**
- **500 mVpp Differential or Single-ended Analog Inputs**
- **Differential or Single-ended 50Ω ECL Compatible Clock Inputs**
- **ECL or LVDS/HSTL Output Compatibility**
- **ADC Gain Adjust**
- **Data Ready Output with Asynchronous Reset**
- **Gray or Binary Selectable Output Data; NRZ Output Mode**
- **Enhanced CBGA Package with Ceramic Lid**
- **Evaluation Board: TSEV8308500GL (Detailed Specification on Request)**
- **Demultiplexer TS81102G0: Companion Device Available**

Performance

- **1.3 GHz Full Power Input Bandwidth**
- **Band Flatness: 0.5 dB up to 500 MHz**
- **SINAD = 45 dB (7.2 Effective Bits), SFDR = 54 dBc at F_S = 500 Msps, F_{IN} = 20 MHz**
- **SINAD = 43 dB (7.1 Effective Bits), SFDR = 53 dBc at F_S = 500 Msps, F_{IN} = 250 MHz**
- **SINAD = 42 dB (7.0 Effective Bits), SFDR = 52 dBc at F_S = 500 Msps, F_{IN} = 500 MHz (-3 dB FS)**
- **2-tone IMD: TBD (199.5 MHz, 200.5 MHz) at 500 Msps**
- **DNL = ±0.3 LSB INL = ±0.7 LSB**
- **Low Bit Error Rate (10^{-13}) at 500 Msps, Tj = 90°C**

Applications

- Digital Sampling Oscilloscopes
- Satellite Receiver
- Electronic Countermeasures/Electronic Warfare
- Direct RF Down-conversion

Screening

- Atmel Standard Screening Level
- Temperature Range:
    - 0°C < Tc; Tj < +90°C
    - -40°C < Tc ; Tj < + 110°C

Description

The TS8308500 is a monolithic 8-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 500 Msps.

The TS8308500 is using an innovative architecture, including an on-chip Sample and Hold (S/H), and is fabricated with an advanced high-speed bipolar process.

The on-chip S/H has a 1.3 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (High IF digitizing).
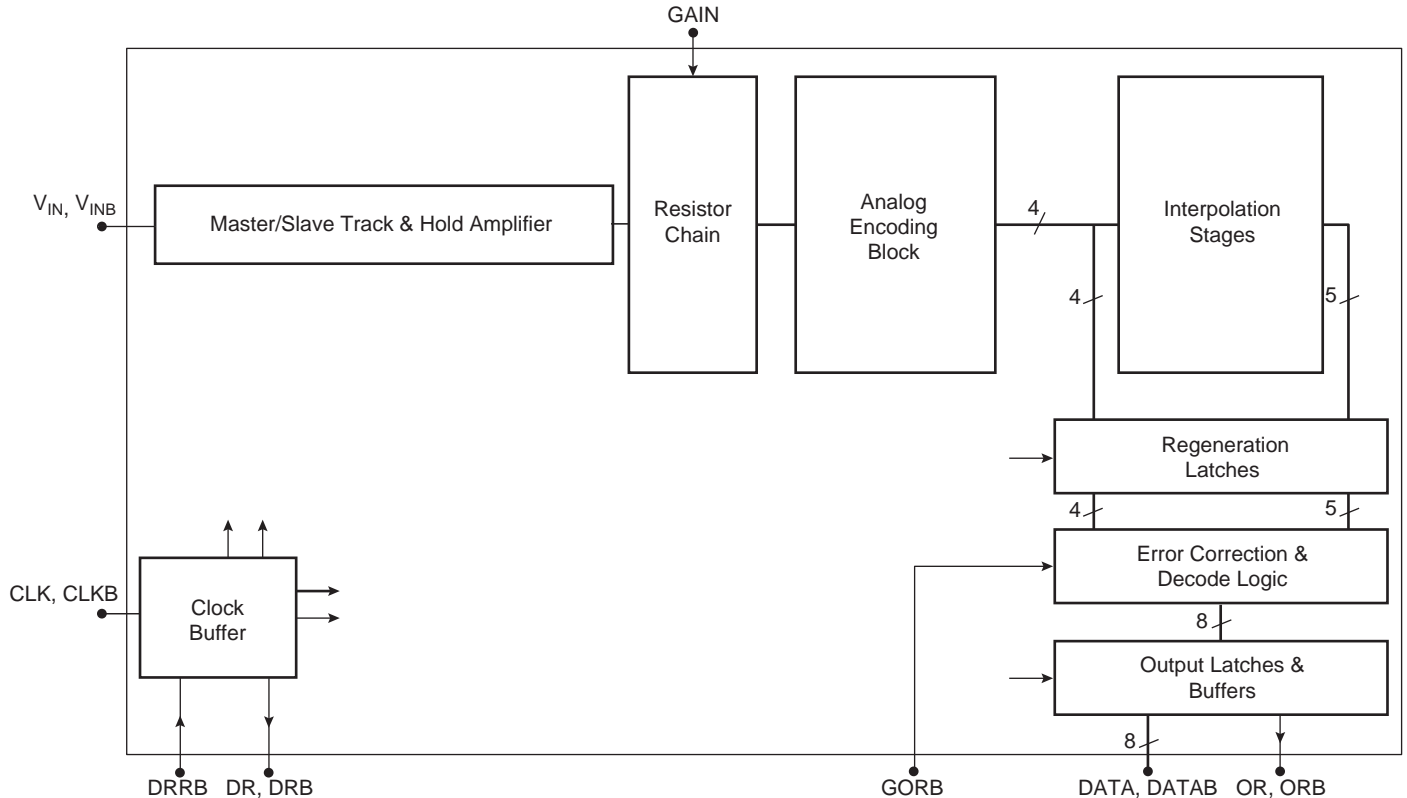
ADC 8-bit 500 Msps

TS8308500

Functional Description

Block Diagram

Figure 1. Simplified Block Diagram

Functional Description

The TS8308500 is an 8-bit 500 Msps ADC based on an advanced high-speed bipolar technology featuring a cutoff frequency of 25 GHz.

The TS8308500 includes a front-end master/slave Track and Hold stage (S/H), followed by an analog encoding stage and interpolation circuitry.

Successive banks of latches are regenerating the analog residues into logical data before entering an error correction circuitry and a resynchronization stage followed by 75Ω differential output buffers.

The TS8308500 works in fully differential mode from analog inputs up to digital outputs.

The TS8308500 features a full-power input bandwidth of 1.3 GHz.

Control pin GORB is provided to select either the Gray or Binary data output format.

The gain control pin is provided in order to adjust the ADC gain.

A Data Ready output asynchronous reset (DRRB) is available on TS8308500.

The TS8308500 uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allow enhanced radiation tolerance (no performance drift measured at 150 kRad total dose).

Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND -0.3 to 2.8	V
Negative supply voltage	V_{EE}		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to 1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-2 to 2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} 0.3	V
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to 0.9	V
Digital output voltage	V_O		V_{PLUSD} -3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to 1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-2 to 2	V
Maximum junction temperature	T_j		135	°C
Storage temperature	T_{stg}		-65 to 150	°C
Lead temperature (soldering 10s)	T_{leads}		300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability. The use of a thermal heat sink is mandatory (see Thermal characteristics).

Recommended Conditions of Use

Table 2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value			Unit
			Min	Typ	Max	
Positive supply voltage	V_{CC}		4.75	5	5.25	V
Positive digital supply voltage	V_{PLUSD}	ECL output compatibility	–	GND	–	V
Positive digital supply voltage	V_{PLUSD}	LVDS output compatibility	1.4	2.4	2.6	V
Negative supply voltages	V_{EE}, DV_{EE}		-5.25	-5	-4.75	V
Differential analog input voltage (full-scale)	V_{IN}, V_{INB} V_{IN} - V_{INB}	50Ω differential or single-ended	±113 450	±125 500	±137 550	mV mVpp
Clock input power level	P_{CLK}, P_{CLKB}	50Ω single-ended clock input	3	4	10	dBm
Operating temperature range	T_J	Commercial grade: "C" Industrial grade "V"	0 < Tc; Tj < 90 -40 < Tc; Tj < 110			°C

Electrical Operating Characteristics

$V_{EE} = DV_{EE} = -5V$; $V_{CC} = +5V$; $V_{IN} - V_{INB}$ = 500 mVpp Full Scale differential input

50Ω differentially terminated digital outputs

Tj (typical) = 70°C

Table 3. Electrical Specifications

Parameter	Symbol	Test Level	Value Min	Value Typ	Value Max	Unit	Note
Power Requirements							
Positive supply voltage							
Analog	V_{CC}	1	4.5	5	5.5	V	
Digital (ECL)	V_{PLUSD}	4	–	0	–	V	
Digital (LVDS)	V_{PLUSD}	4	1.4	2.4	2.6	V	
Positive supply current							
Analog	I_{CC}	1	–	420	445	mA	
Digital	I_{PLUSD}	1	–	130	145	mA	
Negative supply voltage	V_{EE}	1	-5.5	-5	-4.5	V	
Negative supply current							
Analog	AI_{EE}	1	–	185	200	mA	
Digital	DI_{EE}	1	–	160	180	mA	
Nominal power dissipation	PD	1	–	3.9	4.1	W	
Power supply rejection ratio	PSRR	4	–	0.5	2	mW	
Resolution	–	–	–	–	8	bits	[2]
Analog Inputs							
Full-scale input voltage range (differential mode)	V_{IN}	4	-125	–	125	mV	
(0V common mode voltage)	V_{INB}	–	-125	–	125	mV	
Full-scale input voltage range (single-ended input option) [14]	V_{IN}	4	-250	–	250	mV	
	V_{INB}	–	–	0	–	mV	
Analog input capacitance	C_{IN}	4	–	3	3.5	pF	
Input bias current	I_{IN}	4	–	10	20	µA	
Input Resistance	R_{IN}	4	0.5	1	–	MΩ	
Full Power input Bandwidth (-3 dB)	FPBW	4	–	1.8	–	GHz	
Small signal input Bandwidth (10% full-scale)	SSBW	4	–	1.7	–	GHz	
Clock Inputs							
Logic compatibility for clock inputs [14]	–	–	ECL or specified clock input power level in dBm			–	[8]
ECL Clock inputs voltages (V_{CLK} or V_{CLKB}):	–	4	–	–	–	–	
Logic 0 voltage	V_{IL}	–	–	–	-1.5	V	
Logic 1 voltage	V_{IH}	–	-1.1	–	–	V	
Logic 0 current	I_{IL}	–	–	5	50	µA	
Logic 1 current	I_{IH}	–	–	5	50	µA	
Clock input power level into 50Ω termination	–	–	dBm into 50Ω			–	

Table 3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	**Typ**	**Max**		
Clock input power level	–	4	-2	4	10	dBm	
Clock input capacitance	C_{CLK}	4	–	3	3.5	pF	
Digital Outputs Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), binary output data format, Tj (typical) = 70°C. Full temperature range: 0°C < Tc; Tj < +90°C or -40°C < Tc ; Tj < 110°C							(1)(6)
Logic compatibility for digital outputs (Depending on the value of V_{PLUSD}) (14)	–	–	ECL or LVDS			–	
Differential output voltage swings (assuming V_{PLUSD} = 0V):	–	4	–	–	–	–	
75Ω open transmission lines (ECL levels)	–	–	1.5	1.620	–	V	
75Ω differentially terminated	–	–	0.70	0.825	–	V	
50Ω differentially terminated	–	–	0.54	0.660	–	V	
Output levels (assuming V_{PLUSD} = 0V) 75Ω open transmission lines:	–	4	–	–	–	–	(6)
Logic 0 voltage	V_{OL}	–	–	-1.62	-1.54	V	
Logic 1 voltage	V_{OH}	–	-0.88	-0.8	–	V	
Output levels (assuming V_{PLUSD} = 0V) 75Ω differentially terminated:	–	4	–	–	–	–	(6)
Logic 0 voltage	V_{OL}	–	–	-1.41	-1.34	V	
Logic 1 voltage	V_{OH}	–	-1.07	-1	–	V	
Output levels (assuming V_{PLUSD} = 0V) 50Ω differentially terminated:	–	–	–	–	–	–	(6)
Logic 0 voltage	V_{OL}	1, 2	–	-1.40	-1.32	V	
Logic 1 voltage	V_{OH}	1, 2	-1.16	-1.10	–	V	
Differential Output Swing	DOS	4	270	300	–	mV	
Output level drift with temperature	–	4	–	–	1.6	mV/°C	
DC Accuracy Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), Binary output data format Tj (typical) = 70°C							
Differential non linearity	DNL-	1	-0.6	-0.4	–	lsb/V	(2)(3)
Differential non linearity	DNL+	1	–	0.4	0.6	lsb/V	
Integral non linearity	INL-	1	-1.2	-0.7	–	lsb/V	(2)(3)
Integral non linearity	INL+	1	–	0.7	1.2	lsb/V	
No missing codes	–		Guaranteed over specified temperature range				(3)
Gain	–	1, 2	90	98	110	%/V	
Input offset voltage	–	1, 2	-26	-5	26	mV/V	

Table 3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value Min	Value Typ	Value Max	Unit	Note
Gain error drift	–	4	100	125	150	ppm/°C	
Offset error drift	–	4	40	50	60	ppm/°C	
Transient Performance							
Bit error rate F_S = 500 Msps, F_{IN} = 62.5 MHz	BER	4	–	–	1E-13	Error/ sample	(2)(4)
ADC settling time V_{IN} -V_{INB} = 400 mVpp	TS	4	–	0.5	1	ns	(2)
Overvoltage recovery time	TOR	4	–	0.5	1	ns	(2)
AC Performance Single-ended or differential input and clock mode, 50% clock duty cycle (CLK, CLKB), binary output data format, Tj = 70°C, unless otherwise specified							
Signal to noise and distortion ratio	SINAD	–	–	–	–	–	(2)
F_S = 500 Msps, F_{IN} = 20 MHz	–	4	43	45	–	dB	
F_S = 500 Msps, F_{IN} = 500 MHz	–	4	42	44	–	dB	
F_S = 500 Msps, F_{IN} = 1000 MHz (-1 dBFS)	–	4	38	40	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz	–	1	43	46	–	dB	
Effective number of bits	ENOB	–	–	–	–	–	
F_S = 500 Msps, F_{IN} = 20 MHz	–	4	7.0	7.2	–	Bits	
F_S = 500 Msps, F_{IN} = 500 MHz	–	4	6.8	7.0	–	Bits	
F_S = 500 Msps, F_{IN} = 1000 MHz (-1 dBFS)	–	4	6.0	6.3	–	Bits	
F_S = 50 Msps, F_{IN} = 25 MHz	–	1	7.0	7.4	–	Bits	
Signal to noise ratio	SNR	–	–	–	–	–	(2)
F_S = 500 Msps, F_{IN} = 20 MHz	–	4	44	46	–	dB	
F_S = 500 Msps, F_{IN} = 500 MHz	–	4	44	45	–	dB	
F_S = 500 Msps, F_{IN} = 1000 MHz (-1 dBFS)	–	4	40	43	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz	–	1	44	45	–	dB	
Total harmonic distortion	|THD|	–	–	–	–	–	(2)
F_S = 500 Msps, F_{IN} = 20 MHz		4	50	53	–	dB	
F_S = 500 Msps, F_{IN} = 500 MHz	–	4	48	50	–	dB	
F_S = 500 Msps, F_{IN} = 1000 MHz (-1 dBFS)	–	4	38	40	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz	–	1	44	54	–	dB	

Table 3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	**Typ**	**Max**		
Spurious free dynamic range	SFDR	–	–	–	–	–	(2)
F_S = 500 Msps, F_{IN} = 20 MHz	–	4	50	56	–	dBc	
F_S = 500 Msps, F_{IN} = 500 MHz	–	4	50	53	–	dBc	
F_S = 500 Msps, F_{IN} = 1000 MHz (-1 dBFS)	–	4	38	40	–	dBc	
F_S = 50 Msps, F_{IN} = 25 MHz	–	1	50	55	–	dBc	
Two-tone inter-modulation distortion	IMD	4	–	–	–	–	(2)
F_{IN1} = 199.5 MHz at F_S = 500 Msps, F_{IN2} = 200.5 MHz at F_S = 500 Msps	–	–	-47	-52	–	dBc	
Switching Performance and Characteristics – *See Figure 2 and Figure 3 on page 9*							
Maximum clock frequency	F_S	–	500	–	700	Msps	(12)
Minimum clock frequency	F_S	4	10	–	50	Msps	(13)
Minimum clock pulse width (high)	TC1	4	1.71	2	50	ns	
Minimum clock pulse width (low)	TC2	4	1.71	2	50	ns	
Aperture delay	Ta	4	100	+250	400	ps	(2)
Aperture uncertainty	Jitter	4	–	0.4	0.6	ps (rms)	(2)(5)
Data output delay	TDO	4	1150	1360	1660	ps	(2)(8)(9)(10)
Output rise/fall time for data (20%-80%)	TR/TF	4	250	350	550	ps	(9)
Output rise/fall time for data ready (20%-80%)	TR/TF	4	250	350	550	ps	(9)
Data ready output delay	TDR	4	1110	1320	1620	ps	(2)(8)(9)(10)
Data ready reset delay	TRDR	4	–	720	1000	ps	
Data to data ready – Clock low pulse width (See "Timing Diagrams" on page 9)	TOD-TDR	4	0	40	80	ps	(7)(11)(12)
Data to data ready output delay (50% duty cycle) at 1 Gsps (See "Timing Diagrams" on page 9)	TD1	4	920	960	1000	ps	(2)(13)
Data pipeline delay	TPD	4	4			clock cycles	

Notes:
1. Differential output buffers are internally loaded by 75Ω resistors. Buffer bias current = 11 mA
2. See "Definition of Terms" on page 46
3. Histogram testing based on sampling of a 10 MHz sinewave at 50 Msps
4. Output error amplitude < ±4 lsb around worst code
5. Maximum jitter value obtained for single-ended clock input on the die (chip on board): 200 fs
6. Digital output back termination options depicted in Application Notes
7. At 500 Msps, 50/50 clock duty cycle, TC2 = 2 ns (TC1). TDR - TOD = -100 ps (typ) does not depend on the sampling rate
8. Specified loading conditions for digital outputs:
   - 50Ω or 75Ω controlled impedance traces properly 50/75Ω terminated, or unterminated 75Ω controlled impedance traces
   - Controlled impedance traces far end loaded by 1 standard ECLinPS register from Motorola. (i.e.: 10E452) (Typical input parasitic capacitance of 1.5 pF including package and ESD protections.)
9. Termination load parasitic capacitance derating values:
   - 50Ω or 75Ω controlled impedance traces properly 50/75Ω terminated: 60 ps/pF or 75 ps per additionnal ECLinPS load

- Unterminated (source terminated) 75Ω controlled impedance lines: 100 ps/pF or 150 ps per additionnal ECLinPS termination load

10. Apply proper 50/75Ω impedance traces propagation time derating values: 6 ps/mm (155 ps/inch) for TSEV8308500GL Evaluation Board

11. Values for TOD and TDR track each other over temperature, (1% variation for TOD-TDR per 100°C temperature variation). Therefore TOD-TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TODs and TDR effect can be considered negligible. Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values (see Advanced Application Notes about "TOD-TDR Variation Over Temperature" on page 22).

12. Min value guarantees performance. Max value guarantees functionality

13. Min value guarantees functionality. Max value guarantees performance

14. Refer to product Application Notes

Timing Diagrams

Figure 2. TS8308500 Timing Diagram (500 Msps Clock Rate), Data Ready Reset, Clock Held at LOW Level
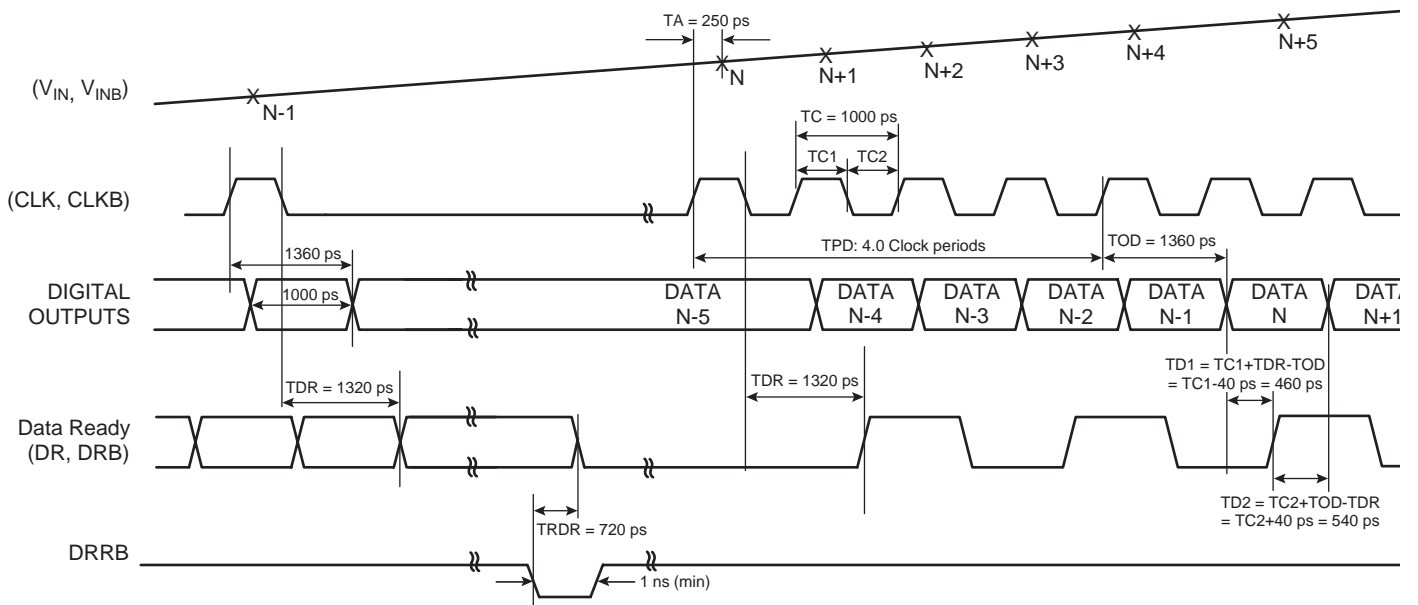
Figure 3. TS8308500 Timing Diagram (500 Msps Clock Rate), Data Ready Reset, Clock Held at HIGH Level
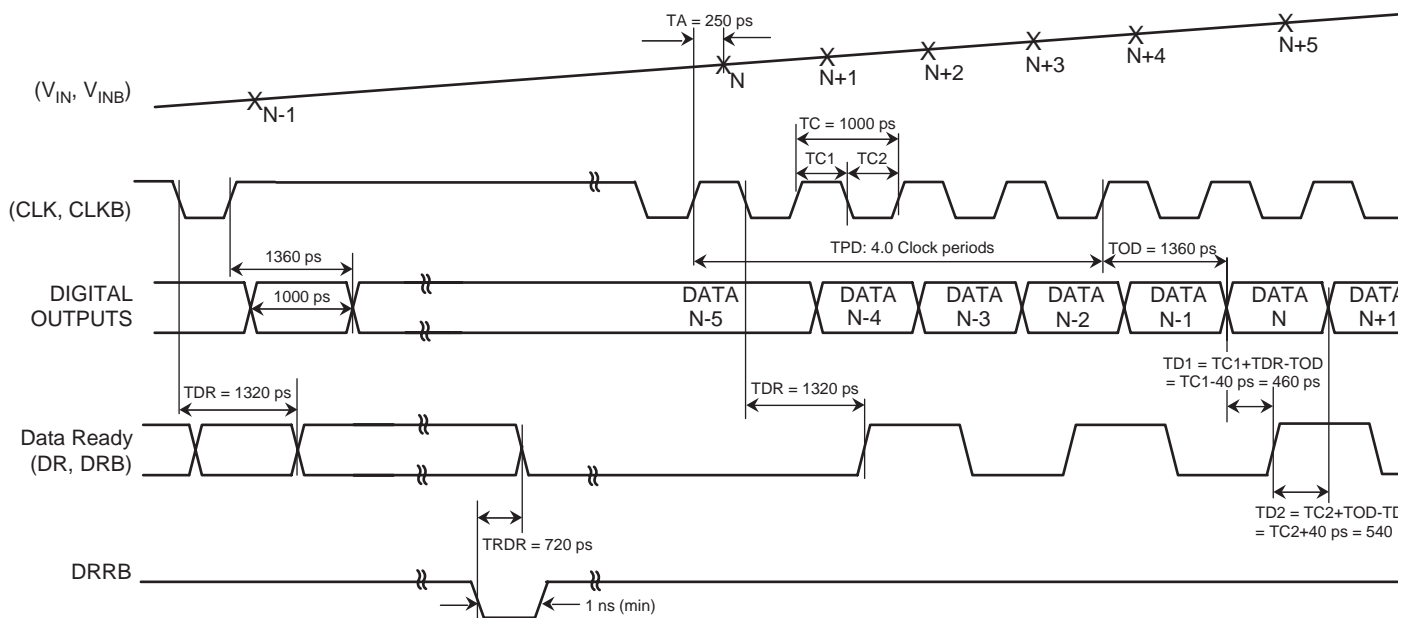
Explanation of Test Levels

Table 4. Explanation of Test Levels[3]

Num	Characteristics
1	100% production tested at +25°C[1] (for "C" Temperature range[2])
2	100% production tested at +25°C[1], and sample tested at specified temperatures (for "V" Temperature range[2])
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only

Note:
1. Unless otherwise specified, all tests are pulsed tests : therefore $T_C = T_A$ where T_C and T_A are case and ambient temperature.
2. Refer to "Ordering Information" on page 48.
3. Only min and max values are guaranteed (typical values are issued from characterization results).

Functions Description

Table 5. Functions Description

Name	Function
V_{CC}	Positive power supply
V_{EE}	Analog negative power supply
V_{PLUSD}	Digital positive power supply
GND	Ground
V_{IN}, V_{INB}	Differential analog inputs
CLK, CLKB	Differential clock inputs
<D0:D7> <D0B:D7B>	Differential output data port
DR, DRB	Differential data ready outputs
OR, ORB	Out of range outputs
GAIN	ADC gain adjust
GORB	Gray or binary digital output select
DIOD/DRRB	Die junction temperature measurement/ asynchronous data ready reset

Digital Output Coding

NRZ (Non Return to Zero) mode, ideal coding: does not include gain, offset, and linearity voltage errors.

Table 6. Digital Output Coding

Differential Analog Input	Voltage Level	Digital Output		Out of Range
		Binary GORB = VCC or Floating	Gray GORB = GND	
> +251 mV	> Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1
+251 mV	Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	0
+249 mV	Positive full-scale - 1/2 LSB	1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 1	0
+126 mV	Positive 1/2 scale + 1/2 LSB	1 1 0 0 0 0 0 0	1 0 1 0 0 0 0 0	0
+124 mV	Positive 1/2 scale - 1/2 LSB	1 0 1 1 1 1 1 1	1 1 1 0 0 0 0 0	0
+1 mV	Bipolar zero + 1/2 LSB	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	0
-1 mV	Bipolar zero - 1/2 LSB	0 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0	0
-124 mV	Negative 1/2 scale + 1/2 LSB	0 1 0 0 0 0 0 0	0 1 1 0 0 0 0 0	0
-126 mV	Negative 1/2 scale - 1/2 LSB	0 0 1 1 1 1 1 1	0 0 1 0 0 0 0 0	0
-249 mV	Negative full-scale + 1/2 LSB	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0
-251 mV	Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0
< -251 mV	< Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1

Typical Characterization Results

50/50 clock duty cycle, Binary output coding, Tj = 70°C, single-ended analog and clock inputs, unless otherwise specified.

Static Linearity

F_S = 50 Msps/F_{IN} = 10 MHz

Figure 4. Integral Non-linearity
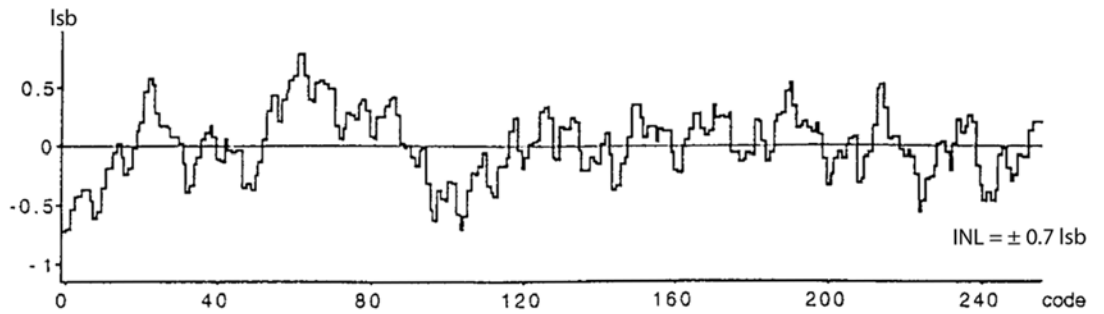
Note: Clock frequency = 50 Msps; signal frequency = 10 MHz
Positive peak: -0.68 LSB; Negative peak: -0.69 LSB

Figure 5. Differential Non-linearity
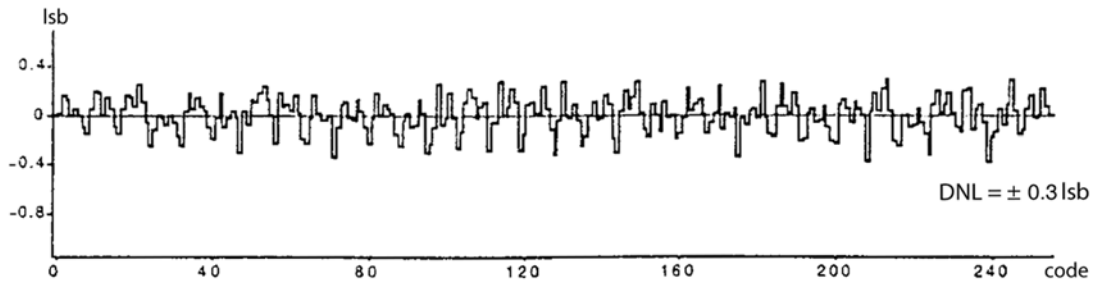
Note: Clock frequency = 50 Msps; signal frequency = 10 MHz;
Positive peak: 0.3 LSB; negative peak: -0.29 LSB

**Effective Number
of Bits Versus
Power Supply
Variation**

Figure 6. Effective Number of Bits = f (V_{EEA}); F_S = 500 Msps; F_{IN} = 100 MHz

VEEA (V)
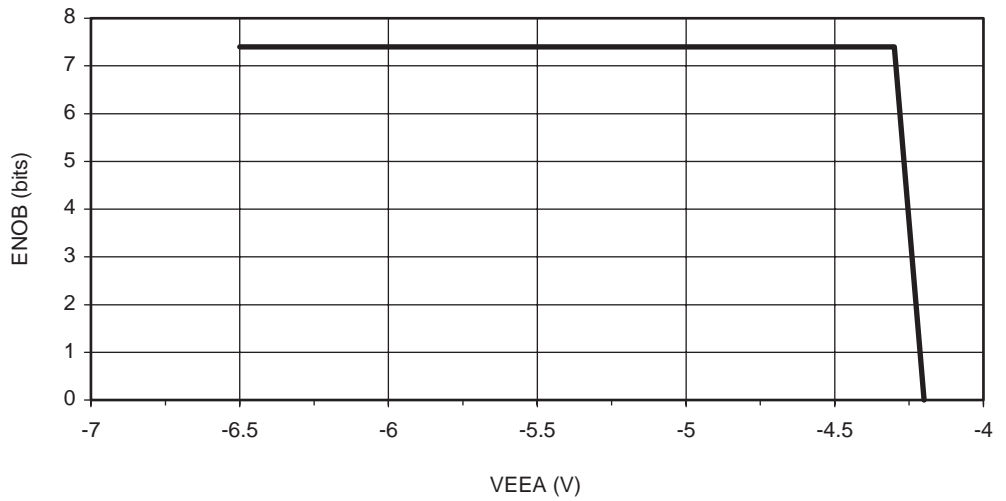
Figure 7. Effective Number of Bits = f (V_{CC}); F_S = 500 Msps; F_{IN} = 100 MHz

VCC (V)
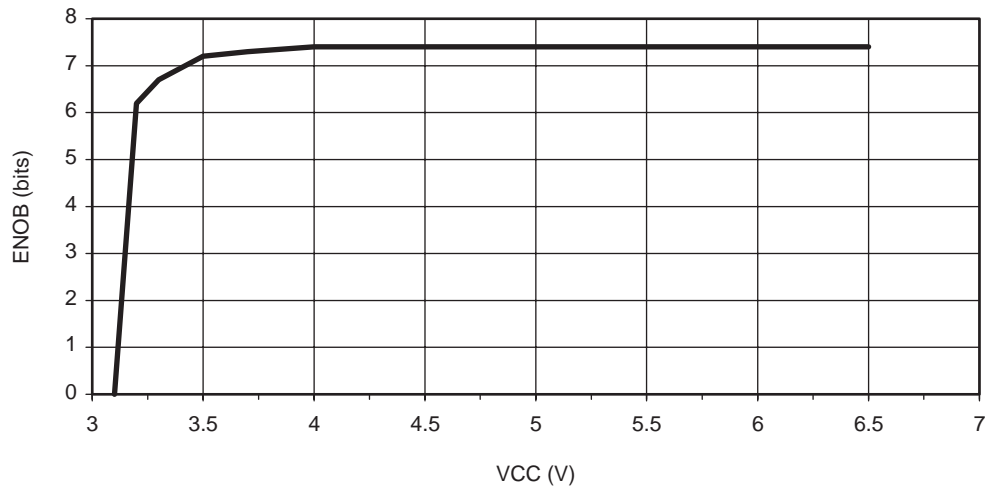
Figure 8. Effective Number of Bits = f (V_{EED}); F_S = 500 Msps; F_{IN} = 100 MHz

VEED (V)
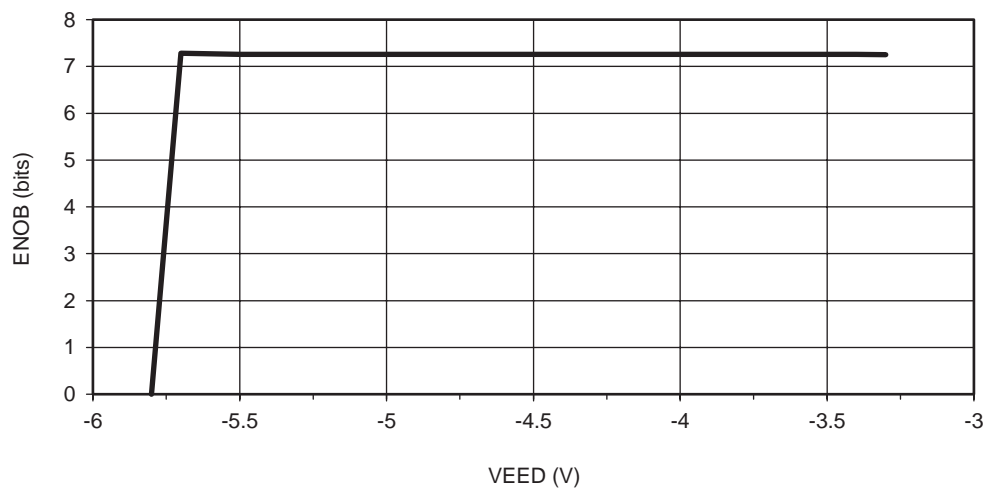
**Typical FFT
Results**

Figure 9. Spectrum for F_S = 500 Msps, F_{IN} = 498 MHz (Full Scale Input)

Acquisition of 4096 samples/FFT
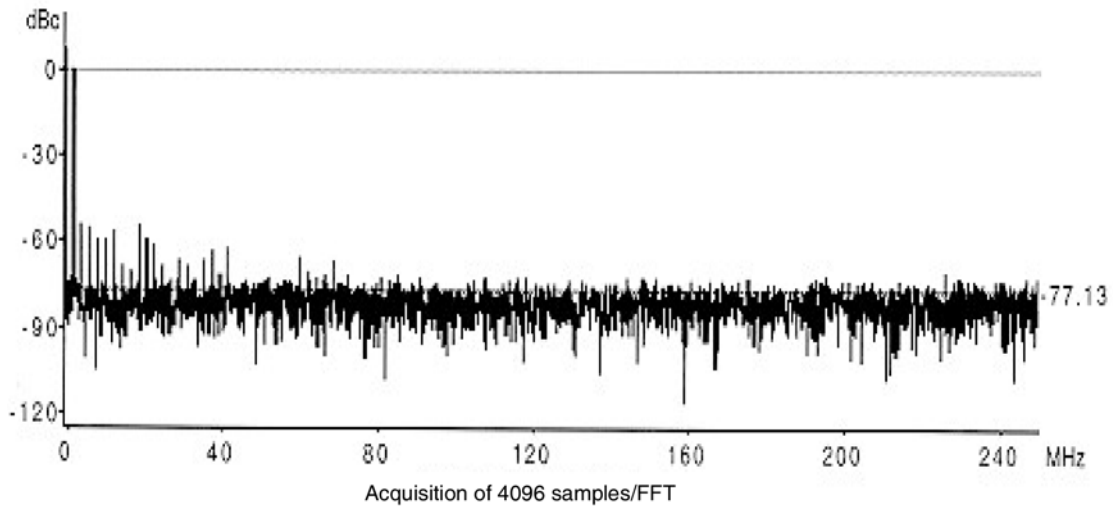
Note: Acquisition of 4096 points; THD = -49.67 dBc; F_s = 500 Msps; SINAD = 44.01 dB; F_{IN} = 498 MHz; SFDR = -54.31 dBc; SFSR = -0.94 dB; ENOB = 7.13 bits; SNR = 45.39 dB

Figure 10. Reconstructed Signal for F_S = 500 Msps, F_{IN} = 498 MHz (Full Scale Input)
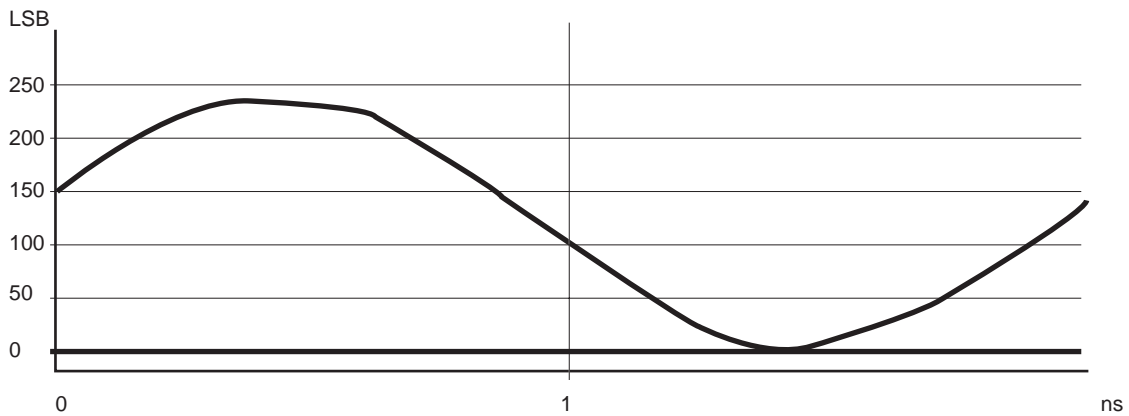
Note: Acquisition of 4096 samples; F_S = 500 Msps; Amplitude: 0.221V (114.5 LSB); F_{IN} = 498 MHz; Offset: 0V (122.5 LSB)

Figure 11. Spectrum for F_S = 500 Msps, F_{IN} = 250 MHz (Full Scale Input)
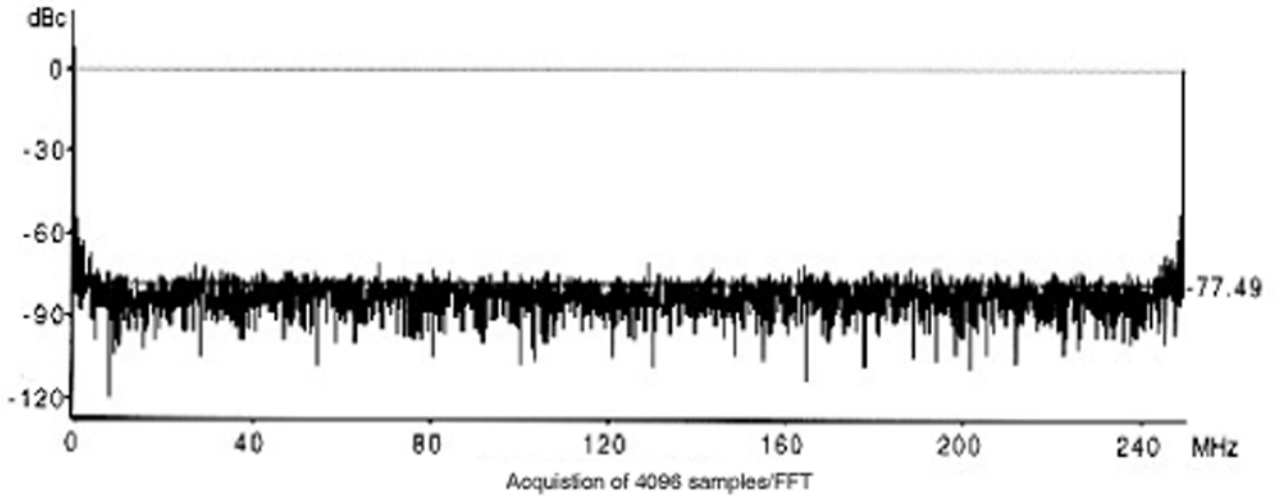
Figure 12. Reconstructed Signal for F_S = 500 Msps, F_{IN} = 250 MHz (Full Scale Input)

Note: Acquisition of 4096 samples; F_S = 500 Msps ; Amplitude: 0.189V (113.5 LSB); F_{IN} = 250 MHz ; Offset: 0V (122.5 LSB)

**Dynamic
Performance
Versus Analog
Input Frequency**

Figure 13. SFDR: F_s = 500 Msps, F_{IN} = 20 MHz up to 1000 MHz, -1dB Full Scale Input, Tj = 70°C

SFDR

Fin (MHz)
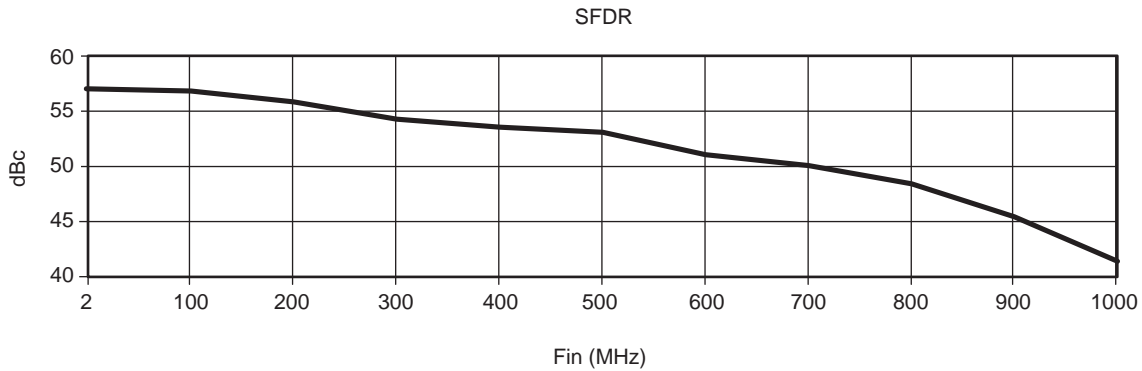
Figure 14. THD: Fs = 500 Msps, F_{IN} = 20 MHz up to 1000 MHz, -1dB Full Scale Input, Tj = 70°C

THD

Fin (MHz)
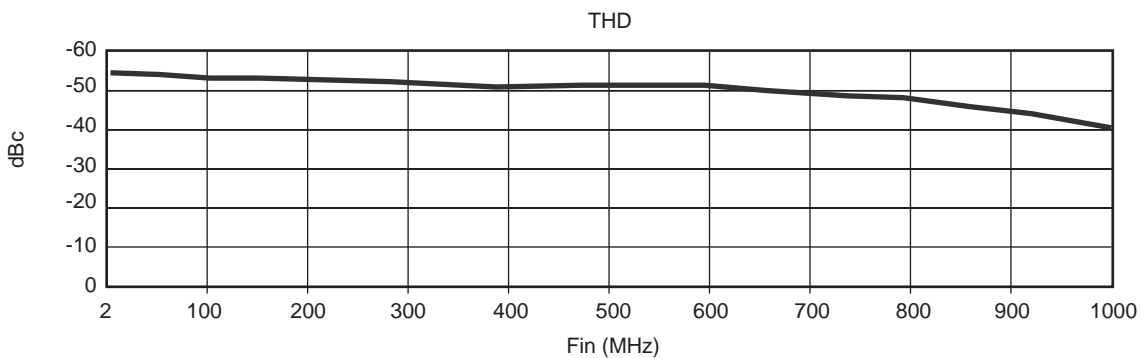
Figure 15. SINAD and SNR: Fs = 500 Msps, F_{IN} = 20 MHz up to 1000 MHz, -1dB Full Scale Input, Tj = 70°C

SINAD   SNR

Fin (MHz)
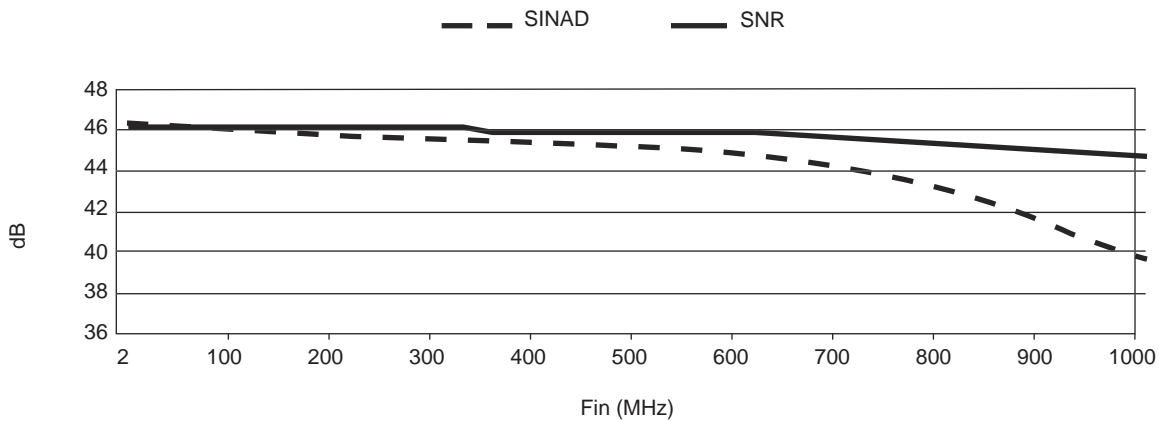
Figure 16. Fs = 500 Msps, F_{IN} = 20 MHz up to 1000 MHz, -1dB Full Scale Input, Tj = 70°C
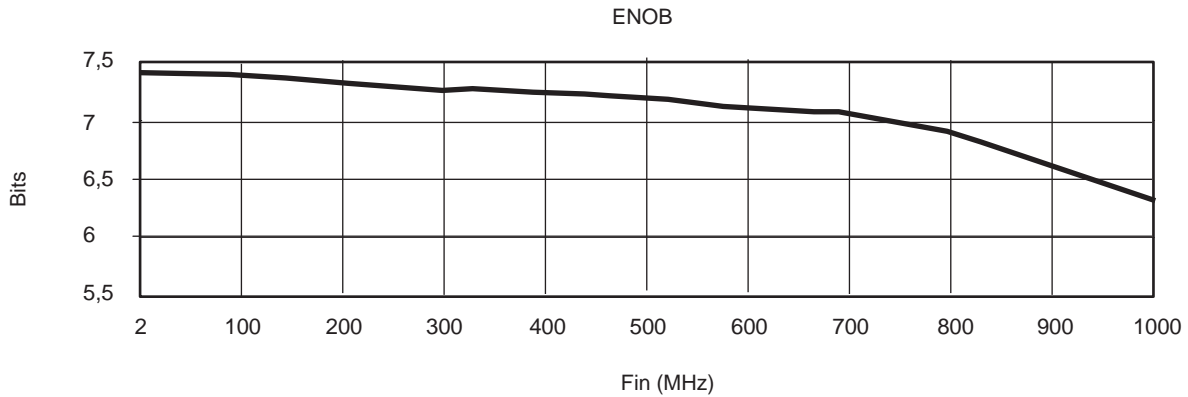
ENOB

SFDR and THD
Versus Sampling Frequency

Figure 17. Analog Input Frequency: F_{IN} = 250 MHz and Fs = 200 Msps to 1400 Msps
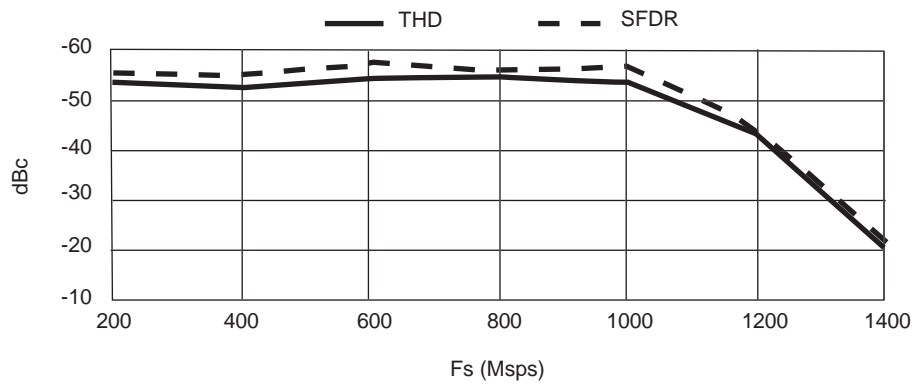
Effective Number of Bits (ENOB)
Versus Sampling Frequency

Figure 18. Analog Input Frequency: F_{IN} = 250 MHz and Fs = 200 Msps to 1400 Msps

ENOB
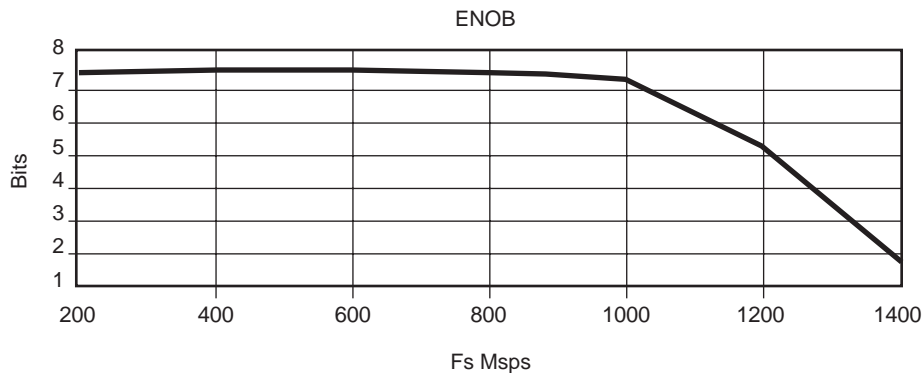
Sinad and SNR
Versus Sampling Frequency

Figure 19. Analog Input Frequency: F_{IN} = 250 MHz and F_S = 200 Msps to 1400 Msps
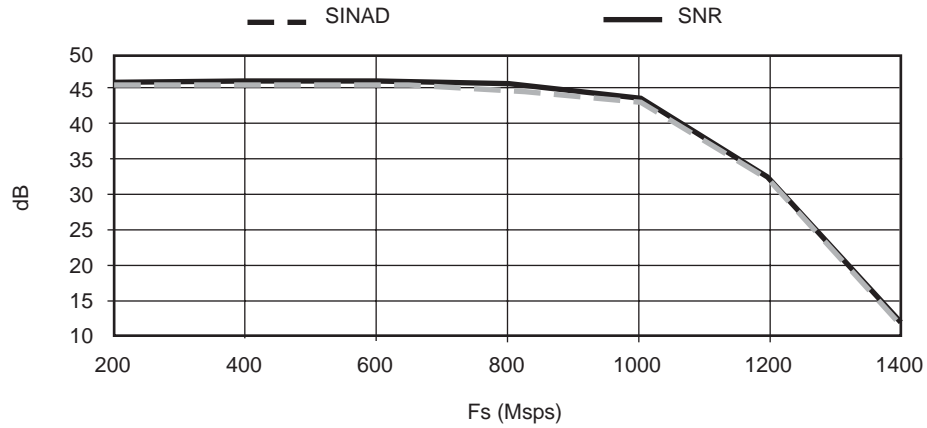
TS8308500 ADC Performances
Versus Junction Temperature

Figure 20. SFDR: F_S = 500 Msps, F_{IN} = 250 MHz, -1dB Full Scale Input, Tj = 0°C to 125°C
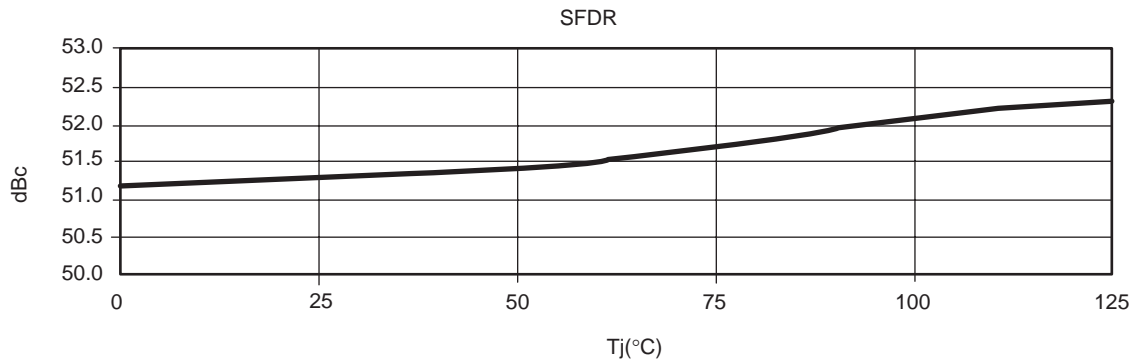
Figure 21. THD: F_S = 500 Msps, F_{IN} = 250 MHz, -1dB Full Scale Input, Tj = 0°C to 125°C

THD
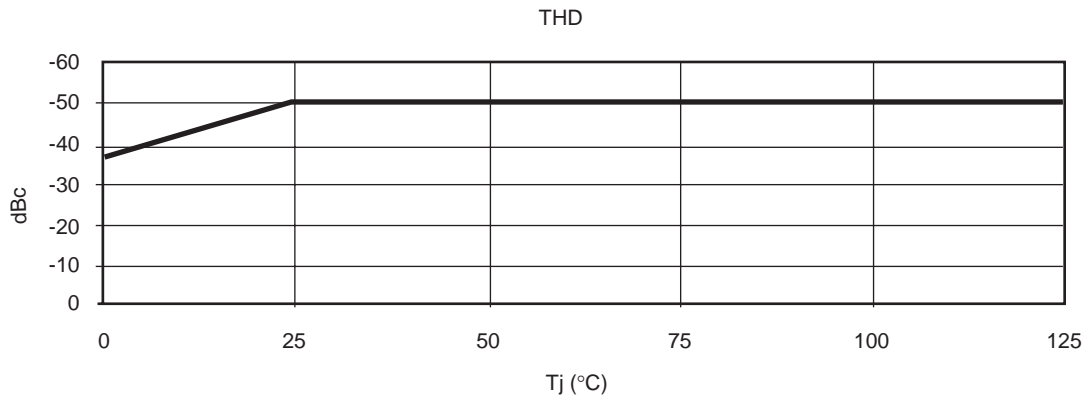
Figure 22. SINAD and SNR: F_S = 500 Msps, F_{IN} = 250 MHz, -1dB Full Scale Input, Tj = 0°C to 125°C
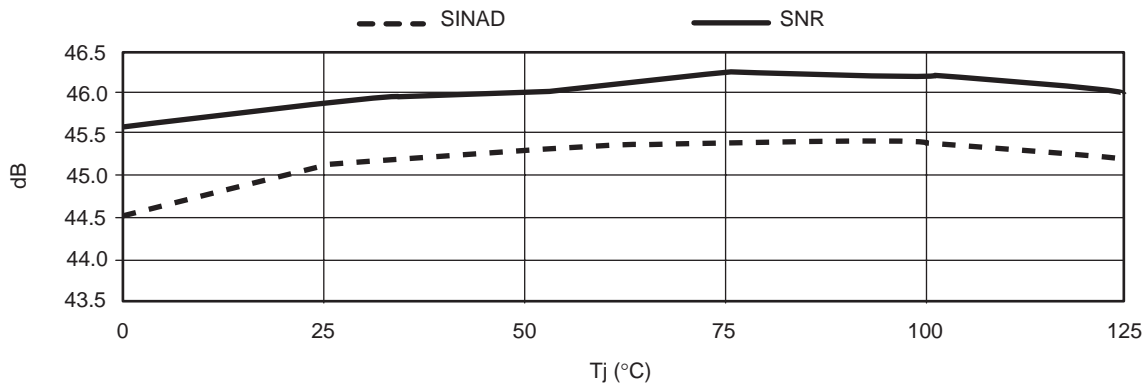
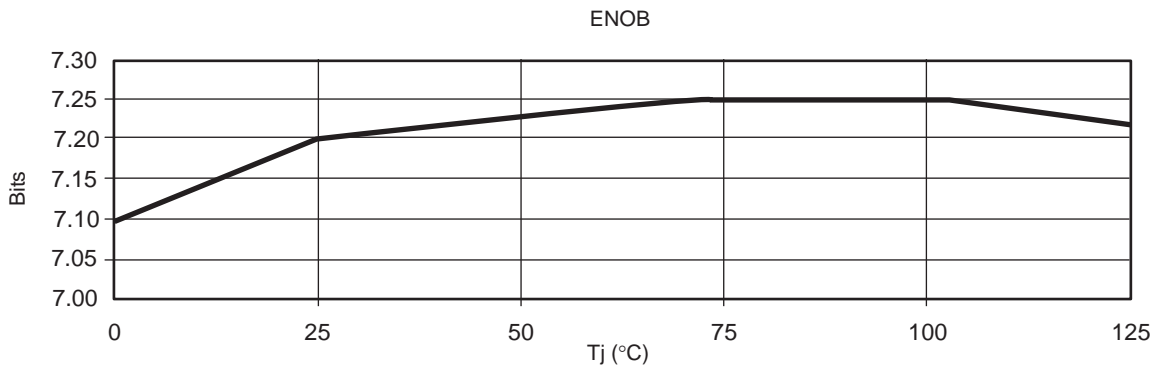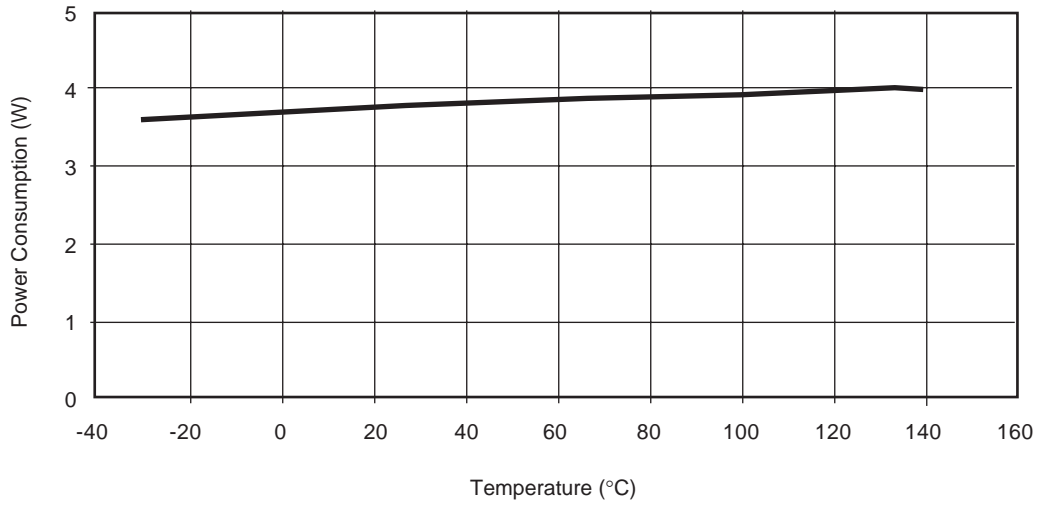**Figure 23.** ENOB: F_S = 500 Msps, F_{IN} = 250 MHz, -1dB Full Scale Input, Tj = 0°C to 125°C
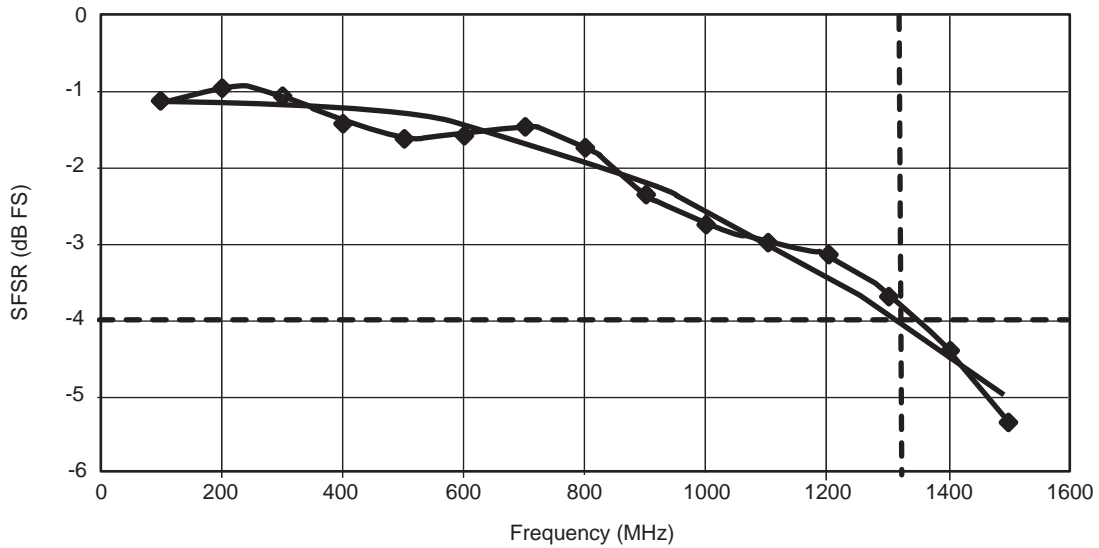
ENOB

Figure 24. Power Consumption Versus Junction Temperature: F_S = 500 Msps; F_{IN} = 250 MHz; Duty cycle = 50%

Typical Full Power Input Bandwidth

Figure 25. Band Flatness at 1.3 GHz ; -3 dB (-2 dBm Full Power Input)

2193A–BDC–04/03

ADC Step Response

Test pulse input characteristics: 20% to 80% input full scale and rise time ~ 200 ps.

Note: This step response was obtained with the TSEV8308500 chip on-board (device in die form).
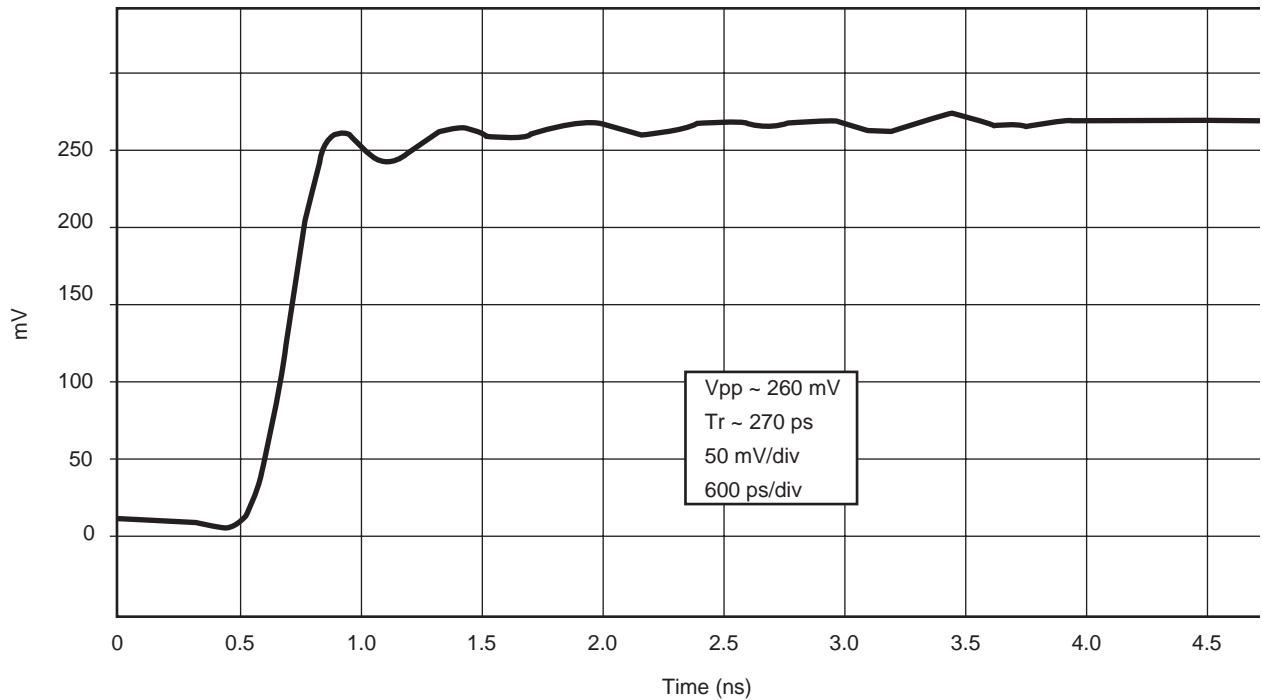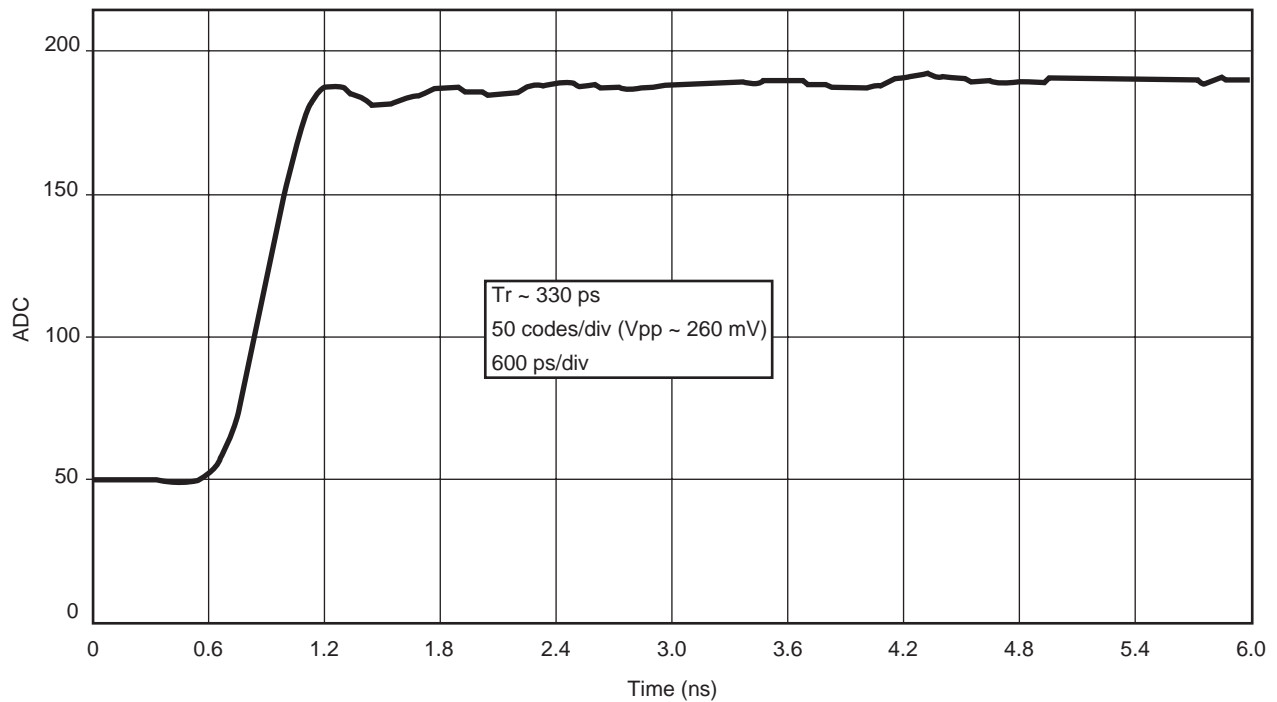
Figure 26. Test Pulse Digitized with 20 GHz DSO

Vpp ~ 260 mV
Tr ~ 270 ps
50 mV/div
600 ps/div

Figure 27. Same Test Pulse Digitized with TS8308500 ADC

Tr ~ 330 ps
50 codes/div (Vpp ~ 260 mV)
600 ps/div

Note: Ripples are due to the test setup (they are present on both measurements).

Timing Information

Timing Value for TS8308500

Timing values as defined in Table 3 on page 4 are advanced data, issuing from electric simulations and are the first characterization results fitted with measurements.

Timing values are given for CBGA68 package inputs/outputs, taking into account package internal controlled impedance traces propagation delays, and specified termination loads.

Propagation delays in 50/75Ω impedance traces are NOT taken into account for TOD and TDR.

Apply proper derating values corresponding to termination topology.

The min/max timing values are valid over the full temperature range in the following conditions:

–   Specified termination load (differential output Data and Data Ready):
    50Ω resistor in parallel with 1 standard ECLinPS register from Motorola, (i.e.:
    10E452). (Typical ECLinPS inputs shows a typical input capacitance of 1.5 pF
    (including package and ESD protections). If addressing an output Dmux, take care
    if some Digital outputs do not have the same termination load and apply
    corresponding derating value given below

–   Output Termination Load derating values for TOD and TDR:
    ~ 35 ps/pF or 50 ps per additional ECLinPS load

–   Propagation time delay derating values have also to be applied for TOD and TDR:
    ~ 6 ps/mm (155 ps/inch) for TSEV8308500 Evaluation Board
    Apply proper time delay derating value if a different dielectric layer is used.

Propagation Time Considerations

TOD and TDR timing values are given from pin to pin and DO NOT include the additional propagation times between device pins and input/output termination loads. For the TSEV8308500 Evaluation Board, the propagation time delay is 6 ps/mm (155 ps/inch) corresponding to 3.4 (at 10 GHz) dielectric constant of the RO4003 used for the Board.

If a different dielectric layer is used (for instance Teflon), use appropriate propagation time values.

TD does NOT depend on propagation times because it is a differential data.

(TD is the time difference between Data Ready output delay and digital Data output delay)

TD is also the most straightforward data to measure, again because it is differential: TD can be measured directly onto termination loads, with matched oscilloscopes probes.

TOD-TDR Variation Over Temperature

Values for TOD and TDR track each other over temperature (1% variation for TOD-TDR per 100°C temperature variation).

Therefore TOD-TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TODs and TDR affect can be considered as negligible.

Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values.

In other words:

– If TOD is at 1150 ps, TDR will not be at 1620 ps (maximum time delay for TDR).
– If TOD is at 1660 ps, TDR will not be at 1110 ps (minimum time delay for TDR). However, external TOD-TDR values may be dictated by total digital data skews between every TODs (each digital data) and TDR: MCM board , bonding wires and output lines lengths differences, and output termination impedance mismatches.

The external (on board) skew effect has NOT been taken into account for the specification of the minimum and maximum values for TOD-TDR.

Principle of Operation   The Analog input is sampled on the rising edge of the external clock input (CLK, CLKB) after TA (aperture delay) of typically 250 ps .

The digitized data is available after 4 clock periods latency (pipeline delay (TPD), on clock rising edge, after 1360 ps typical propagation delay TOD.)

The Data Ready differential output signal frequency (DR, DRB) is half the external clock frequency, that is it switches at the same rate as the digital outputs.

The Data Ready output signal (DR, DRB) switches on the external clock falling edge after a propagation delay TDR of typically 1320 ps.

A Master Asynchronous Reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR, DRB).

This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Actually, without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

Principle of Data Ready Signal Control by DRRB Input Command

Data Ready Output Signal Reset   The Data Ready signal is reset on the falling edge of the DRRB input command, on the ECL logical low level (-1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal Master Reset. So long as DRRB remains at a logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data Ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typical.

TRDR is measured between the -1.3V point of the falling edge of the DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.

Data Ready Output Signal Restart

The Data Ready output signal restarts on the DRRB command's rising edge, ECL logical high levels (-0.8V). DRRB may also be grounded, or is allowed to float, for a normal free running Data Ready output signal.

The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at DRRB rising edge instant:

- The DRRB rising edge occurs when the external encoding clock input (CLK,CLKB) is LOW: The Data Ready output's first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 1320 ps already defined hereabove.

- The DRRB rising edge occurs when external encoding clock input (CLK,CLKB) is HIGH: The Data Ready output's first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 1320 ps.

Consequently, as the analog input is sampled on the clock's rising edge, the first digitized data corresponding to the first acquisition (N) after a Data Ready signal restart (rising edge) is always strobed by the third rising edge of the Data Ready signal.

The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR,DRB) (zero crossing point).

Note: 1. For normal initialization of the Data Ready output signal, the external encoding clock signal frequency and level must be controlled. The minimum encoding clock sampling rate for the ADC is 10 Msps and consequently the clock cannot be stopped.

2. One single pin is used for both the DRRB input command and die junction temperature monitoring. Pin denomination will be DRRB/DIOD. (On former versions the denomination was DIOD.). Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

Analog Inputs (V_{IN}, V_{INB})

The analog input Full Scale range is 0.5V, or -2 dBm into the 50Ω termination resistor.

In differential mode input configuration, that means 0.25V on each input, or ±125 mV around 0V. The input common mode is ground.

The typical input capacitance is 3 pF for TS8308500 in a CBGA package.

Differential Input Voltage Span

Figure 28. Differential Input Voltage Span

(VIN, VINB) = ±250 mV = 500 mV diff
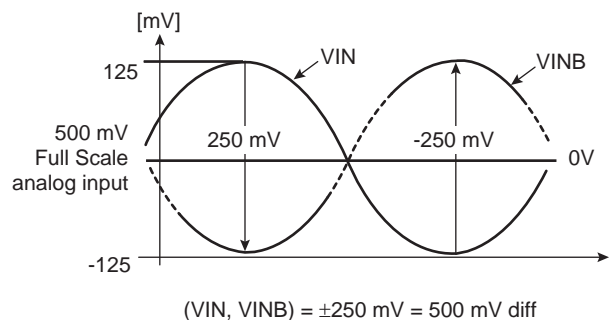
Differential Versus Single-ended Analog Input Operation

The TS8308500 can operate at full speed in either the differential or single-ended configuration.

This is explained by the fact the ADC uses a high input impedance differential preamplifier stage, (preceeding the sample and hold stage), which has been designed in order to be entered either in differential mode or single-ended mode.

This is true so long as the out-of-phase analog input pin V_{INB} is 50Ω terminated very closely to one of the neighboring shield ground pins (52, 53, 58, 59) which constitute the local ground reference for the in-phase analog input pin (V_{IN}).

Thus the differential analog input preamplifier will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

In a typical single-ended configuration, enter on the (V_{IN}) input pin, with the inverted phase input pin (V_{INB}) grounded through the 50Ω termination resistor.

In a single-ended input configuration, the in-phase input amplitude is 0.5V, centered on 0V (or -2 dBm into 50Ω). The inverted phase input is at ground potential through the 50Ω termination resistor.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

Typical Single-ended Analog Input Configuration

Figure 29. Typical Single-ended Analog Input Configuration

VIN = ±250 mV = 500 mV diff

50Ω reverse termination
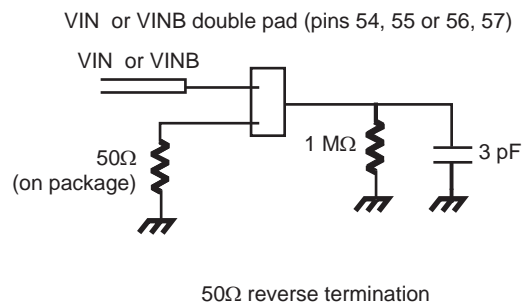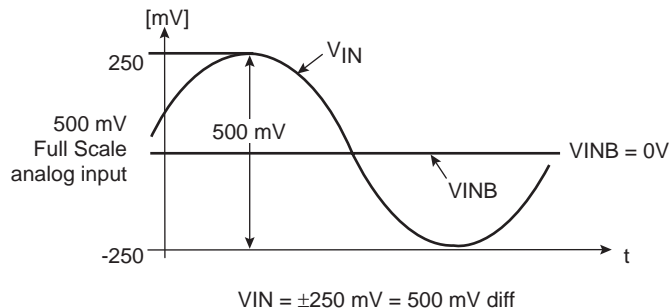
Clock Inputs (CLK, CLKB)

The TS8308500 can be clocked at full speed without noticeable performance degradation in either the differential or single-ended configuration.

This is explained by the fact the ADC uses a differential preamplifier stage for the clock buffer, which has been designed in order to be entered either in differential or single-ended mode.

The recommended sinewave generator characteristics are typically -120 dBc/Hz phase noise floor spectral density, at 1 kHz from carrier, assuming a single tone 4 dBm input for the clock signal.

Single-ended Clock Input (Ground Common Mode)

Although the clock inputs were intended to be driven differentially with nominal -0.8V/-1.8V ECL levels, the TS8308500 clock buffer can manage a single-ended sinewave clock signal centered around 0V. This is the most convenient clock input configuration as it does not require the use of a power splitter.

No performance degradation (i.e.: due to timing jitter) is observed in this particular single-ended configuration up to 500 Msps Nyquist Conditions (F_{IN} = 250 MHz).

This is all the more so since the inverted phase clock input pin is 50Ω terminated on the package (that is very close to one of the neighboring shield ground pins, which constitutes the local ground reference for the inphase clock input).

Thus the TS8308500 differential clock input buffer will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects. Moreover, a very low phase noise sinewave generator must be used for enhanced jitter performance.

The typical in-phase clock input amplitude is 1V, centered on 0V (ground) common mode. This corresponds to a typical clock input power level of 4 dBm into the 50Ω termination resistor. Do not exceed 10 dBm to avoid saturation of the preamplifier input transistors.

Figure 30. Single-ended Clock Input (Ground Common Mode):
VCLK common mode = 0V; VCLKB = 0V; 4 dBm typical clock input power level (into 50Ω termination resistor)
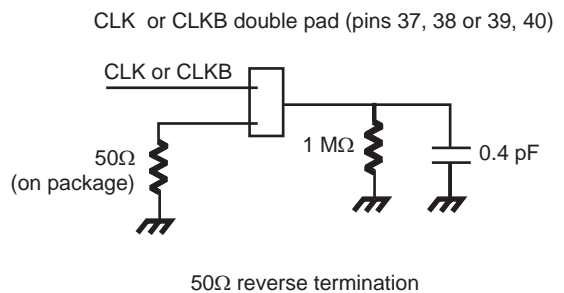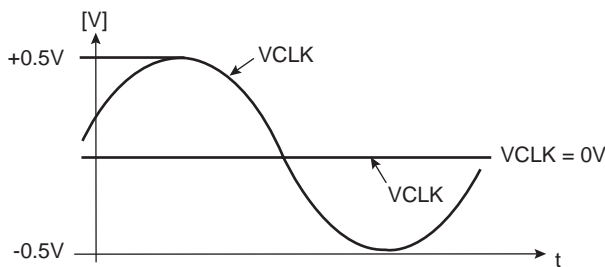
Note: Do not exceed 10 dBm into the 50Ω termination resistor for the single clock input power level.

Differential ECL Clock Input

The clock inputs can be driven differentially with nominal -0.8V/-1.8V ECL levels.

In this mode, a low-phase noise sinewave generator can be used to drive the clock inputs, followed by a power splitter (hybrid junction) in order to obtain 180° out of phase sinewave signals. Biasing tees can be used for offseting the common mode voltage to ECL levels.

Note: As the biasing tees propagation times are not matching, a tunable delay line is required in order to ensure the signals are 180° out of phase, especially at fast clock rates in the 500 Msps range.

Figure 31. Differential Clock Inputs (ECL Levels)
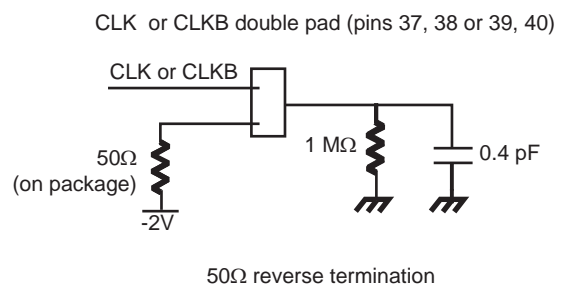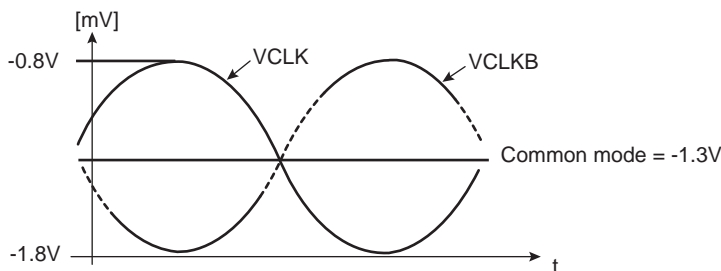
Single-ended ECL Clock Input

In a single-ended configuration, enter at CLK (resp. CLKB) pin, with the inverted phase clock input pin CLKB (respectively CLK) connected to -1.3V through the 50Ω termination resistor.

The in-phase input amplitude is 1V, centered on -1.3V common mode.

Figure 32. Single-ended Clock Input (ECL):
VCLK common mode = -1.3V; VCLKB = -1.3V
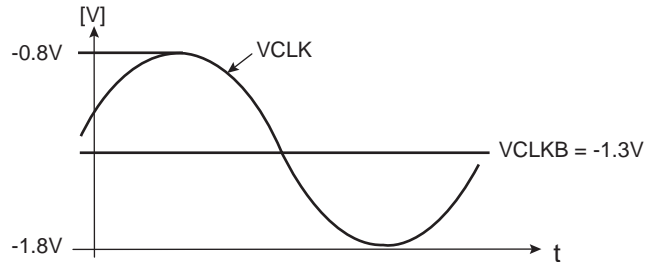
Noise Immunity Information

Circuit noise immunity performance begins at design level.

Efforts have been made to the design to make it as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry. (Cascode stage isolation, internal damping resistors, clamps, internal (on-chip) decoupling capacitors.)

Furthermore, the fully differential operation from the analog input up to the digital outputs provides enhanced noise immunity with common mode noise rejection.

Common mode noise voltage induced on the differential analog and clock inputs will be canceled out by these balanced differential amplifiers.

Moreover, proper active signal shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs.

The analog inputs and clock inputs of the TS8308500 device have been surrounded by ground pins, which must be directly connected to the external ground plane.

Digital Outputs

The TS8308500 differential output buffers are internally loaded with 75Ω. The 75Ω resistors are connected to the digital ground pins through a -0.8V level shift diode (see Figure 33, Figure 34, Figure 35 on page 29).

The TS8308500 output buffers are designed for driving 75Ω (default) or 50Ω properly terminated impedance lines or coaxial cables. An 11 mA bias current flowing alternately into one of the 75Ω resistors when switching ensures a 0.825V voltage drop across the resistor (unterminated outputs).

The V_{PLUSD} positive supply voltage allows the adjustment of the output common mode level from -1.2V (V_{PLUSD} = 0V for ECL output compatibility) to +1.2V (V_{PLUSD} = 2.4V for LVDS output compatibility).

Therefore, the single-ended output voltages vary approximately between -0.8V and -1.625V, (outputs unterminated), around -1.2V common mode voltage.

Three possible line driving and back-termination scenarios are proposed (assuming $V_{PLUSD} = 0V$):

1. 75Ω impedance transmission lines, 75Ω differentially terminated (Figure 33):

   Each output voltage varies between -1V and -1.42V (respectively +1.4V and +1V), leading to ±0.41V = 0.825V in differential, around -1.21V (respectively +1.21V) common mode for $V_{PLUSD} = 0V$ (respectively 2.4V)

2. 50Ω impedance transmission lines, 50Ω differentially terminated (Figure 34):

   Each output voltage varies between -1.02V and -1.35V (respectively +1.38V and +1.05V), leading to ±0.33V = 660 mV in differential, around -1.18V (respectively +1.21V) common mode for $V_{PLUSD} = 0V$ (respectively 2.4V)

3. 75Ω impedance open transmission lines (Figure 35):

   Each output voltage varies between -1.6V and -0.8V (respectively +0.8V and +1.6V), which are true ECL levels, leading to ±0.8V = 1.6V in differential, around -1.2V (respectively +1.2V) common mode for $V_{PLUSD} = 0V$ (respectively 2.4V)

   Therefore, it is possible to directly drive high input impedance storing registers, without terminating the 75Ω transmission lines.

   In the time domain, that means that the incident wave will reflect at the 75Ω transmission line output and travel back to the generator (i.e.: the 75Ω data output buffer). As the buffer output impedance is 75Ω, no back reflection will occur.

Note: This is no longer true if a 50Ω transmission line is used, as the latter is not matching the buffer 75Ω output impedance.

Each differential output termination length must be kept identical.

It is recommended to decouple the midpoint of the differential termination with a 10 nF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

Too large mismatches (keep < a few mm) in the differential line lengths will lead to switching currents flowing into the decoupling capacitor leading to switching ground noise.

The differential output voltage levels (75Ω or 50Ω termination) are not ECL standard voltage levels, however, it is possible to drive standard logic ECL circuitry like the ECLinPS logic line from Motorola®.

Differential Output Loading Configurations (Levels for ECL Compatibility)

Figure 33. Differential Output: 75Ω Terminated
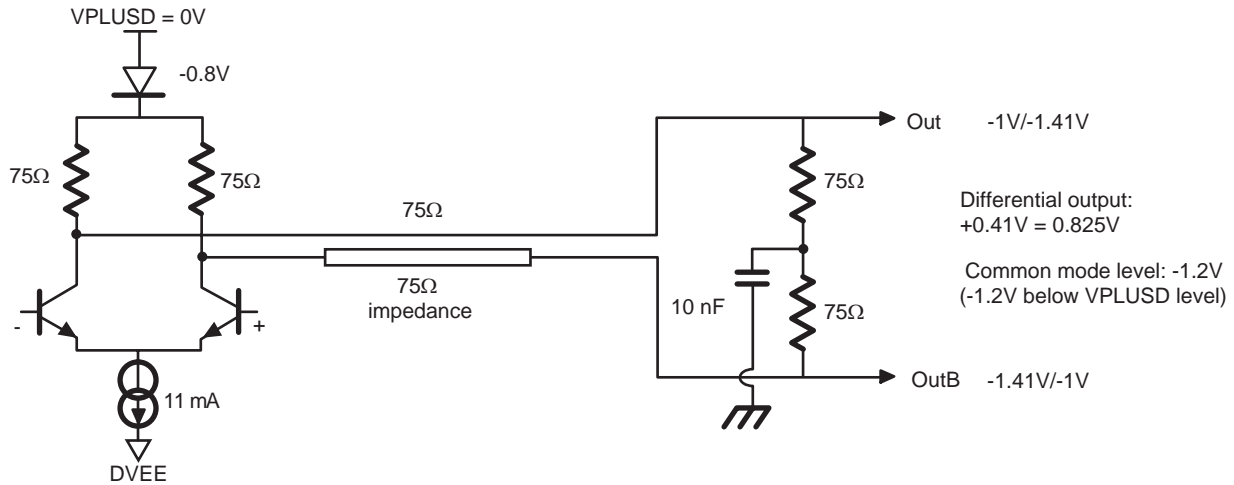

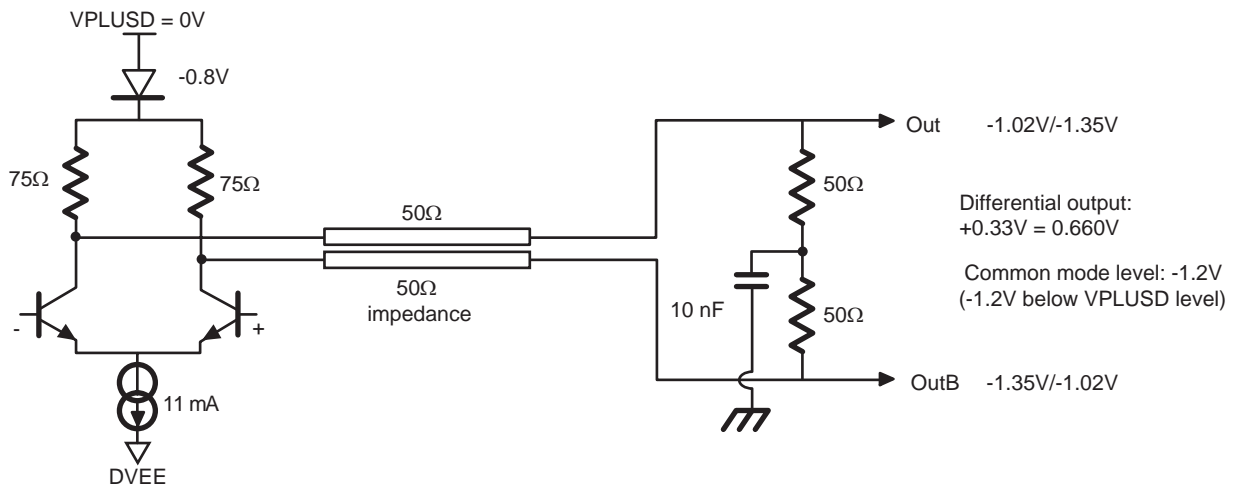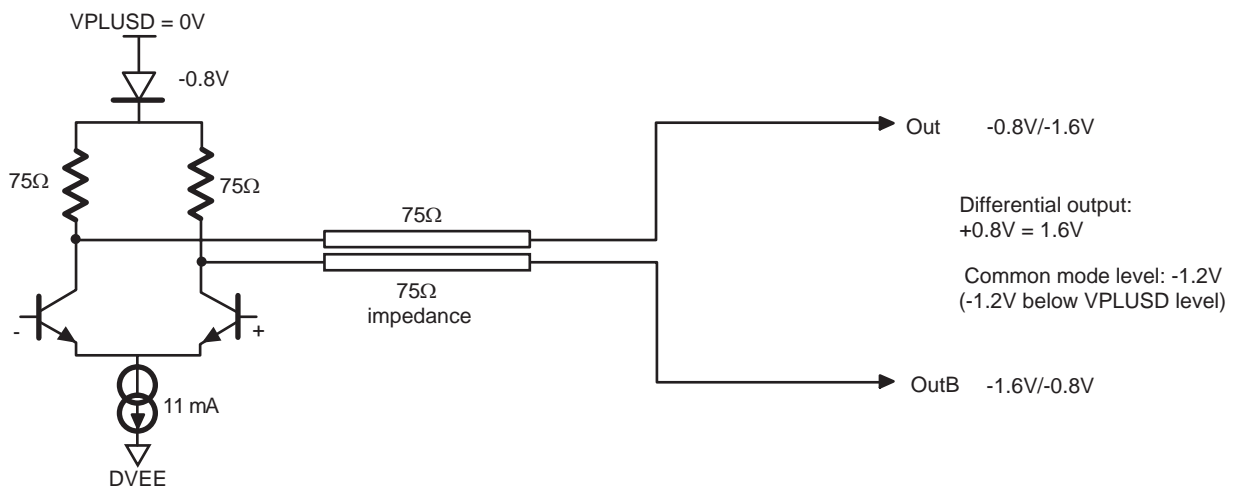**Figure 34.** Differential Output: 50Ω Terminated

Figure 35. Differential Output: Open Loaded

Differential Output Loading Configurations (Levels for LVDS Compatibility)

Figure 36. Differential Output: 75Ω Terminated

VPLUSD = 2.4V

1.6V

75Ω   75Ω

75Ω

75Ω impedance

-    +

11 mA

DVEE

Out   1.4V/0.99V

75Ω

10 nF   75Ω

Differential output:
+0.41V = 0.825V

Common mode level: -1.2V
(-1.2V below VPLUSD level)

OutB   0.99V/1.4V
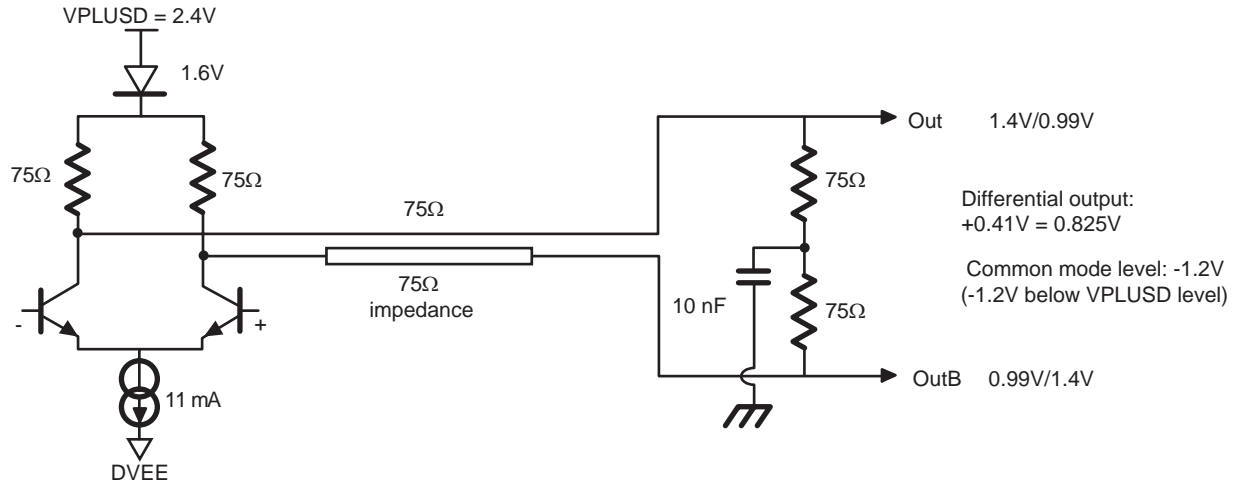
Figure 37. Differential Output: 50Ω Terminated

VPLUSD = 2.4V

1.6V

75Ω   75Ω

50Ω

50Ω impedance

-    +

11 mA

DVEE

Out   1.38V/1.05V

50Ω

10 nF   50Ω

Differential output:
+0.33V = 0.660V

Common mode level: -1.2V
(-1.2V below VPLUSD level)

OutB   1.05V/1.38V
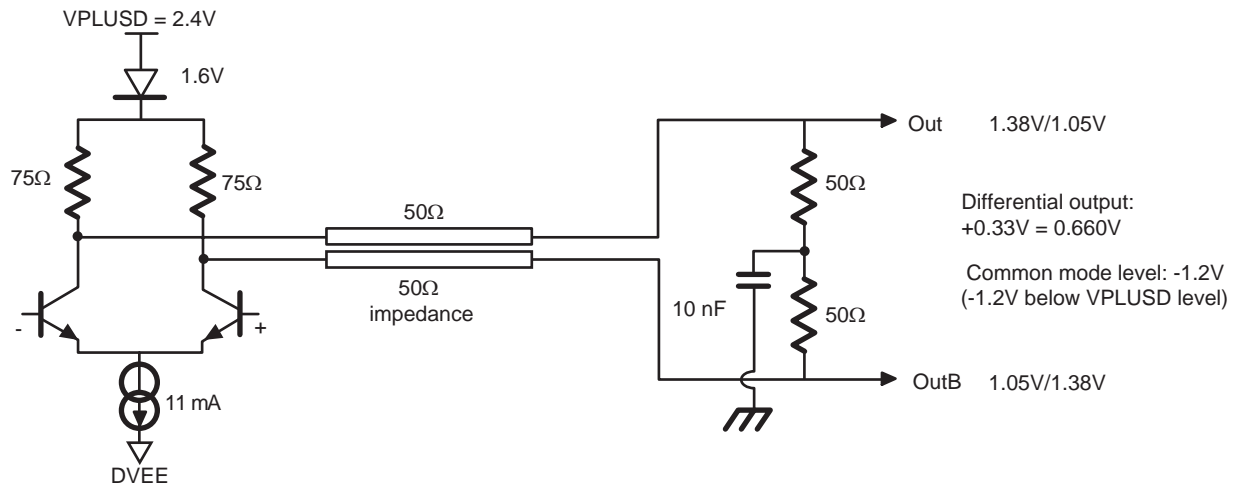
Figure 38. Differential Output: Open Loaded

VPLUSD = 2.4V

1.6V

75Ω   75Ω

75Ω

75Ω impedance

-    +

11 mA

DVEE

Out   1.6V/0.8V

Differential output:
+0.8V = 1.6V

Common mode level: -1.2V
(-1.2V below VPLUSD level)

OutB   0.8V/1.6V
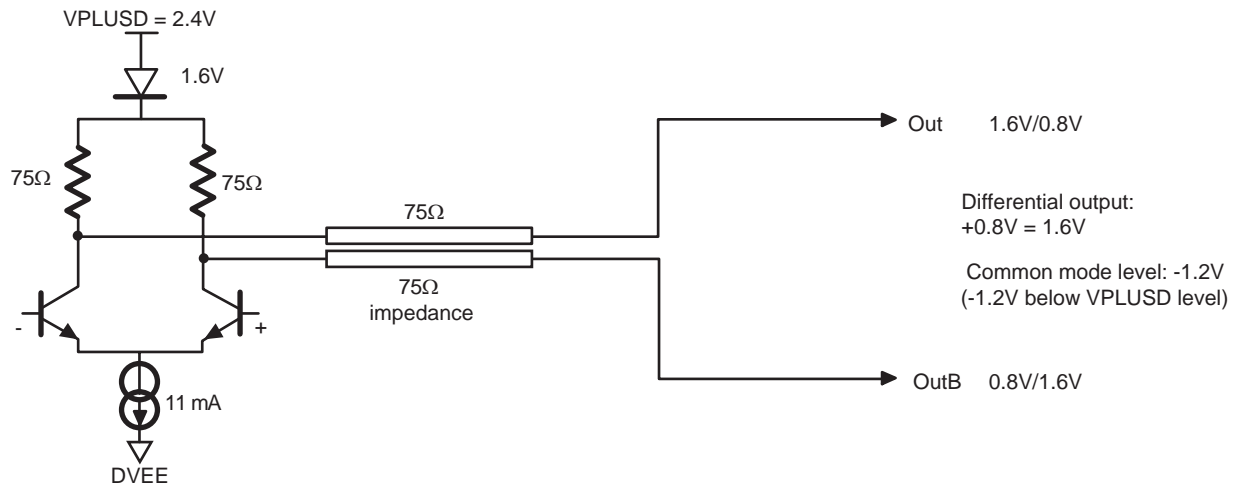
Out of Range Bit

An Out of Range (OR, ORB) bit that goes to logical high state when the input exceeds the positive full scale or falls below the negative full scale is available.

When the analog input exceeds the positive full-scale, the digital output datas remain at a high logical state, with (OR, ORB) at logical one.

When the analog input falls below the negative full-scale, the digital outputs remain at a logical low state, with (OR, ORB) at logical one again.

Gray or Binary Output Data Format Select

The TS8308500 internal regeneration latches indecisions (for inputs very close to a latch threshold) that can produce errors in the logic encoding circuitry and lead to large amplitude output errors.

This is due to the fact that the latches are regenerating the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time (t):

$Av = \exp(\Delta(t)/\tau)$, where τ is the positive feedback regeneration time constant.

The TS8308500 has been designed to reduce the probability of occurrence of such errors to approximately 10^{-13} (targeted for the TS8308500 at 500 Msps).

A standard technique for reducing the amplitude of such errors down to ±1 LSB consists in outputing the digital data in Gray code format. Though the TS8308500 has been designed to feature a bit error rate of 10^{-13} with a binary output format, it is possible for the user to select between the Binary or Gray output data format, in order to reduce the amplitude of such errors when they occur, by storing Gray output codes.

Digital Data format selection:
- BINARY output format if GORB is floating or V_{CC}.
- GRAY output format if GORB is connected to ground (0V).

Diode Pin K1

A single pin is used for both the DRRB input command and die junction monitoring. The pin denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

(See "Principle of Data Ready Signal Control by DRRB Input Command" on page 23 for Data Ready Reset input command).

The operating die junction temperature must be kept below 145°C, therefore an adequate cooling system has to be set up. The diode mounted transistor measured Vbe value versus junction temperature is given below.

Figure 39. Diode Pin K1
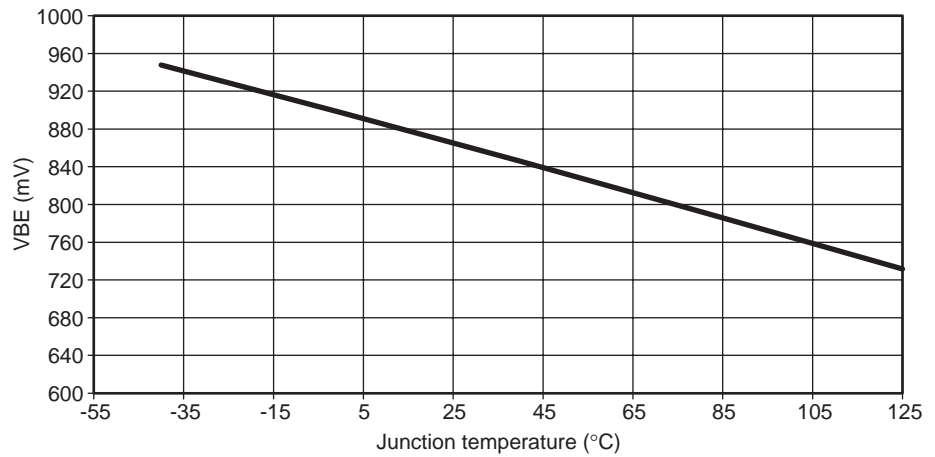
ADC Gain Control Pin K6

The ADC gain is adjustable by means of the pin K6 (input impedance is 1 MΩ in parallel with 2 pF).

The gain adjust transfer function is given below:

Figure 40. ADC Gain Control Pin K6
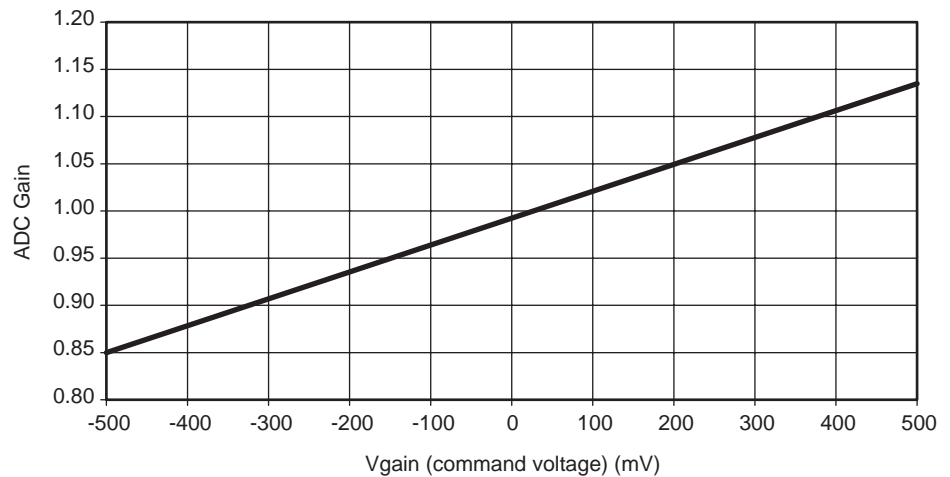
Equivalent Input/Output Schematics

Figure 41. Equivalent Analog Input Circuit and ESD Protections

Note: The ESD protection equivalent capacitance is 150 fF.

Figure 42. Equivalent Analog Clock Input Circuit and ESD Protections
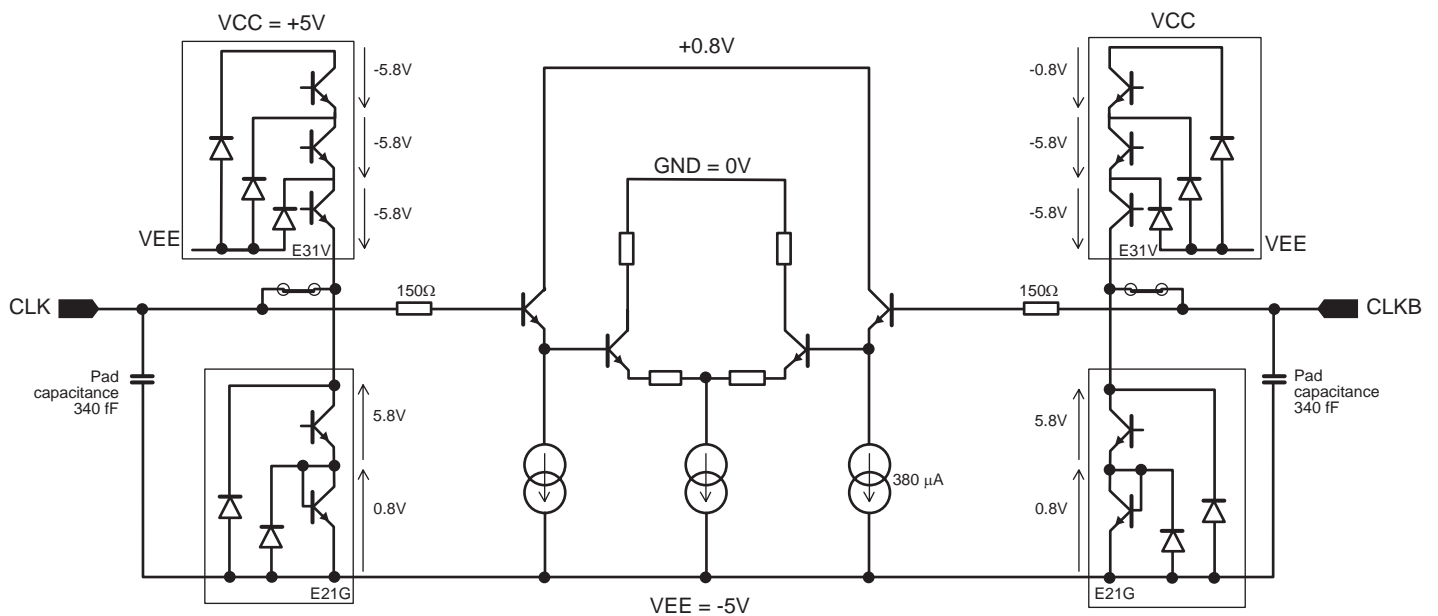
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 43. Equivalent Data Output Buffer Circuit and ESD Protections

VPLUSD = 0V to 2.4V

-5.8V

VEE

E01V

OUT

Pad
capacitance
180 fF

5.8V

0.8V

0.8V

VEE = -5V

-5.8V

E01V

VEE

OUTB

Pad
capacitance
180 fF

5.8V

0.8V

0.8V

VEE = -5V

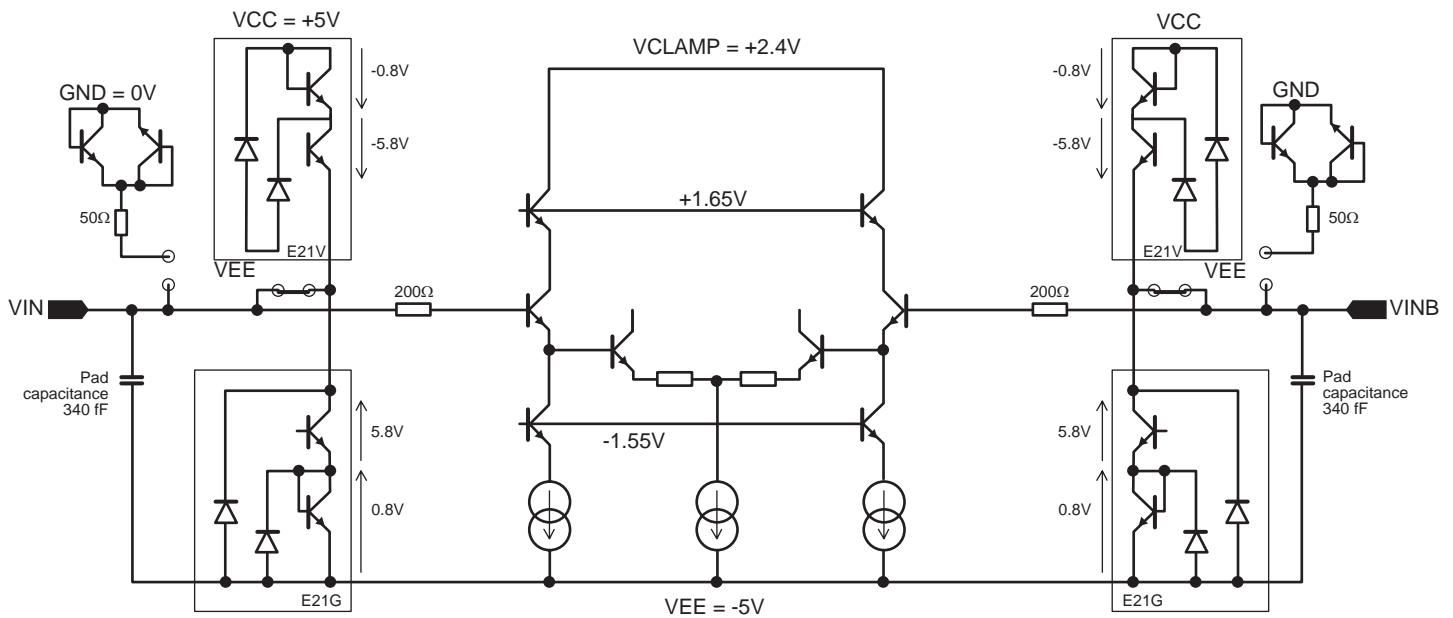DVEE = -5V
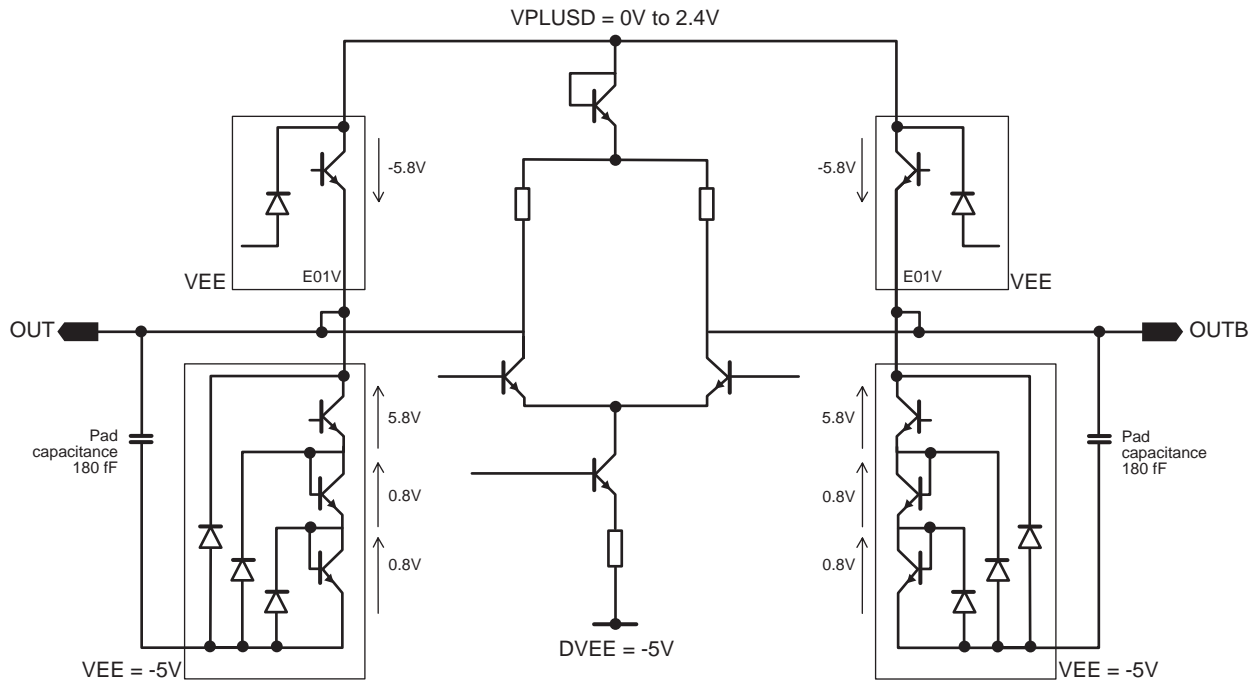
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 44. ADC Gain Adjust Equivalent Input Circuits and ESD Protections

VCC = +5V

-0.8V

-5.8V

NP1032C2

E22V

GA

Pad
capacitance
180 fF

0.8V

0.8V

5.8V

VEE

E22GA

1 kΩ

2 pF

GND

+0.8V

GND

500 µA

500 µA

VEE = -5V
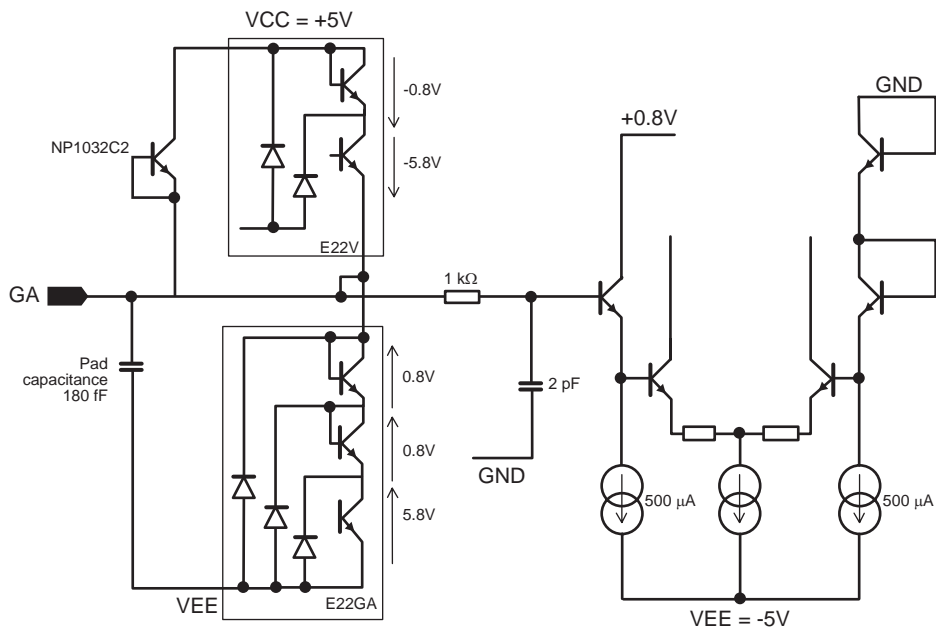
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 45. GORB Equivalent Input Schematic and ESD Protections
GORB: gray or binary select input; floating or tied to V_{CC} -> binary
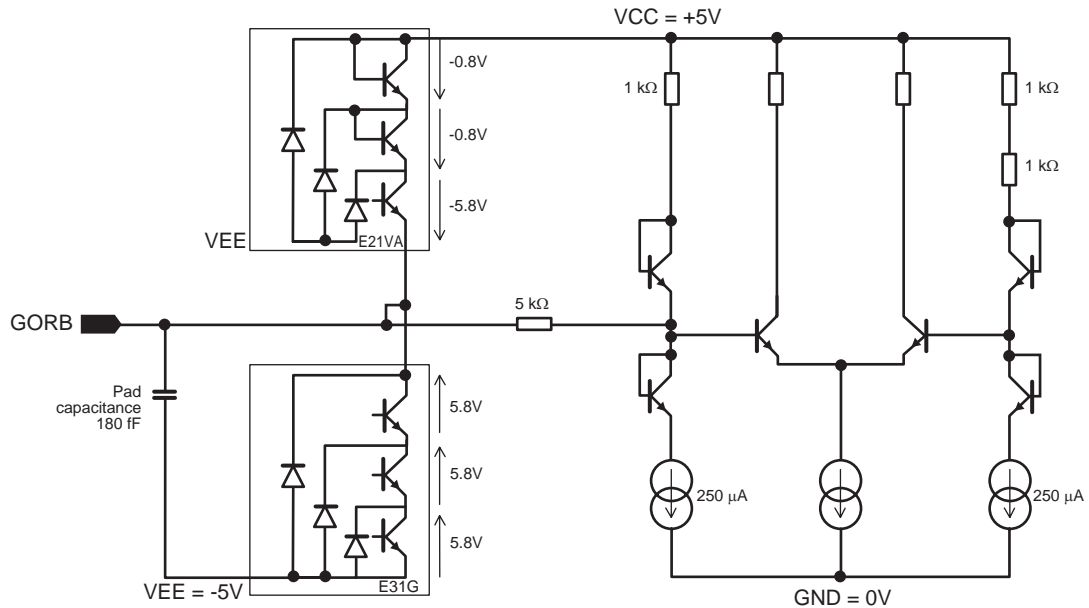
Note: The ESD protection equivalent capacitance is 150 fF.
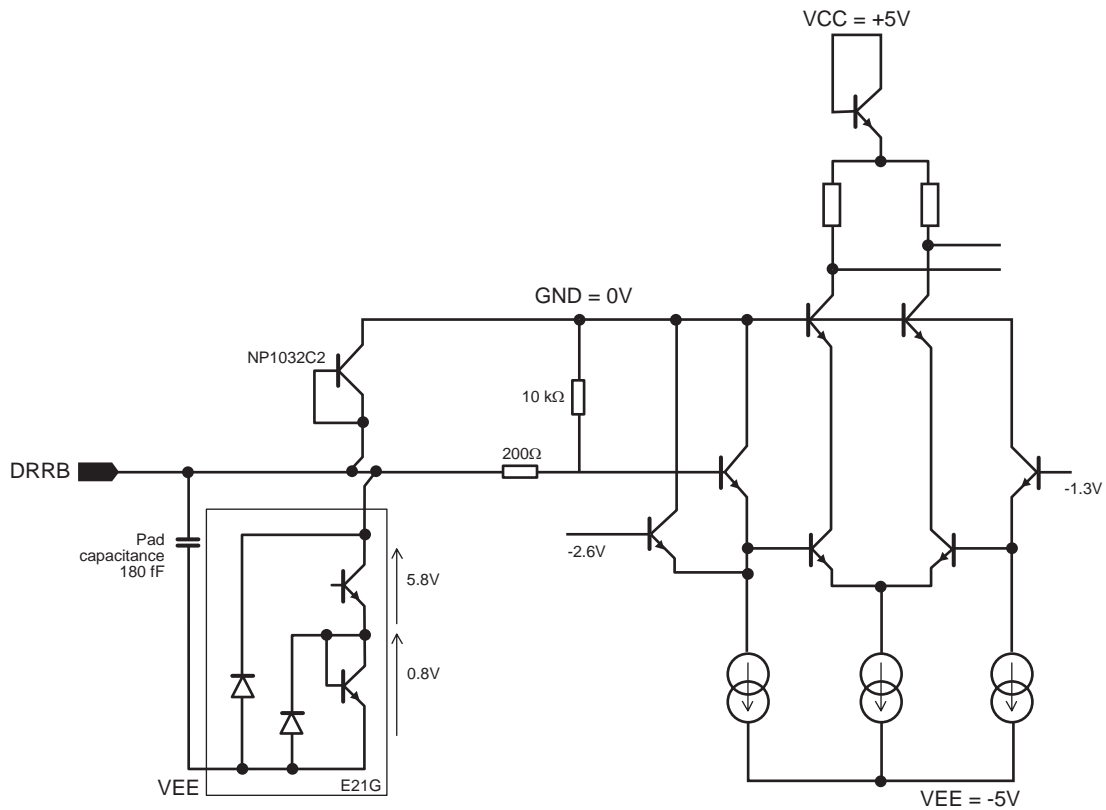
Figure 46. DRRB Equivalent Input Schematic and ESD Protections
Actual protection range: 6.6V above V_{EE}, in fact stress above GND are clipped by the CB diode used for Tj monitoring

Note: The ESD protection equivalent capacitance is 150 fF.

TSEV8308500:
Device Evaluation Board

For complete specification, see the separate "TSEV8308500" document.

General Description

The TSEV8308500 Evaluation Board (EB) is a board which has been designed in order to facilitate the evaluation and the characterization of the TS8308500 device up to its 1.3 GHz full power bandwidth at up to 500 Msps in the commercial temperature range.

The high speed of the TS8308500 requires careful attention to circuit design and layout to achieve optimal performance.

This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8308500 ADC performances over the temperature range.

The TSEV8308500 Evaluation Board is very straightforward as it only implements the TS8308500 ADC, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with HP16500C high frequency probes.

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines, and a die junction temperature measurement setting.

The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TS8308500 and its heatsink installed.

Package Description

Table 7. TS8308500 Pad Description

Pad number	Chip Pad Name	Chip Pad Function
1	V_{PLUSD}	Positive digital supply (double pad)[2]
2	D5	In-phase (+) digital output, bit 5 (D7 is the MSB; Bit 7, D0 is the LSB; Bit 0)
3	D5B	Inverted phase (-) digital output, bit 5
4	D4	In-phase (+) digital output, bit 4
5	D4B	Inverted phase (-) digital output, bit 4
6	DV_{EE}	-5V digital supply (double pad)
7	DR	In-phase (+) Data Ready
8	DRB	Inverted phase (-) Data Ready
9	D3	In-phase (+) digital output, bit 3
10	D3B	Inverted phase (-) digital output, bit 3
11	V_{PLUSD}	Positive digital supply (double pad)[2]
12	D2	In-phase (+) digital output, bit 2
13	D2B	Inverted phase (-) digital output, bit 2
14	D1	In-phase (+) digital output, bit 1
15	D1B	Inverted phase (-) digital output, bit 1
16	D0	In-phase (+) digital output, bit 0, Least Significant Bit
17	D0B	Inverted phase (-) digital output, bit 0, Least Significant Bit
18	GORG	Gray or Binary data output format select[1]
19	V_{CC}	+5V supply (double pad)
20	GND	Analog ground (double pad)
21	V_{CC}	+5V supply (double pad)
22	V_{EE}	-5V analog supply (double pad)
23	V_{CC}	+5V supply (double pad)
24	GND	Analog ground (double pad)
25	CLK	In-phase (+) clock input (double pad)
26	GND	Analog ground
27	CLKB	Inverted phase (-) clock input (double pad)
28	GND	Analog ground (double pad)
29	V_{EE}	-5V analog supply (double pad)
30	V_{CC}	+5V supply (double pad)
31	V_{EE}	-5V analog supply (double pad)
32	DIOD/DRRB	Diode input for Tj monitoring/Input for asynchronous Data Ready Reset
33	GND	Analog ground

Table 7. TS8308500 Pad Description (Continued)

Pad number	Chip Pad Name	Chip Pad Function
34	V_{IN}	In-phase (+) analog input (double pad)
35	GND	Analog ground
36	V_{IN}B	Inverted phase (-) analog input (double pad)
37	GND	Analog ground (double pad)
38	GAIN	ADC gain adjust input
39	V_{CC}	+5V supply (double pad)
40	V_{CC}	+5V supply
41	OR	In-phase (+) Out of Range digital output
42	ORB	Inverted phase (-) Out of Range digital output
43	D7	In-phase (+) digital output, bit 7, Most Significant Bit
44	D7B	Inverted phase (-) digital output bit 7
45	D6	In-phase (+) digital output, bit 6
46	D6B	Inverted phase (-) digital output, bit 6

Notes: 1. GORB tied to V_{CC} or floating: Binary output data format. GORB tied to GND: Gray output data format.
2. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is remmended to lower the positive digital supply level in the name proportion in order to spare power dissipation.
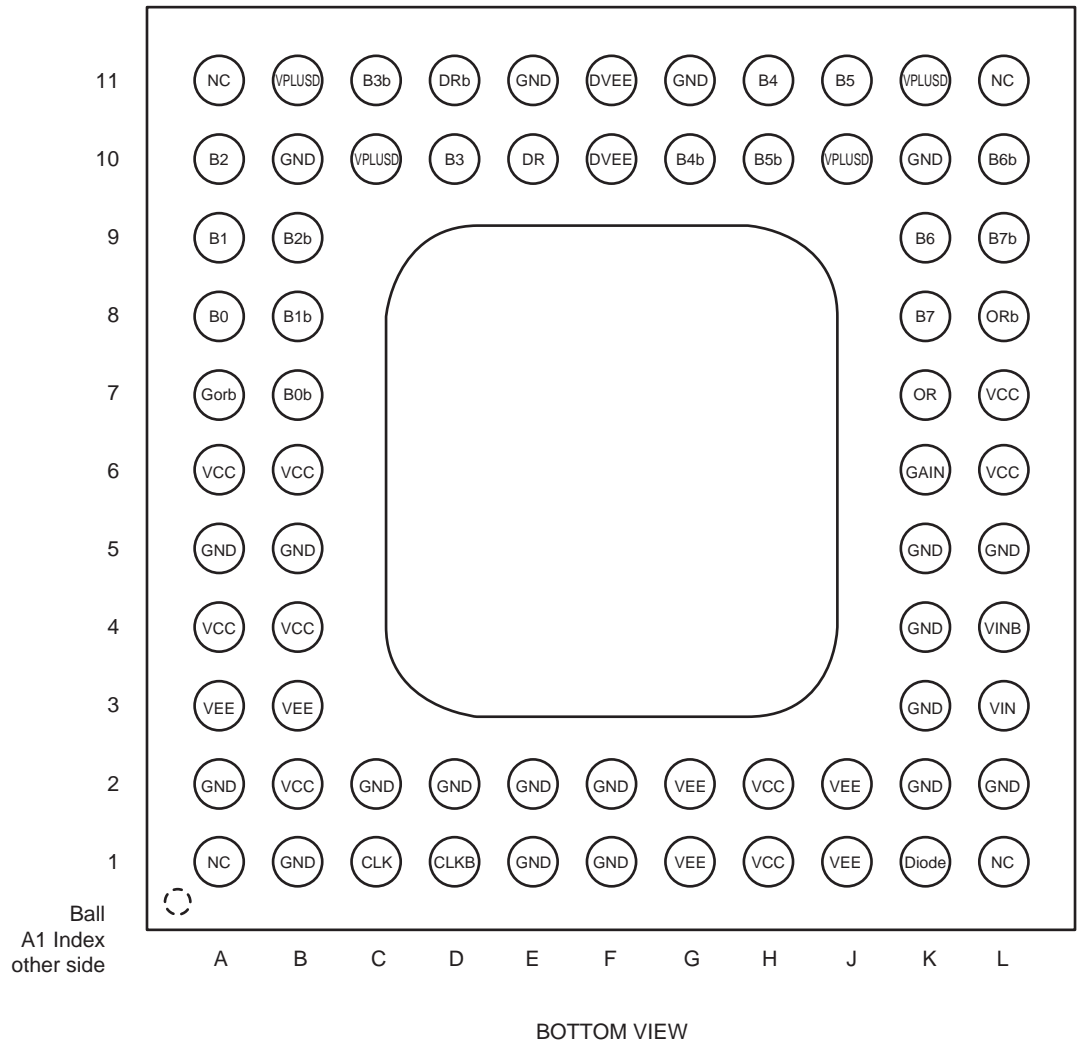
TS8308500
Pin Description
(CBGA68 package)

Table 8. TS8308500 Pin Description

Symbol	Pin number	Function
GND	A2, A5, B1, B5, B10, C2, D2, E1, E2, E11, F1, F2, G11, K2, K3, K4, K5, K10, L2, L5	Ground pins, to be connected to external ground plane
V_{CC}	A4, A6, B2, B4, B6, H1, H2, L6, L7	+5V positive supply
V_{EE}	A3, B3, G1, G2, J1, J2	5V analog negative supply
DV_{EE}	F10, F11	-5V digital negative supply
V_{IN}	L3	In-phase (+) analog input signal of the Sample and Hold differential preamplifier
V_{INB}	L4	Inverted phase (-) of ECL clock input signal (CLK)
CLK	C1	In-phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal
CLKB	D1	Inverted phase (-) of ECL clock input signal (CLK)
B0, B1, B2, B3, B4, B5, B6, B7	A8, A9, A10, D10, H11, J11, K9, K8	In-phase (+) digital outputs. B0 is the LSB, B7 is the MSB
B0B, B1B, B2B, B3B, B4B, B5B, B6B, B7B	B7, B8, B9, C11, G10, H10, L10, L9	Inverted phase (-) Digital outputs. B0B is the inverted LSB B7B is the inverted MSB
OR	K7	In-phase (+) Out of Range bit. Out of Range is high on the leading edge of code 0 and code 256
ORB	L8	Inverted phase (+) of Out of Range bit (OR)
DR	E10	In-phase (+) output of Data Ready signal
DRB	D11	Inverted phase (-) output of Data Ready signal (DR)
GORB	A7	Gray or Binary select output format control pin – Binary output format if GORB is floating or V_{CC} – Gray output format if GORB is connected at ground (0V)
GAIN	K6	ADC gain adjust pin. The gain pin is grounded by default, the ADC gain transfer fuction is nominally close to one
DIOD/DRRB	K1	Die function temperature measurement pin and asynchronous data ready reset active low, single ended ECL input
V_{PLUSD}	B11, C10, J10, K11	+ 2.4V for LVDS output levels otherwise to GND[1]
NC	A1, A11, L1, L11	Not connected

Note: 1. The common mode level of the output buffers is 1.2V below the positive digital supply
For ECL compatibility the positive digital supply must be set at 0V (ground)
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V
If the subsequent LVDS circuitry can withstand a lower level for the input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation

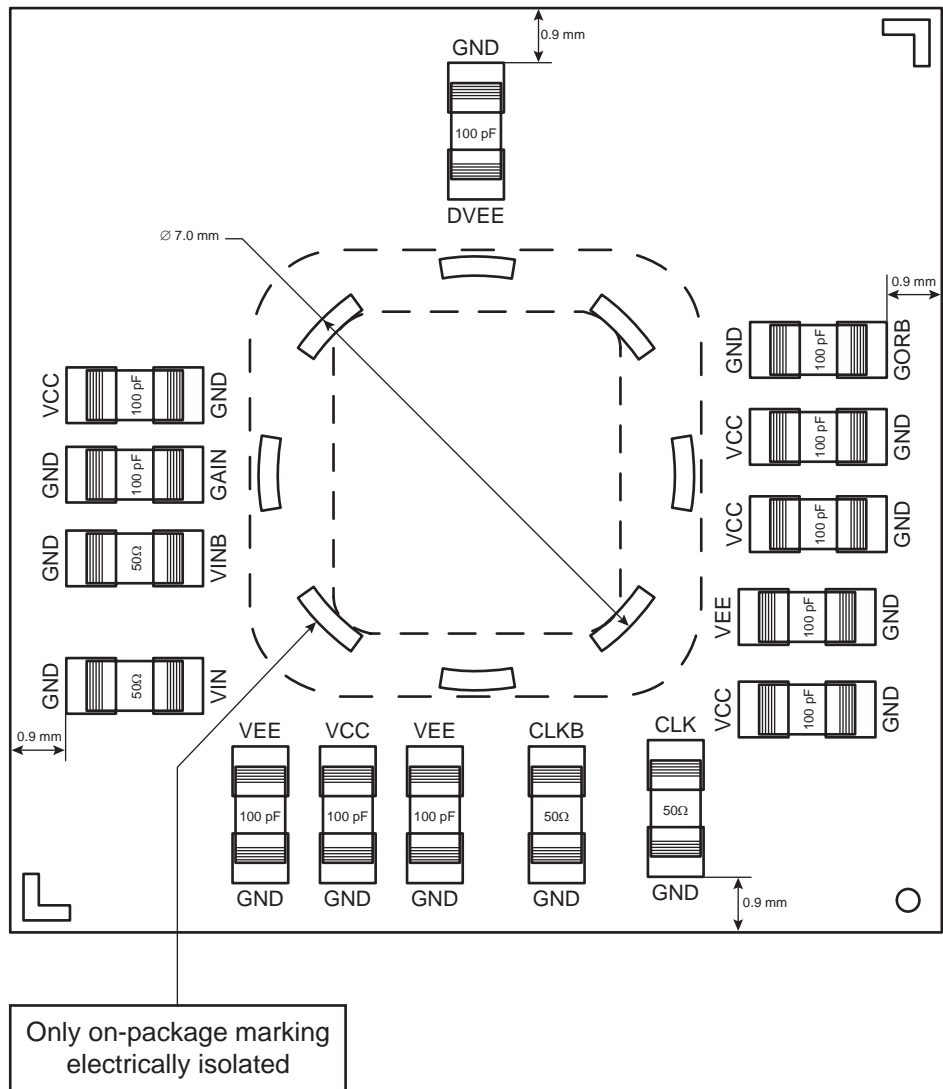**TS8308500GL
Pinout of CBGA68
Package**

Figure 47. TS8308500 Pinout of CBGA68 Package

BOTTOM VIEW

**TS8308500
Capacitors and
Resistors Implant**

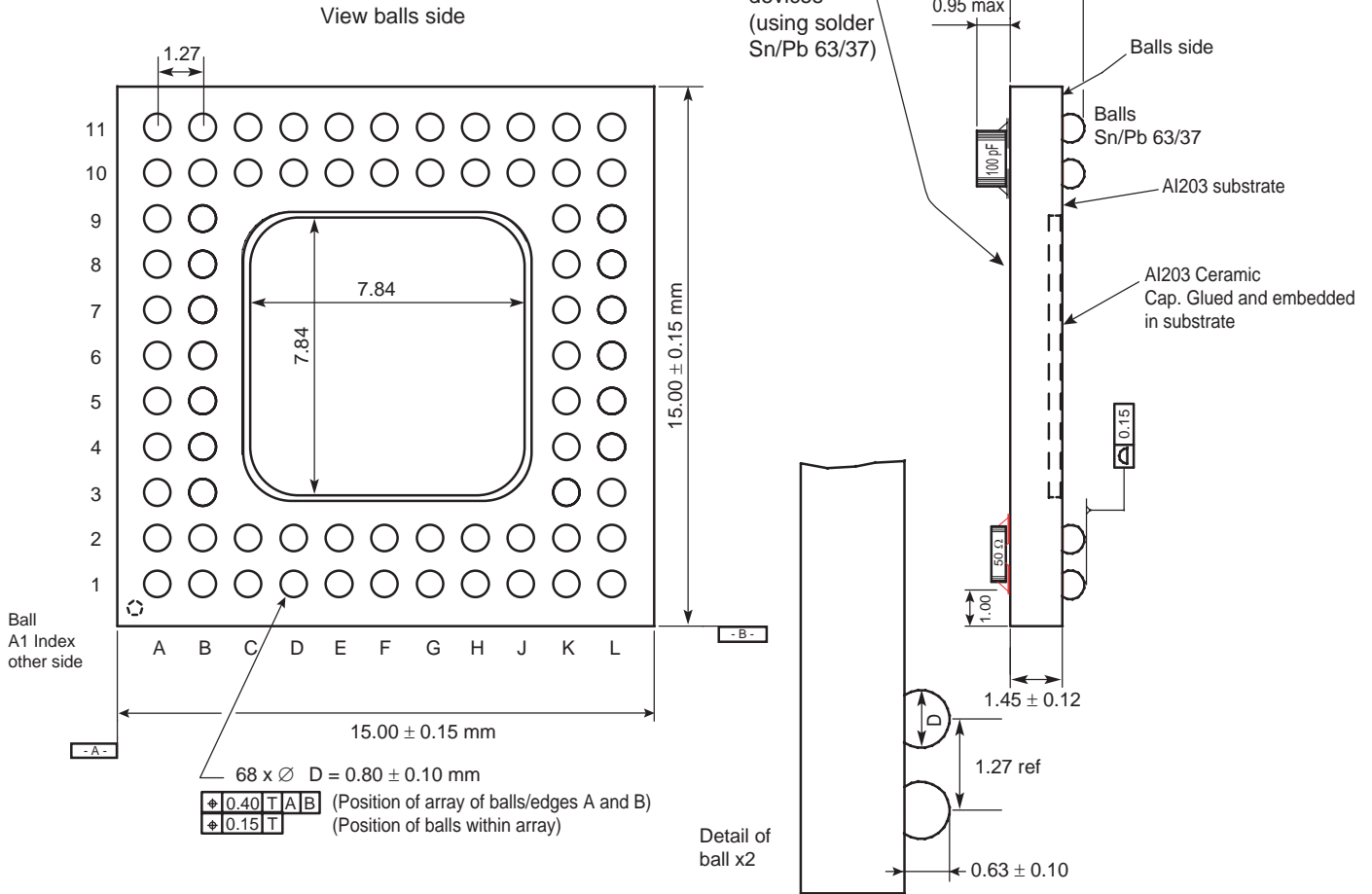**Figure 48.** TS8308500 Capacitors and Resistors Implant

Note: R and C discrete components are 0603 size (1.6 x 0.8mm)

Outline Dimensions

Figure 49. Outline Dimensions - 68 Pins CBGA

CBGA 68 package.
AL203 substrate.
Package design.
Corner balls (x4) are not connected (mechanical ball).
Balls : 1.27 mm pitch on 11x11 grid.

View balls side

1.27

11 10 9 8 7 6 5 4 3 2 1

7.84

7.84

15.00 ± 0.15 mm

15.00 ± 0.15 mm

Ball
A1 Index
other side

A B C D E F G H J K L

- A -

- B -

68 x ∅ D = 0.80 ± 0.10 mm

| ⊕ | 0.40 | T | A | B | (Position of array of balls/edges A and B)
| ⊕ | 0.15 | T | (Position of balls within array)

Top side with
soldered R, C
devices
(using solder
Sn/Pb 63/37)

0.95 max

- T -

0.20

Balls side

Balls
Sn/Pb 63/37

100 pF

Al203 substrate

Al203 Ceramic
Cap. Glued and embedded
in substrate

0.15

50 Ω

1.00

1.45 ± 0.12

1.27 ref

D

Detail of
ball x2

0.63 ± 0.10

All units in mm

Cross Section   **Figure 50.** Cross Section

T
0.20 T

- T -

Top side with soldered R, C devices
(using solder Sn/Pb 63/37)

0.95 max

Balls side

Balls
Sn/Pb 63/37

100 pF

AI203 substrate

AI203 Ceramic Cap.
Glued on substrate

(0.400)

0.15

50 Ω

(0.20)

(2 x 0.20)

(0.25)

(0.20)

1.45 ± 0.12

All units in mm
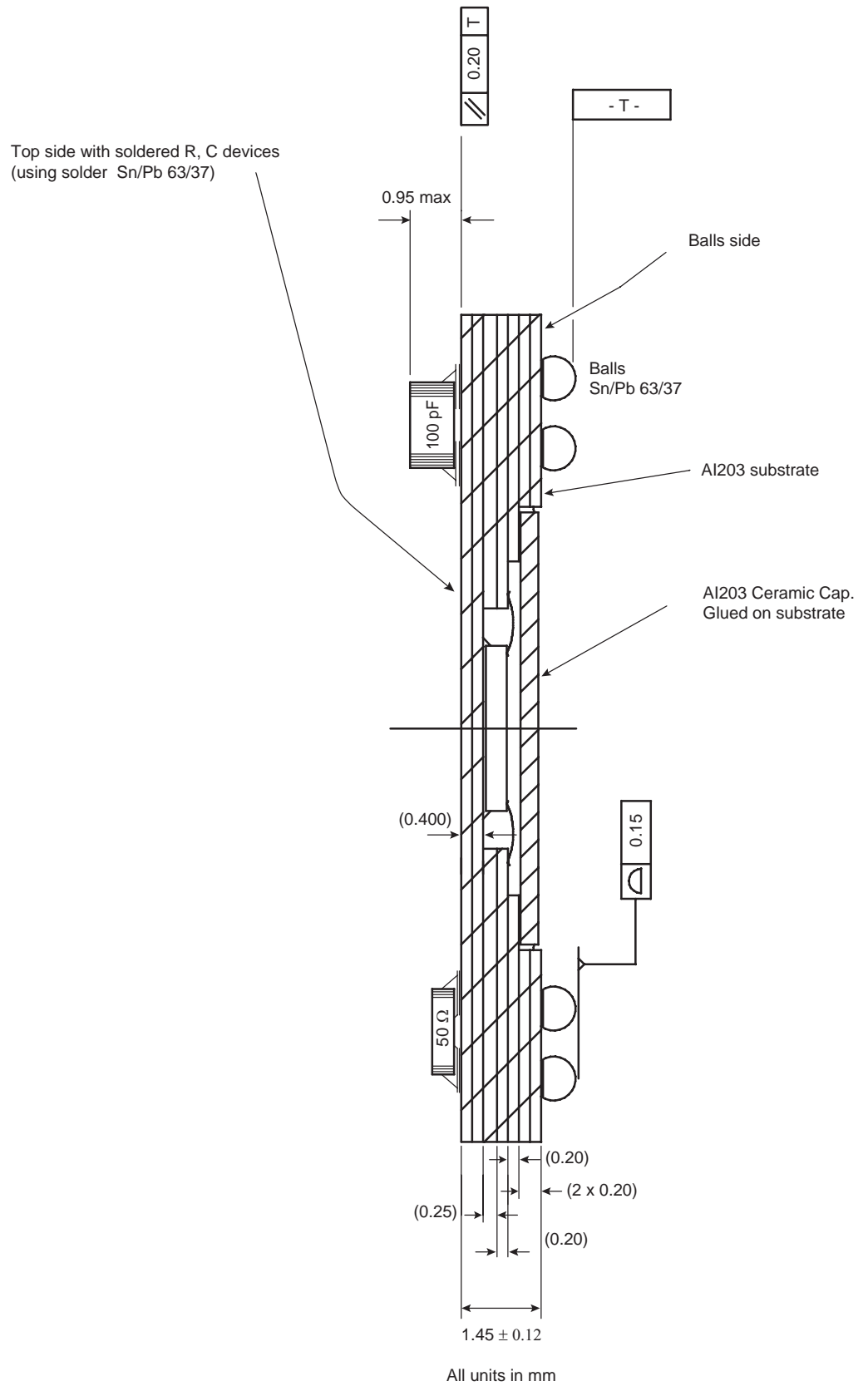
Thermal And Moisture Characteristics

Thermal Resistance from Junction to Ambient: RTHJA

The following table lists the convection thermal performances parameters of the device itself, with no external heatsink added.

Table 9. Thermal Resistance

Air Flow (m/s)	Estimated ja Thermal Resistance (°C/W)	
0	45	
0.5	35.8	
1	30.8	
1.5	27.4	
2	24.9	
2.5	23	
3	21.5	
4	19.3	
5	17.7	

Thermal Resistance from Junction to Case: RTHJC

The typical value for Rthjc is given as 6.7°C/W (8°C/W max).

This value does not include thermal contact resistance between package and external component (heatsink or PC Board).

As an example, 2.0°C/W can be taken for 50 μm of thermal grease.

CBGA68 Board Assembly with External Heatsink

It is recommended that an external heatsink or specifically designed PCB be used. Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

Figure 51. CBGA68 Board Assembly
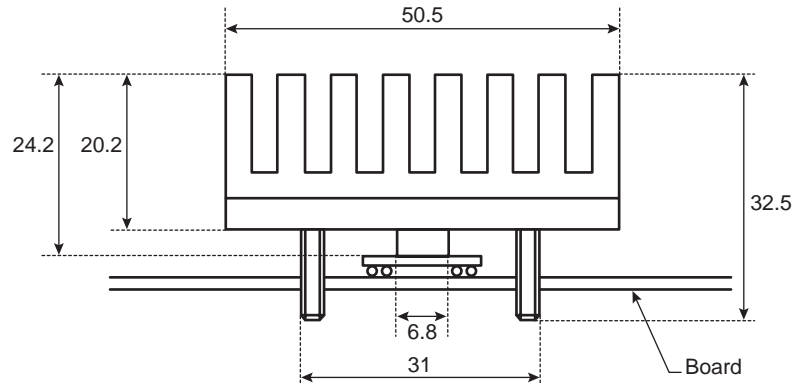
Note: Units = mm

Moisture Characteristics

This device is sensitive to moisture (MSL3 according to JEDEC standard):

Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220°C) must be:

• mounted within 198 hours at factory conditions of ≤30°C/60% RH, or

• stored at ≤20% RH

Devices require baking, before mounting, if Humidity Indicator Card is >20% when read at 23°C ±5°C.

If baking is required, devices may be baked for:

• 192 hours at 40°C +5°C/-0°C and <5% RH for low-temperature device containers, or

• 24 hours at 125°C ±5°C for high temperature device containers

Definitions

Definition of Terms

(BER) Bit Error Rate
Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than ±4 LSB from the correct code.

(BW) Full-Power Input Bandwidth
Analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale.

(DG) Differential Gain
The peak gain variation (in percent) at five different DC levels for an AC signal of 20% Full-Scale peak to peak amplitude. F_{IN} = 5 MHz (TBC).

(DNL) Differential Non-Linearity
The Differential Non-Linearity for an output code (i) is the difference between the measured step size of code (i) and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.

(DP) Differential Phase
Peak Phase variation (in degrees) at five different DC levels for an AC signal of 20% Full-Scale peak to peak amplitude. F_{IN} = 5 MHz (TBC).

(ENOB) Effective Number of Bits

$$ENOB = \frac{SINAD - 1.76 + 20 \log (A/V/2)}{6.02}$$

Where A is the actual input amplitude and V is the full-scale range of the ADC under test.

(IMD) InterModulation Distortion
The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at -7 dB full-scale.

(INL) Integral Non-Linearity
The Integral Non-Linearity for an output code (i) is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.

(JITTER) Aperture Uncertainty
Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

(NPR) Noise Power Ratio
The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.

(NRZ) Non-Return to Zero
When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of Range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).

(ORT) Overvoltage Recovery Time
Time to recover 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale.

(PSRR) Power Supply Rejection Ratio	Ratio of input offset variation to a change in power supply voltage.
(SFDR) Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (Radar systems, digital receiver, network analyzer, etc.). It may be reported in dBc (i.e.: degrades as signal level is lowered), or in dBFS (i.e.: always related back to converter full scale)
(SINAD) Signal to Noise and Distortion Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR) Signal to Noise Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the five first harmonics.
(TA) Aperture Delay	Delay between the rising edge of the differential clock inputs (CLK, CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled.
(TC) Encoding Clock Period	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TD1) Time Delay from Data to Data Ready	Time delay from Data transition to Data Ready.
(TD2) Time Delay from Data Ready to Data	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TF) Fall Time	Time delay for the output Data signals to fall from 80% to 20% of delta between low level and high level.
(THD) Total Harmonic Distorsion	Ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component.
(TOD) Digital Data Output Delay	Delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with a specified load.
(TPD) Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD). For the TS8388BF the TPD is 4 clock periods.
(TR) Rise Time	Time delay for the output Data signals to rise from 20% to 80% of delta between low level and high level.
(TRDR) Data Ready Reset Delay	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR).
(TS) Settling Time	Time delay to achieve 0.2% accuracy at the converter output when a 80% full-scale step function is applied to the differential analog input.

Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
TSX8308500GL	CBGA 68	Ambient	Prototype	Prototype version
TS8308500CGL	CBGA 68	"C" grade $0°C < Tc ; Tj < 90°C$	Standard	
TS8308500VGL	CBGA 68	"V" grade $-40°C < Tc ; Tj < 110°C$	Standard	
TSEV8308500GL	CBGA 68	Ambient	Prototype	Evaluation Board (delivered with a heat sink)
TSEV8308500GLZA2	CBGA 68	Ambient	Prototype	Evaluation Board with digital output buffers (delivered with a heat sink)

Datasheet Status Description

Table 10. Datasheet Status

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet also contains characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

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