



**HIGH-SPEED 3.3V  
128/64K x 36  
SYNCHRONOUS  
DUAL-PORT STATIC RAM  
WITH 3.3V OR 2.5V INTERFACE**

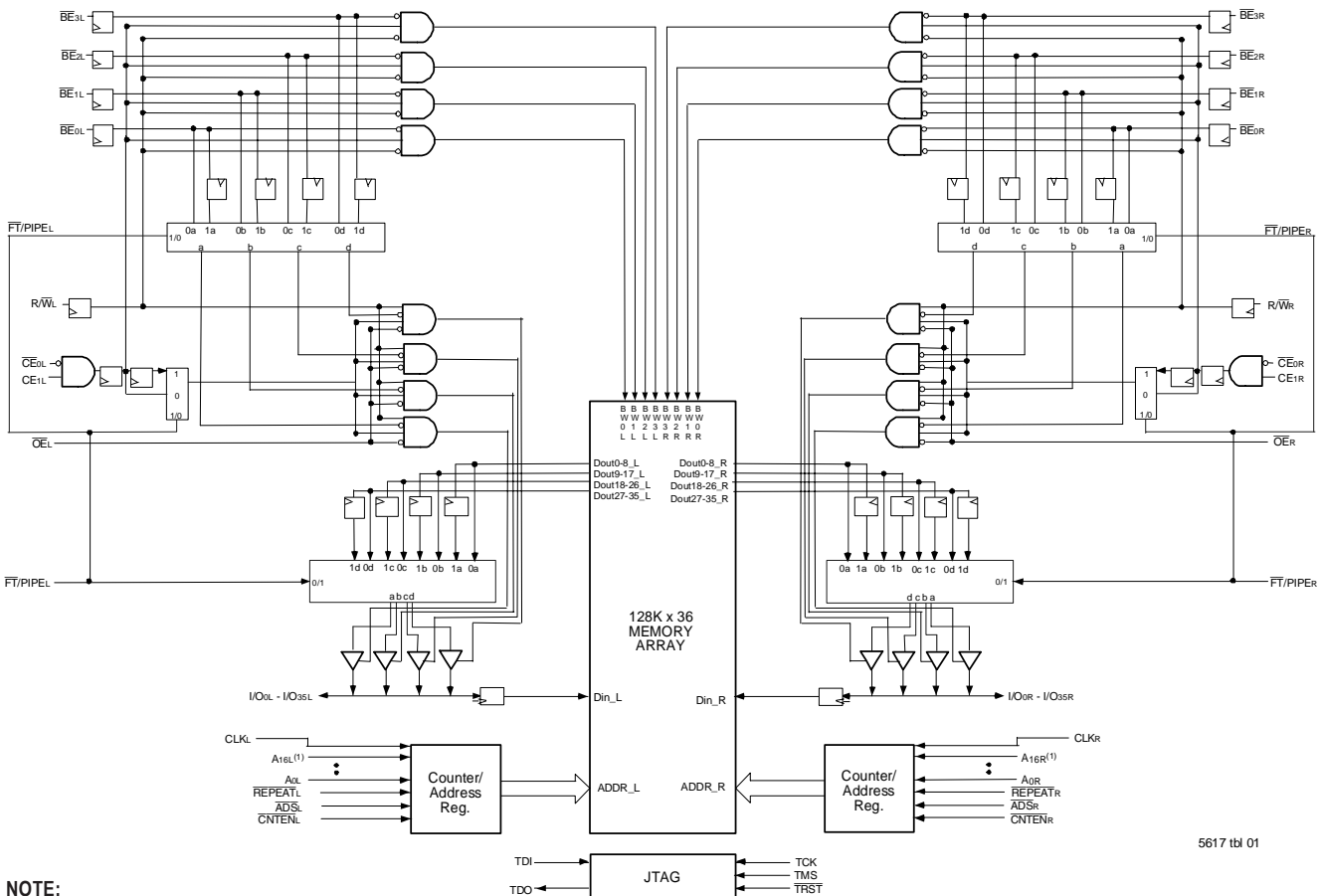
**IDT70V3599/89S**

**Features:**

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed data access
  - Commercial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
  - Industrial: 4.2ns (133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 6ns cycle time, 166MHz operation (12Gbps bandwidth)
  - Fast 3.6ns clock to data out
  - 1.7ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz
  - Data input, address, byte enable and control registers
  - Self-timed write allows fast cycle time

- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ Dual Cycle Deselect (DCD) for Pipelined Output mode
- ◆ LVTTTL-compatible, 3.3V (±150mV) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available at 133MHz.
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-pin fine pitch Ball Grid Array (fpBGA), and 256-pin Ball Grid Array (BGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1

**Functional Block Diagram**



5617 tbl 01

**NOTE:**

1. A16 is a NC for IDT70V3589.

**MAY 2003**

### Description:

The IDT70V3599/89 is a high-speed 128/64K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3599/89 has been optimized for applications having unidirectional

or bidirectional data flow in bursts. An automatic power down feature, controlled by CE<sub>0</sub> and CE<sub>1</sub>, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3599/89 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

### Pin Configuration(1,2,3,4,5)

06/28/02

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	
I/O19L	I/O18L	VSS	TDO	NC	A16L <sup>(1)</sup>	A12L	A8L	BE <sub>1</sub> L	VDD	CLKL	CNTENL	A4L	A0L	OPTL	I/O17L	VSS	
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	
I/O20R	VSS	I/O18R	TDI	NC	A13L	A9L	BE <sub>2</sub> L	CE <sub>0</sub> L	VSS	ADSL	A5L	A1L	VSS	VDDQR	I/O16L	I/O15R	
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	
VDDQL	I/O19R	VDDQR	PL/F <sub>T</sub> L	NC	A14L	A10L	BE <sub>3</sub> L	CE <sub>1</sub> L	VSS	R <sub>W</sub> L	A6L	A2L	VDD	I/O16R	I/O15L	VSS	
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	
I/O22L	VSS	I/O21L	I/O20L	A15L	A11L	A7L	BE <sub>0</sub> L	VDD	OE <sub>L</sub>	REPEATL	A3L	VDD	I/O17R	VDDQL	I/O14L	I/O14R	
E1	E2	E3	E4	<b>70V3599/89BF</b> <b>BF-208<sup>(6)</sup></b>  <b>208-Pin fpBGA</b> <b>Top View<sup>(7)</sup></b>										E14	E15	E16	E17
I/O23L	I/O22R	VDDQR	I/O21R											I/O12L	I/O13R	VSS	I/O13L
F1	F2	F3	F4											F14	F15	F16	F17
VDDQL	I/O23R	I/O24L	VSS											VSS	I/O12R	I/O11L	VDDQR
G1	G2	G3	G4											G14	G15	G16	G17
I/O26L	VSS	I/O25L	I/O24R											I/O9L	VDDQL	I/O10L	I/O11R
H1	H2	H3	H4											H14	H15	H16	H17
VDD	I/O26R	VDDQR	I/O25R											VDD	IO9R	VSS	I/O10R
J1	J2	J3	J4											J14	J15	J16	J17
VDDQL	VDD	VSS	VSS											VSS	VDD	VSS	VDDQR
K1	K2	K3	K4	K14	K15	K16	K17										
I/O28R	VSS	I/O27R	VSS	I/O7R	VDDQL	I/O8R	VSS										
L1	L2	L3	L4	L14	L15	L16	L17										
I/O29R	I/O28L	VDDQR	I/O27L	I/O6R	I/O7L	VSS	I/O8L										
M1	M2	M3	M4	M14	M15	M16	M17										
VDDQL	I/O29L	I/O30R	VSS	VSS	I/O6L	I/O5R	VDDQR										
N1	N2	N3	N4	N14	N15	N16	N17										
I/O31L	VSS	I/O31R	I/O30L	I/O3R	VDDQL	I/O4R	I/O5L										
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	
I/O32R	I/O32L	VDDQR	I/O35R	TRST	A16R <sup>(1)</sup>	A12R	A8R	BE <sub>1</sub> R	VDD	CLKR	CNTENR	A4R	I/O2L	I/O3L	VSS	I/O4L	
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	
VSS	I/O33L	I/O34R	TCK	NC	A13R	A9R	BE <sub>2</sub> R	CE <sub>0</sub> R	VSS	ADSR	A5R	A1R	VSS	VDDQL	I/O1R	VDDQR	
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	
I/O33R	I/O34L	VDDQL	TMS	NC	A14R	A10R	BE <sub>3</sub> R	CE <sub>1</sub> R	VSS	R <sub>W</sub> R	A6R	A2R	VSS	I/O0R	VSS	I/O2R	
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	
VSS	I/O35L	PL/F <sub>T</sub> R	NC	A15R	A11R	A7R	BE <sub>0</sub> R	VDD	OE <sub>R</sub>	REPEATR	A3R	A0R	VDD	OPTR	I/O0L	I/O1L	

5617 drw 02c

**NOTES:**

1. A16 is a NC for IDT70V3589.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

**Pin Configuration<sup>(1,2,3,4,5)</sup> (con't.)**

70V3599/89BC

BC-256<sup>(6)</sup>

256-Pin BGA

Top View<sup>(7)</sup>

06/28/02

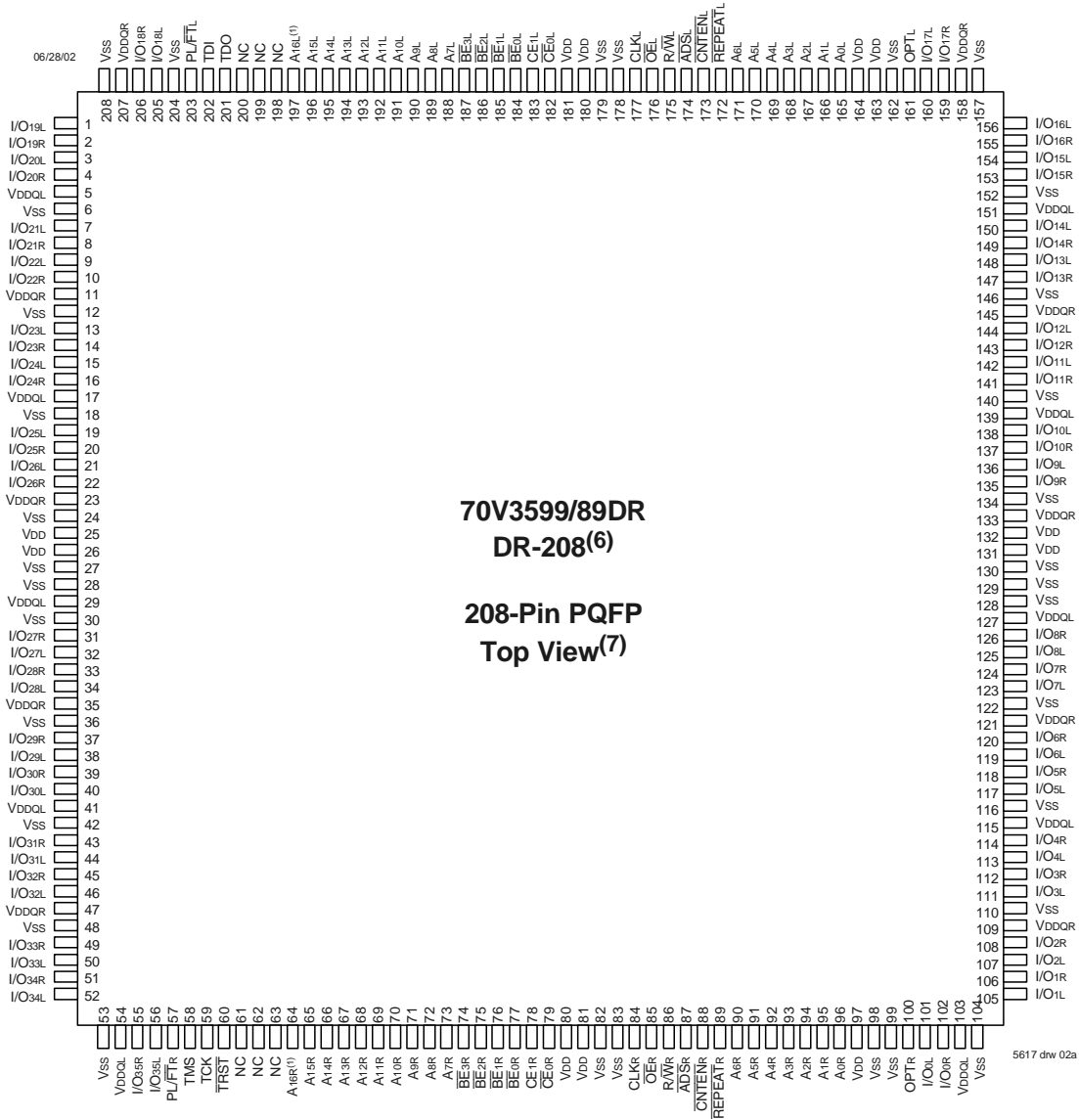
A1 NC	A2 TDI	A3 NC	A4 NC	A5 A14L	A6 A11L	A7 A8L	A8 $\overline{BE}_{2L}$	A9 CE1L	A10 $\overline{OE}_{L}$	A11 CNTENL	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 I/O18L	B2 NC	B3 TDO	B4 NC	B5 A15L	B6 A12L	B7 A9L	B8 $\overline{BE}_{3L}$	B9 $\overline{CE}_{0L}$	B10 R/WL	B11 $\overline{REPEAT}_{L}$	B12 A4L	B13 A1L	B14 VDD	B15 I/O17L	B16 NC
C1 I/O18R	C2 I/O19L	C3 VSS	C4 A16L <sup>(1)</sup>	C5 A13L	C6 A10L	C7 A7L	C8 $\overline{BE}_{1L}$	C9 $\overline{BE}_{0L}$	C10 CLKL	C11 $\overline{AD}_{SL}$	C12 A6L	C13 A3L	C14 OPTL	C15 I/O17R	C16 I/O16L
D1 I/O20R	D2 I/O19R	D3 I/O20L	D4 PIPE/F $\overline{T}$ L	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 I/O15R	D15 I/O15L	D16 I/O16R
E1 I/O21R	E2 I/O21L	E3 I/O22L	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 I/O13L	E15 I/O14L	E16 I/O14R
F1 I/O23L	F2 I/O22R	F3 I/O23R	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O12R	F15 I/O13R	F16 I/O12L
G1 I/O24R	G2 I/O24L	G3 I/O25L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O10L	G15 I/O11L	G16 I/O11R
H1 I/O26L	H2 I/O25R	H3 I/O26R	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 I/O9R	H15 I/O9L	H16 I/O10R
J1 I/O27L	J2 I/O28R	J3 I/O27R	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQR	J14 I/O8R	J15 I/O7R	J16 I/O8L
K1 I/O29R	K2 I/O29L	K3 I/O28L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 I/O6R	K15 I/O6L	K16 I/O7L
L1 I/O30L	L2 I/O31R	L3 I/O30R	L4 VDDQR	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O5L	L15 I/O4R	L16 I/O5R
M1 I/O32R	M2 I/O32L	M3 I/O31L	M4 VDDQR	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O3R	M15 I/O3L	M16 I/O4L
N1 I/O33L	N2 I/O34R	N3 I/O33R	N4 PIPE/F $\overline{T}$ R	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 I/O2L	N15 I/O1R	N16 I/O2R
P1 I/O35R	P2 I/O34L	P3 TMS	P4 A16R <sup>(1)</sup>	P5 A13R	P6 A10R	P7 A7R	P8 $\overline{BE}_{1R}$	P9 $\overline{BE}_{0R}$	P10 CLKR	P11 $\overline{AD}_{SR}$	P12 A6R	P13 A3R	P14 I/O0L	P15 I/O0R	P16 I/O1L
R1 I/O35L	R2 NC	R3 $\overline{TR}_{ST}$	R4 NC	R5 A15R	R6 A12R	R7 A9R	R8 $\overline{BE}_{3R}$	R9 $\overline{CE}_{0R}$	R10 R/WR	R11 $\overline{REPEAT}_{R}$	R12 A4R	R13 A1R	R14 OPTR	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 NC	T5 A14R	T6 A11R	T7 A8R	T8 $\overline{BE}_{2R}$	T9 CE1R	T10 $\overline{OE}_{R}$	T11 CNTENR	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

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**NOTES:**

1. A16 is a NC for IDT70V3589.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

**Pin Configuration<sup>(1,2,3,4,5)</sup> (con't.)**



**70V3599/89DR  
DR-208<sup>(6)</sup>  
208-Pin PQFP  
Top View<sup>(7)</sup>**

**NOTES:**

1. A16 is a NC for IDT70V3589.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 28mm x 28mm x 3.5mm.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , $CE_{1L}$	$\overline{CE}_{0R}$ , $CE_{1R}$	Chip Enables <sup>(5)</sup>
$R/\overline{WL}$	$R/\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}$ - $A_{16L}$ <sup>(1)</sup>	$A_{0R}$ - $A_{16R}$ <sup>(1)</sup>	Address
$I/O_{0L}$ - $I/O_{35L}$	$I/O_{0R}$ - $I/O_{35R}$	Data Input/Output
$CLK_L$	$CLK_R$	Clock
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$REPEAT_L$	$REPEAT_R$	Counter Repeat <sup>(4)</sup>
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes) <sup>(5)</sup>
$V_{DDQL}$	$V_{DDQR}$	Power (I/O Bus) (3.3V or 2.5V) <sup>(2)</sup>
$OPT_L$	$OPT_R$	Option for selecting $V_{DDQX}$ <sup>(2,3)</sup>
$V_{DD}$		Power (3.3V) <sup>(2)</sup>
$V_{SS}$		Ground (0V)
$TDI$		Test Data Input
$TDO$		Test Data Output
$TCK$		Test Logic Clock (10MHz)
$TMS$		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

5617 tbl 01

### NOTES:

1.  $A_{16}$  is a NC for IDT70V3589.
2.  $V_{DD}$ ,  $OPT_X$ , and  $V_{DDQX}$  must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
3.  $OPT_X$  selects the operating voltage levels for the I/Os and controls on that port. If  $OPT_X$  is set to  $V_{IH}$  (3.3V), then that port's I/Os and controls will operate at 3.3V levels and  $V_{DDQX}$  must be supplied at 3.3V. If  $OPT_X$  is set to  $V_{IL}$  (0V), then that port's I/Os and address controls will operate at 2.5V levels and  $V_{DDQX}$  must be supplied at 2.5V. The  $OPT$  pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
4. When  $REPEAT_X$  is asserted, the counter will reset to the last valid address loaded via  $\overline{ADS}_X$ .
5. Chip Enables and Byte Enables are double buffered when  $PL/\overline{FT} = V_{IH}$ , i.e., the signals take two cycles to deselect.

**Truth Table I—Read/Write and Enable Control<sup>(1,2,3,4)</sup>**

OE	CLK	CE <sub>0</sub>	CE <sub>1</sub>	BE <sub>3</sub>	BE <sub>2</sub>	BE <sub>1</sub>	BE <sub>0</sub>	R/W	Byte 3 I/O <sub>27-35</sub>	Byte 2 I/O <sub>18-26</sub>	Byte 1 I/O <sub>9-17</sub>	Byte 0 I/O <sub>0-8</sub>	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	DN	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	DN	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	DN	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	DN	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	DN	DN	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	DN	DN	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	DN	DN	DN	DN	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	DOUT	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	DOUT	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	DOUT	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	DOUT	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	DOUT	DOUT	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	DOUT	DOUT	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	DOUT	DOUT	DOUT	DOUT	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- ADS, CNTEN, REPEAT = V<sub>IH</sub>.
- OE is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

5617 tbl 02

**Truth Table II—Address Counter Control<sup>(1,2)</sup>**

External Address	Previous Internal Address	Internal Address Used	CLK	ADS	CNTEN	REPEAT <sup>(6)</sup>	I/O <sup>(6)</sup>	MODE
X	X	A <sub>n</sub>	↑	X	X	L <sup>(4)</sup>	D <sub>VO</sub> (0)	Counter Reset to last valid ADS load
A <sub>n</sub>	X	A <sub>n</sub>	↑	L <sup>(4)</sup>	X	H	D <sub>VO</sub> (n)	External Address Used
A <sub>n</sub>	A <sub>p</sub>	A <sub>p</sub>	↑	H	H	H	D <sub>VO</sub> (p)	External Address Blocked—Counter disabled (A <sub>p</sub> reused)
X	A <sub>p</sub>	A <sub>p</sub> + 1	↑	H	L <sup>(5)</sup>	H	D <sub>VO</sub> (p+1)	Counter Enabled—Internal Address generation

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/W, CE<sub>0</sub>, CE<sub>1</sub>, BE<sub>n</sub> and OE.
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- ADS and REPEAT are independent of all other memory control signals including CE<sub>0</sub>, CE<sub>1</sub> and BE<sub>n</sub>.
- The address counter advances if CNTEN = V<sub>IL</sub> on the rising edge of CLK, regardless of all other memory control signals including CE<sub>0</sub>, CE<sub>1</sub>, BE<sub>n</sub>.
- When REPEAT is asserted, the counter will reset to the last valid address loaded via ADS. This value is not set at power-up: a known location should be loaded via ADS during initialization if desired. Any subsequent ADS access during operations will update the REPEAT address location.

5617 tbl 03

## Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V $\pm$ 150mV
Industrial	-40°C to +85°C	0V	3.3V $\pm$ 150mV

5617 tbl 04

### NOTES:

- This is the parameter TA. This is the "instant on" case temperature.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub> <sup>(3)</sup>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub>	Junction Temperature	+150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

5617 tbl 06

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to  $\leq 20$ mA for the period of V<sub>TERM</sub>  $\geq$  V<sub>DD</sub> + 150mV.
- Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

## Recommended DC Operating Conditions with V<sub>DDQ</sub> at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	2.4	2.5	2.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs)	1.7	—	V <sub>DDQ</sub> + 100mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	1.7	—	V <sub>DDQ</sub> + 100mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

5617 tbl 05a

### NOTES:

- Undershoot of V<sub>IL</sub>  $\geq$  -1.5V for pulse width less than 10ns is allowed.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 100mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IL</sub> (0V), and V<sub>DDQX</sub> for that port must be supplied as indicated above.

## Recommended DC Operating Conditions with V<sub>DDQ</sub> at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	3.15	3.3	3.45	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs) <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

5617 tbl 05b

### NOTES:

- Undershoot of V<sub>IL</sub>  $\geq$  -1.5V for pulse width less than 10ns is allowed.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IH</sub> (3.3V), and V<sub>DDQX</sub> for that port must be supplied as indicated above.

## Capacitance<sup>(1)</sup>

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10.5	pF

5617 tbl 07

### NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C<sub>OUT</sub> also references C<sub>I/O</sub>.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3599/89S		Unit
			Min.	Max.	
I <sub>L</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DDQ</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
I <sub>O</sub>	Output Leakage Current <sup>(1)</sup>	$\overline{CE_0} = V_H$ or $CE_1 = V_L$ , V <sub>OUT</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
V <sub>OL</sub> (3.3V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +4mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (3.3V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -4mA, V <sub>DDQ</sub> = Min.	2.4	—	V
V <sub>OL</sub> (2.5V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +2mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (2.5V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -2mA, V <sub>DDQ</sub> = Min.	2.0	—	V

5617 tbl 08

### NOTE:

- At V<sub>DD</sub> ≤ 2.0V leakages are undefined.
- V<sub>DDQ</sub> is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.



## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ )

Symbol	Parameter	Test Condition	Version	70V3599/89S166 Com'l Only		70V3599/89S133 Com'l & Ind		Unit	
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	370	500	320	400	mA
			IND	S	—	—	320	480	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	125	200	115	160	mA
			IND	S	—	—	115	195	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports Outputs Disabled $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	S	15	30	15	30	mA
			IND	S	—	—	15	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	

5617 tbl 09

**NOTES:**

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $I_{DD} \text{ dc}(f=0) = 120mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{CC} - 0.2V$   
 $\overline{CE}_X \geq V_{CC} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{CC} - 0.2V$  or  $CE_{1X} = 0.2V$   
 "X" represents "L" for left port or "R" for right port.

**AC Test Conditions (V<sub>DDQ</sub> - 3.3V/2.5V)**

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5617 tbl 10

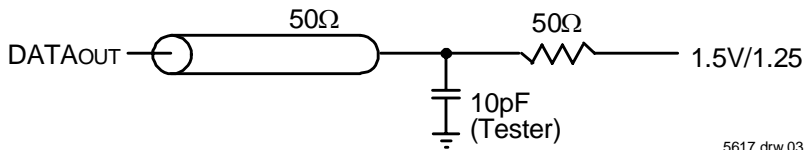


Figure 1. AC Output Test load.

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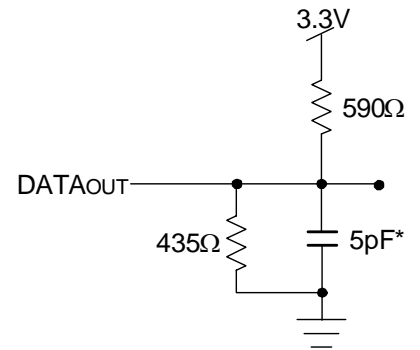
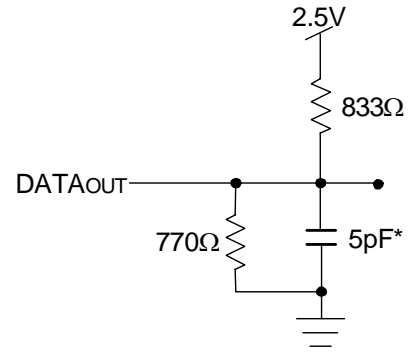
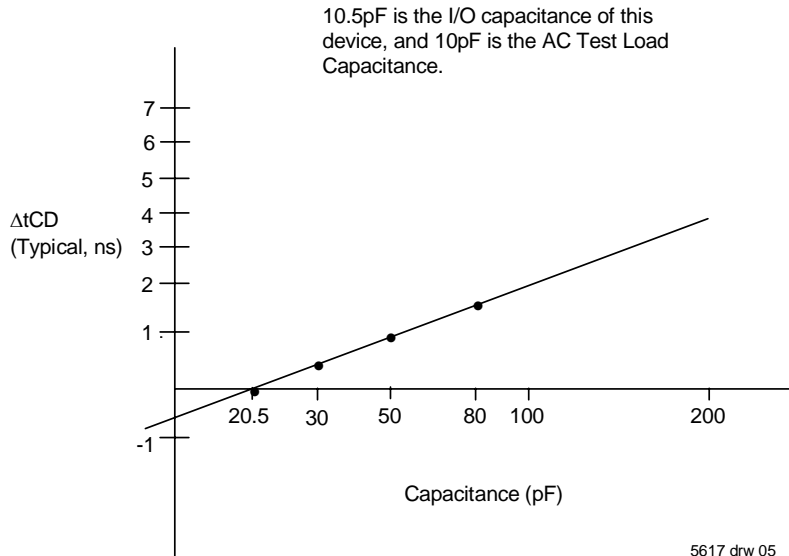


Figure 2. Output Test Load  
(For t<sub>CKLZ</sub>, t<sub>CKHZ</sub>, t<sub>OLZ</sub>, and t<sub>OHZ</sub>).  
\*Including scope and jig.

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Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(2,3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

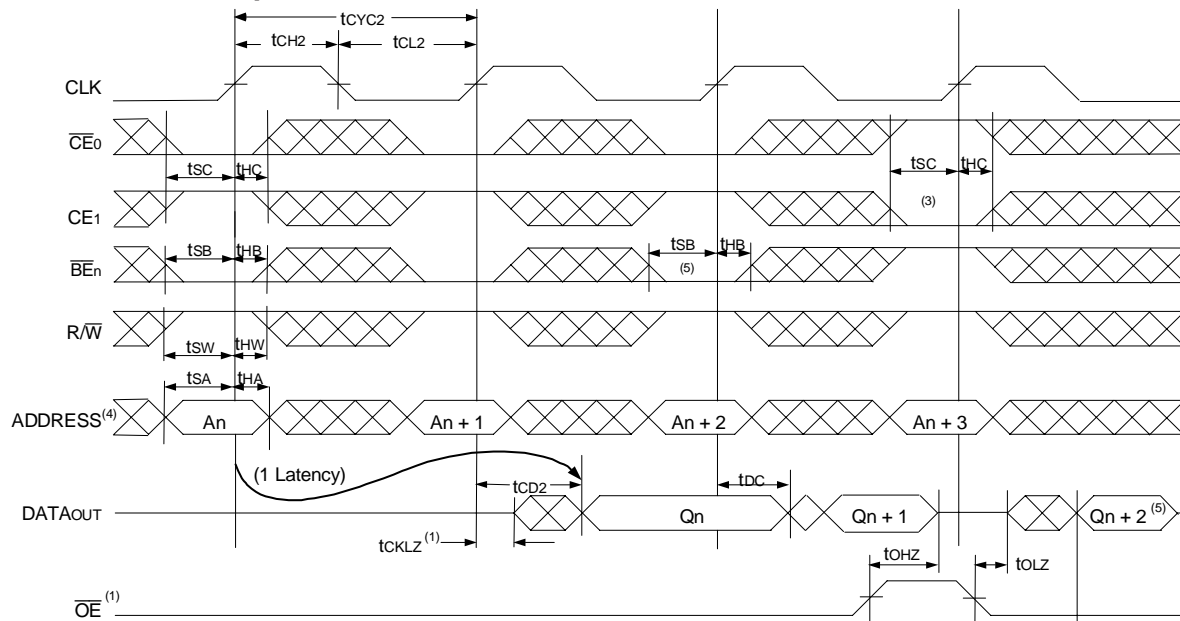
Symbol	Parameter	70V3599/89S166 Com'1 Only		70V3599/89S133 Com'1 & Ind		Unit
		Min.	Max.	Min.	Max.	
t <sub>CYC1</sub>	Clock Cycle Time (Flow-Through) <sup>(1)</sup>	20	—	25	—	ns
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined) <sup>(1)</sup>	6	—	7.5	—	ns
t <sub>CH1</sub>	Clock High Time (Flow-Through) <sup>(1)</sup>	6	—	7	—	ns
t <sub>CL1</sub>	Clock Low Time (Flow-Through) <sup>(1)</sup>	6	—	7	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined) <sup>(2)</sup>	2.1	—	2.6	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined) <sup>(1)</sup>	2.1	—	2.6	—	ns
t <sub>SA</sub>	Address Setup Time	1.7	—	1.8	—	ns
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	1.7	—	1.8	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0.5	—	0.5	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	1.7	—	1.8	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0.5	—	0.5	—	ns
t <sub>SW</sub>	R/W Setup Time	1.7	—	1.8	—	ns
t <sub>HW</sub>	R/W Hold Time	0.5	—	0.5	—	ns
t <sub>SD</sub>	Input Data Setup Time	1.7	—	1.8	—	ns
t <sub>HD</sub>	Input Data Hold Time	0.5	—	0.5	—	ns
t <sub>SAD</sub>	$\overline{ADS}$ Setup Time	1.7	—	1.8	—	ns
t <sub>HAD</sub>	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ Setup Time	1.7	—	1.8	—	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
t <sub>SRPT</sub>	$\overline{REPEAT}$ Setup Time	1.7	—	1.8	—	ns
t <sub>HRPT</sub>	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
t <sub>OE</sub>	Output Enable to Data Valid	—	4.0	—	4.2	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z	1	—	1	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t <sub>CD1</sub>	Clock to Data Valid (Flow-Through) <sup>(1)</sup>	—	12	—	15	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined) <sup>(1)</sup>	—	3.6	—	4.2	ns
t <sub>DC</sub>	Data Output Hold After Clock High	1	—	1	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z	1	3	1	3	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z	1	—	1	—	ns
<b>Port-to-Port Delay</b>						
t <sub>CO</sub>	Clock-to-Clock Offset	5	—	6	—	ns

5617 tbl 11

**NOTES:**

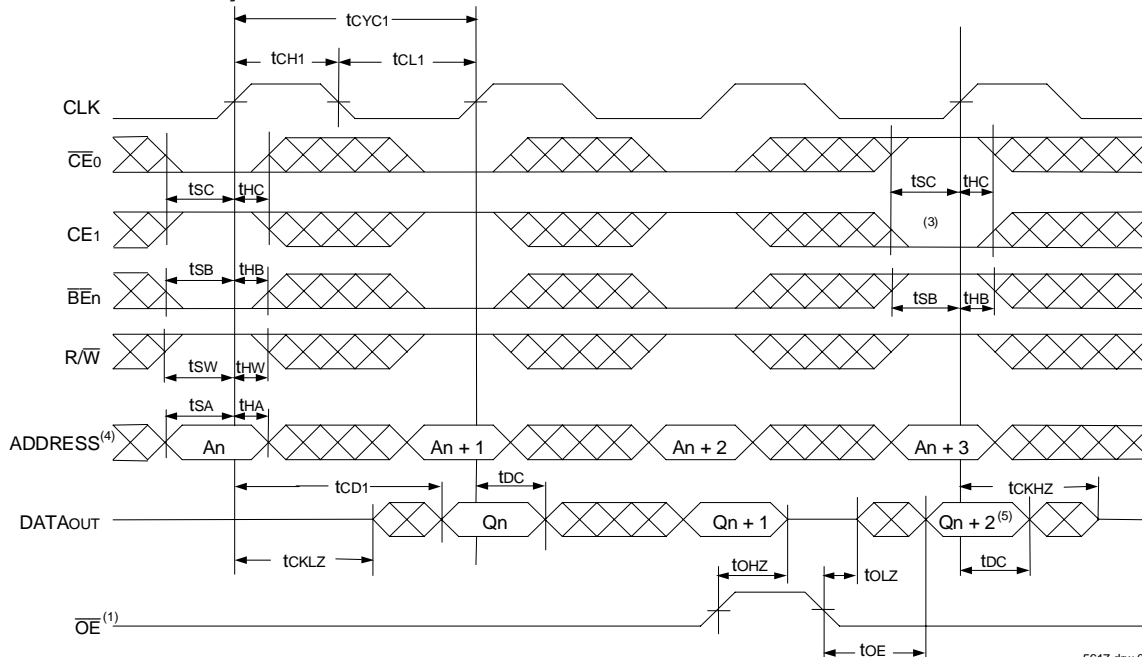
- The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both left and right ports when  $\overline{FT}/PIPE_x = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPE_x = V_{IL}$  for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of  $V_{DDQ}$  (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.

### Timing Waveform of Read Cycle for Pipelined Operation ( $\overline{FT}/PIPE^*x = V_{IH}$ )<sup>(2)</sup>



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### Timing Waveform of Read Cycle for Flow-through Output ( $\overline{FT}/PIPE^*x = V_{IL}$ )<sup>(2,6)</sup>

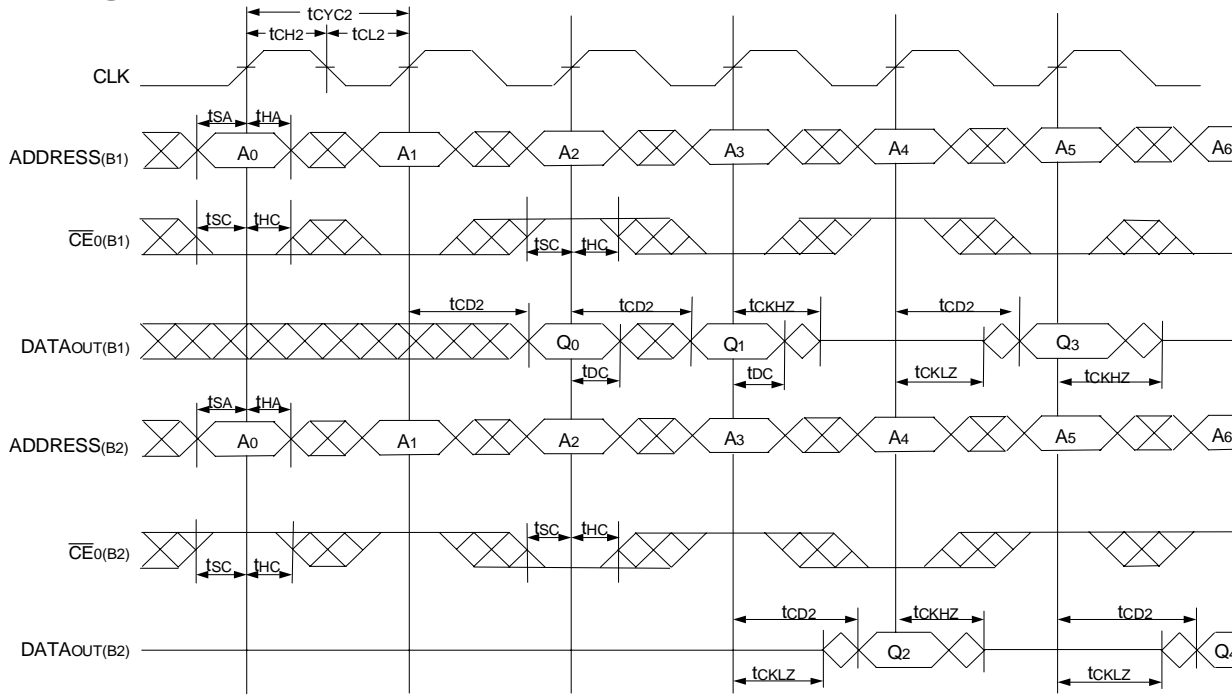


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**NOTES:**

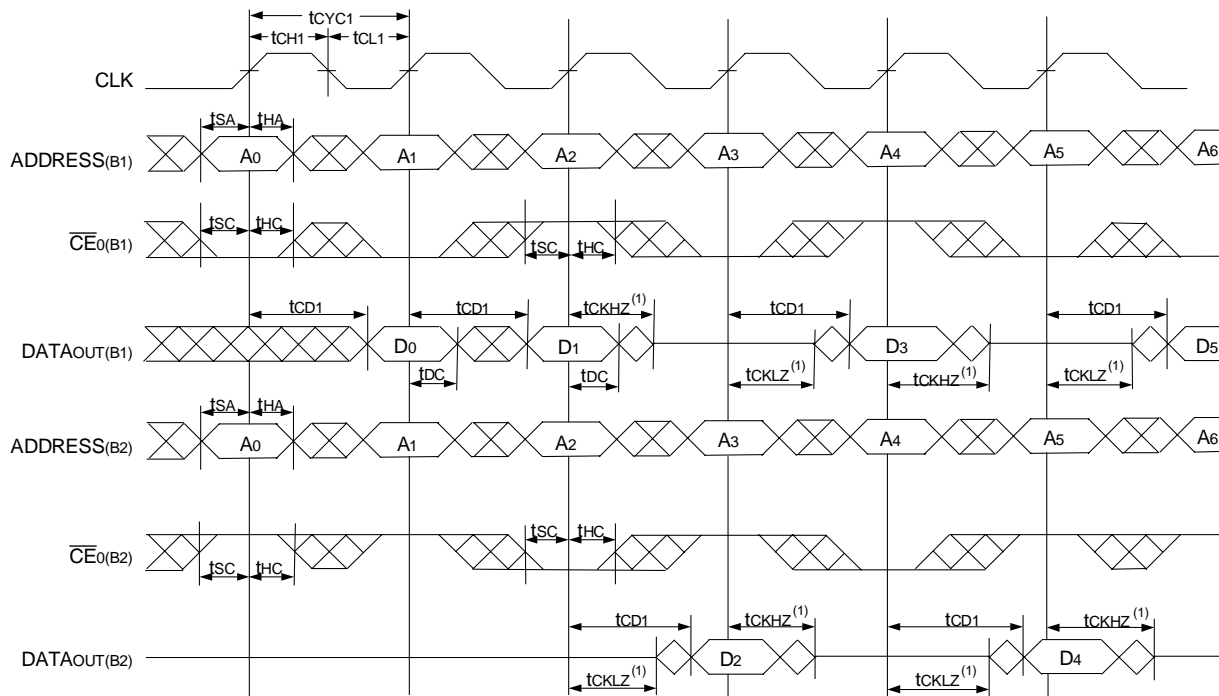
1.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2.  $\overline{ADS} = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{REPEAT} = V_{IH}$ .
3. The output is disabled (High-Impedance state) by  $\overline{CE}_0 = V_{IH}$ ,  $CE_1 = V_{IL}$ ,  $\overline{BE}_n = V_{IH}$  following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If  $\overline{BE}_n$  was HIGH, then the appropriate Byte of DATAout for  $Q_n + 2$  would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

### Timing Waveform of a Multi-Device Pipelined Read<sup>(1,2)</sup>



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### Timing Waveform of a Multi-Device Flow-Through Read<sup>(1,2)</sup>

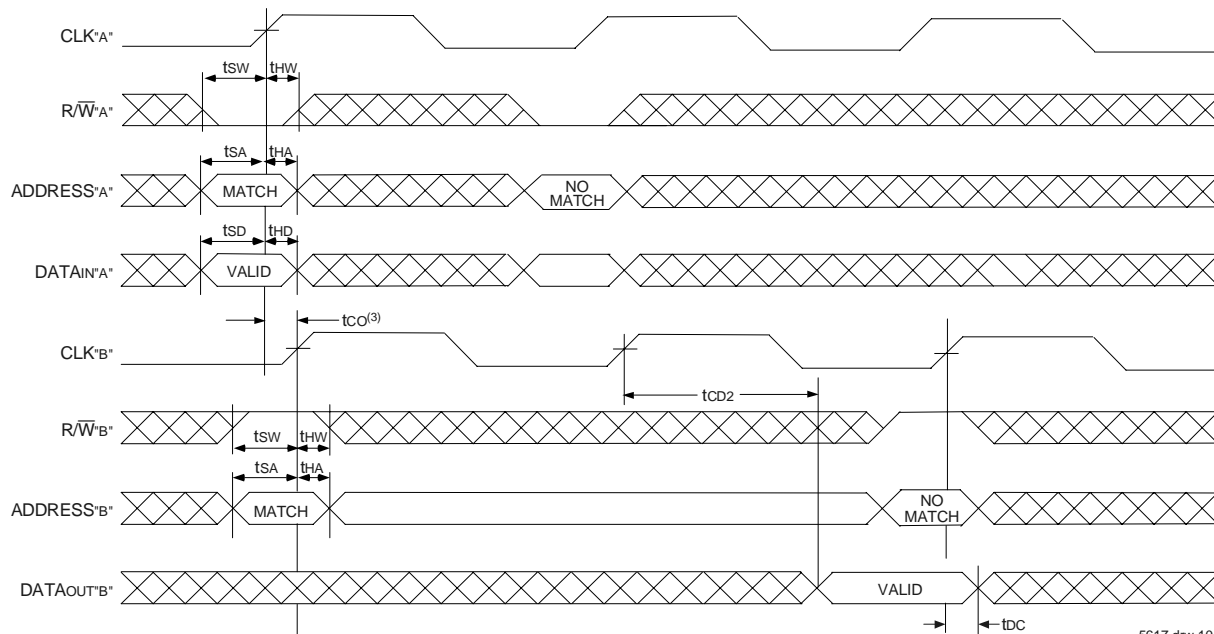


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**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3599/89 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. BE<sub>n</sub>, OE, and ADS = V<sub>IL</sub>; CE<sub>1</sub>(B1), CE<sub>1</sub>(B2), R/W, CNTEN, and REPEAT = V<sub>IH</sub>.

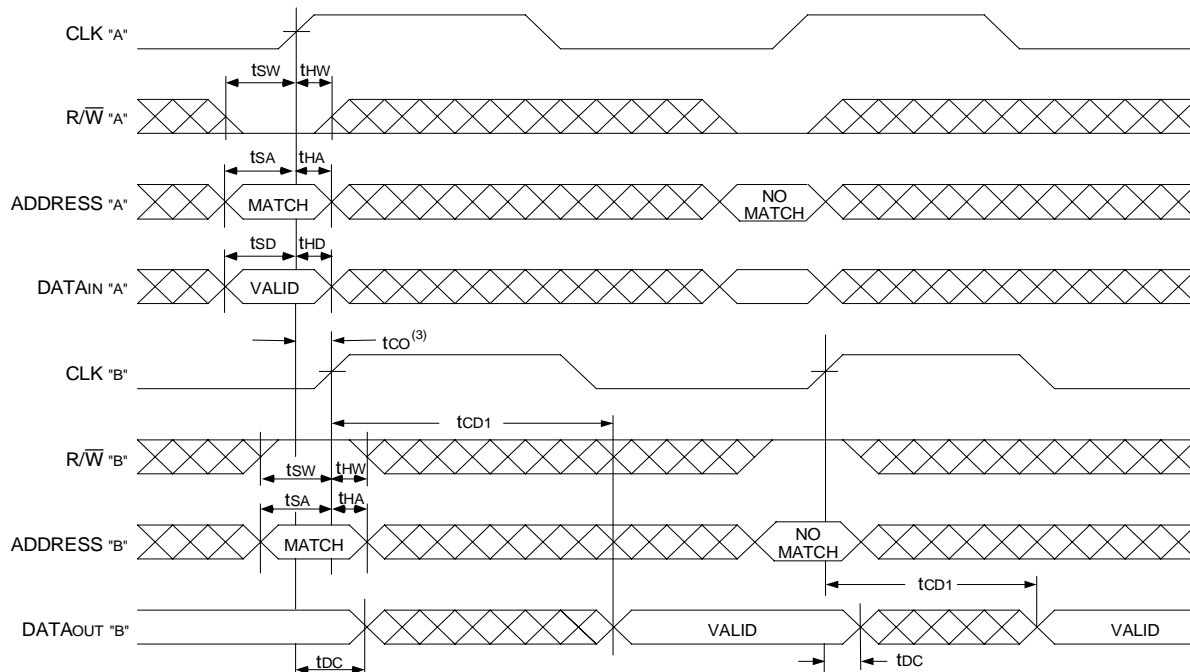
### Timing Waveform of Left Port Write to Pipelined Right Port Read<sup>(1,2,4)</sup>



**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for Port "B", which is being read from.  $\overline{OE} = V_{IH}$  for Port "A", which is being written to.
3. If  $t_{CO} \leq$  minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + 2 t_{CYC2} + t_{CD2}$ ). If  $t_{CO} >$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + t_{CYC2} + t_{CD2}$ ).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

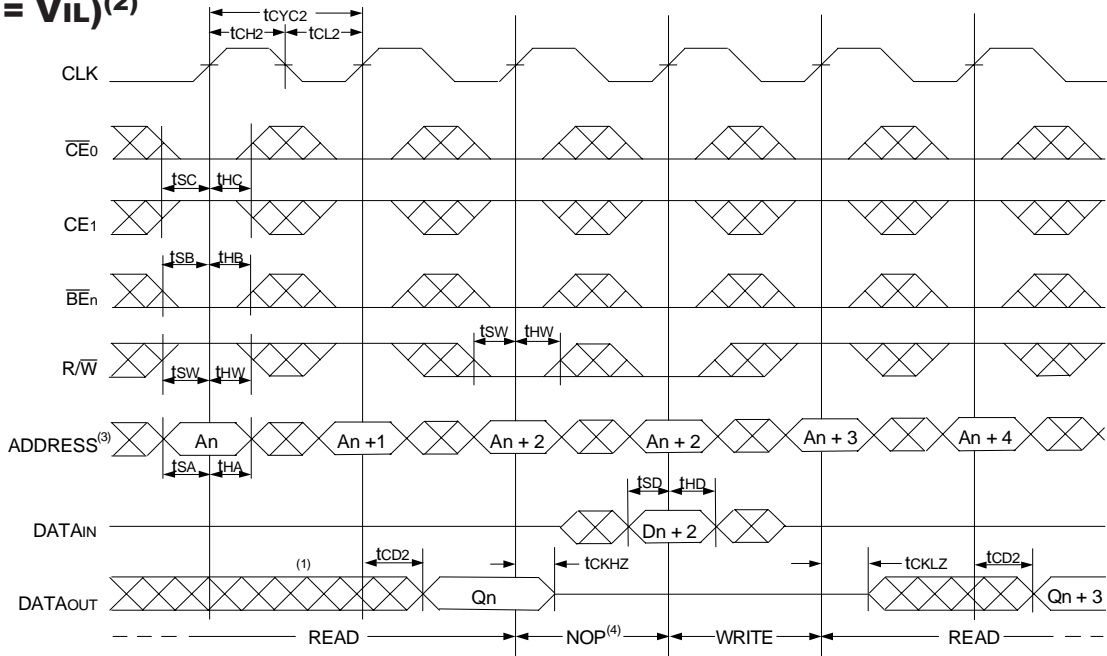
### Timing Waveform with Port-to-Port Flow-Through Read<sup>(1,2,4)</sup>



**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} \leq$  minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be  $t_{CO} + t_{CYC} + t_{CD1}$ ). If  $t_{CO} >$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be  $t_{CO} + t_{CD1}$ ).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>

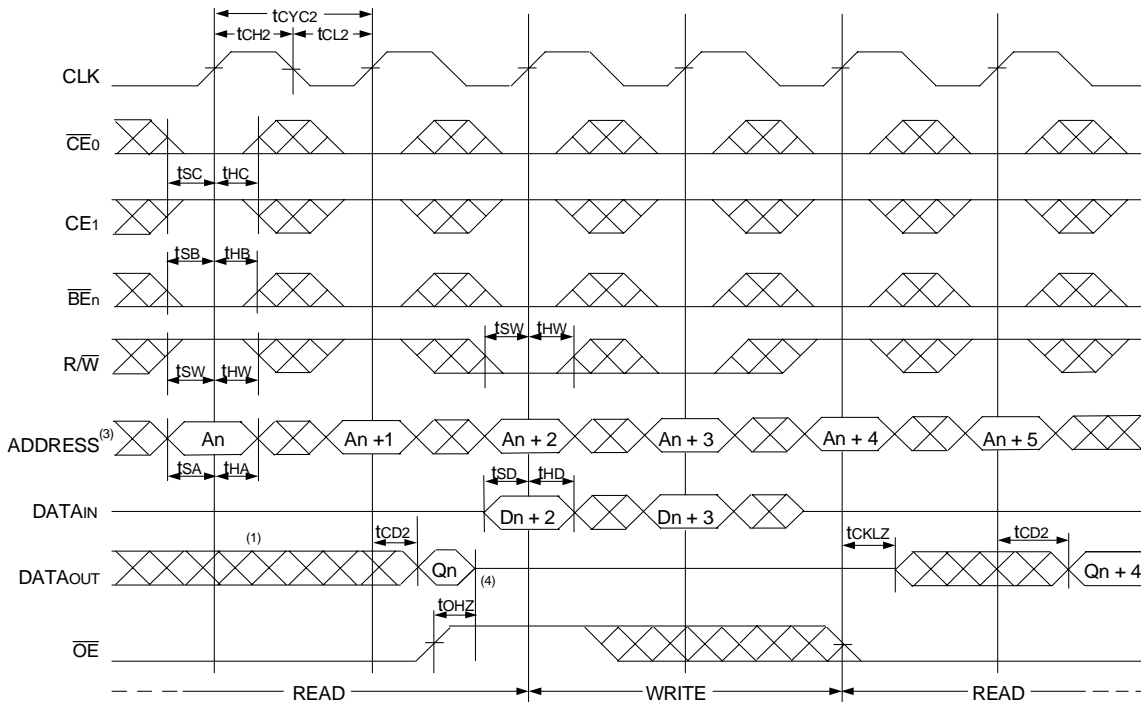


**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ . "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>

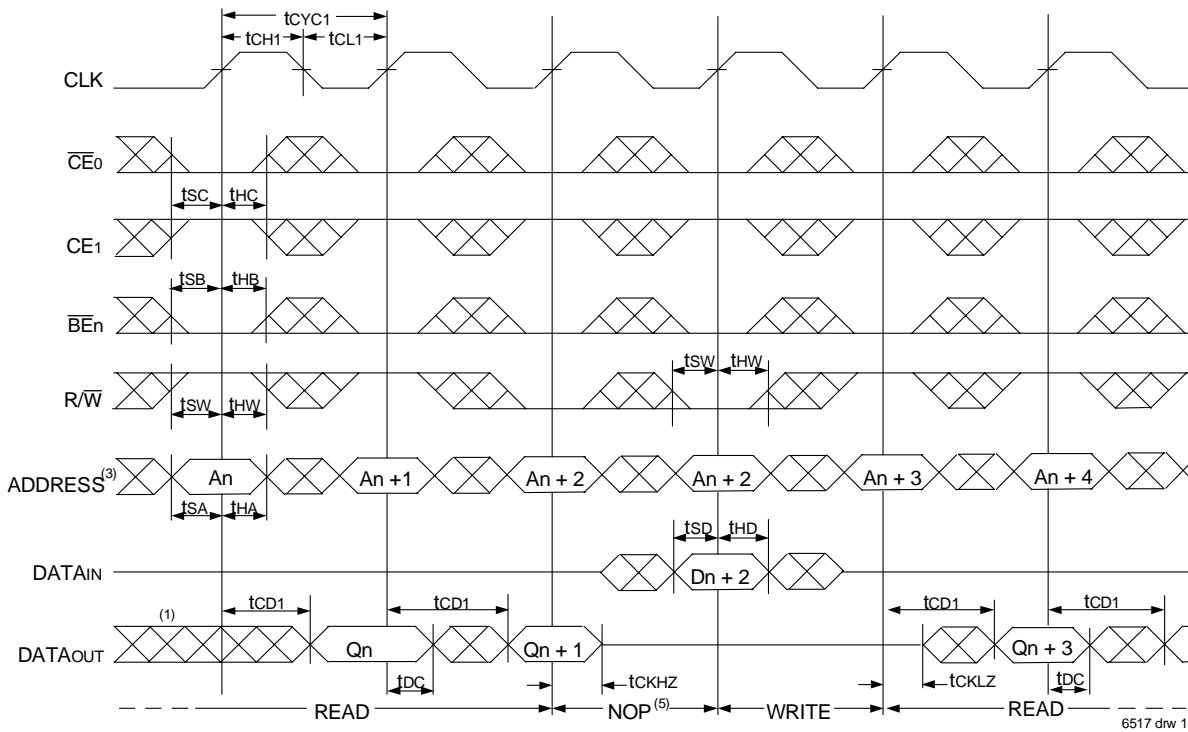


**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

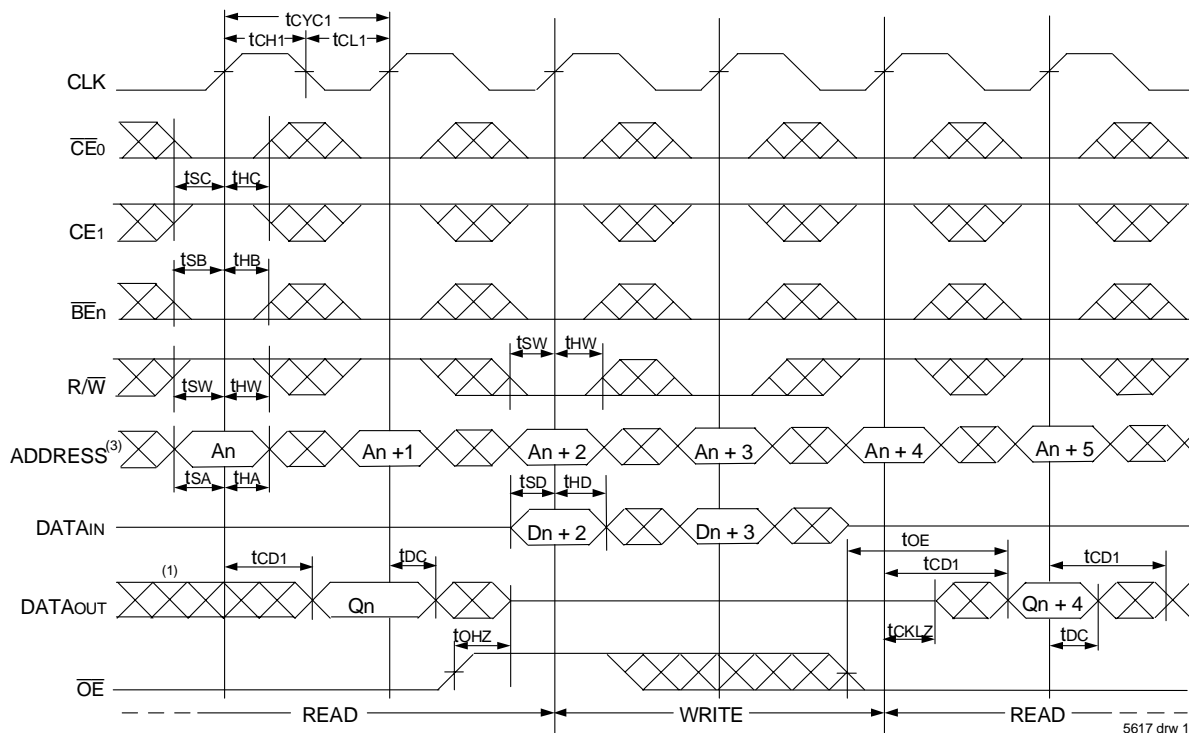
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### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>



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### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>



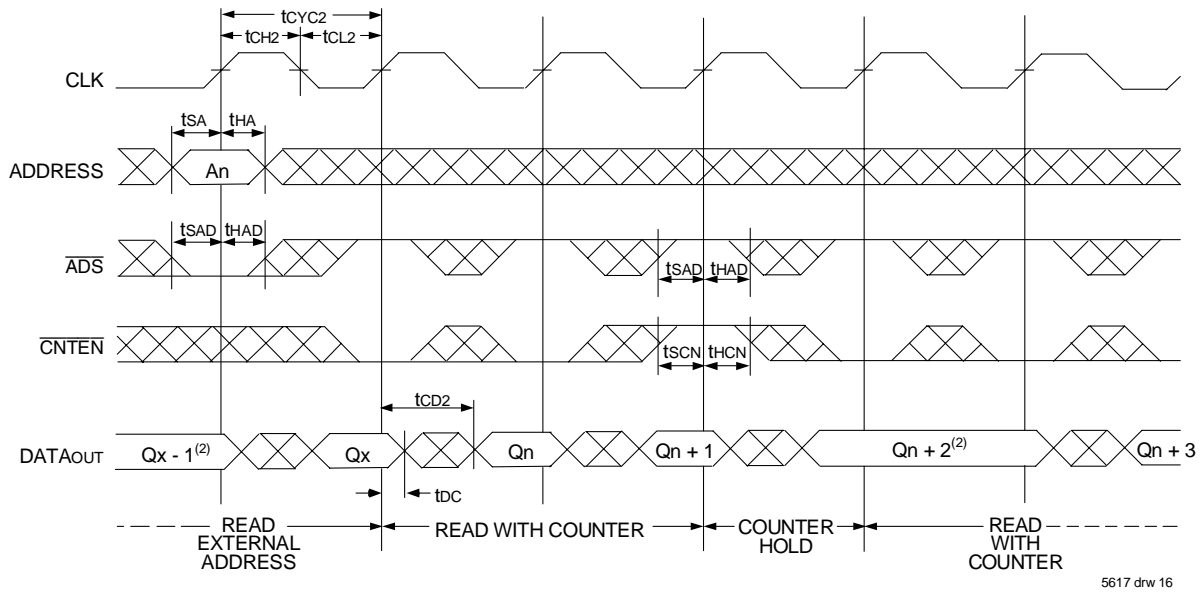
5617 drw 15

**NOTES:**

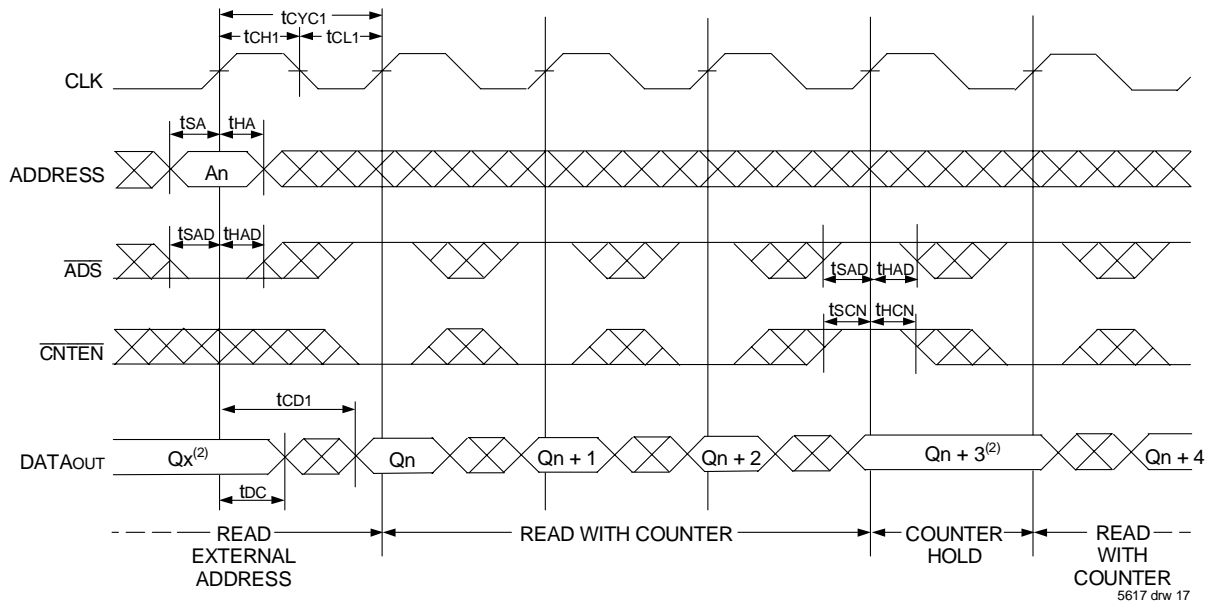
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE0}$ ,  $\overline{BEn}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.



### Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



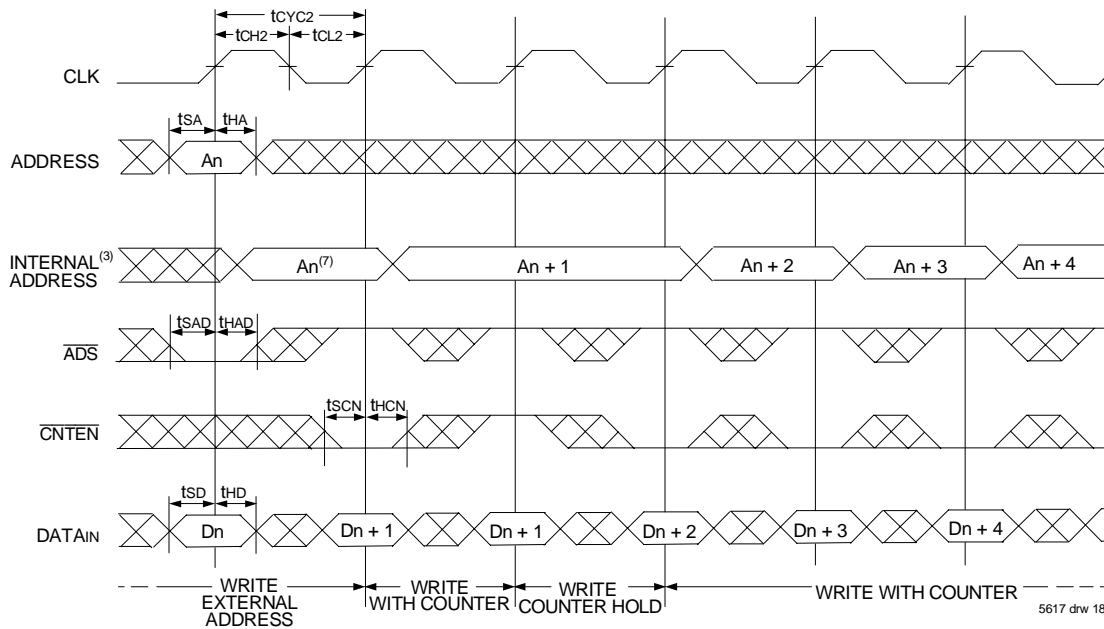
### Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>



**NOTES:**

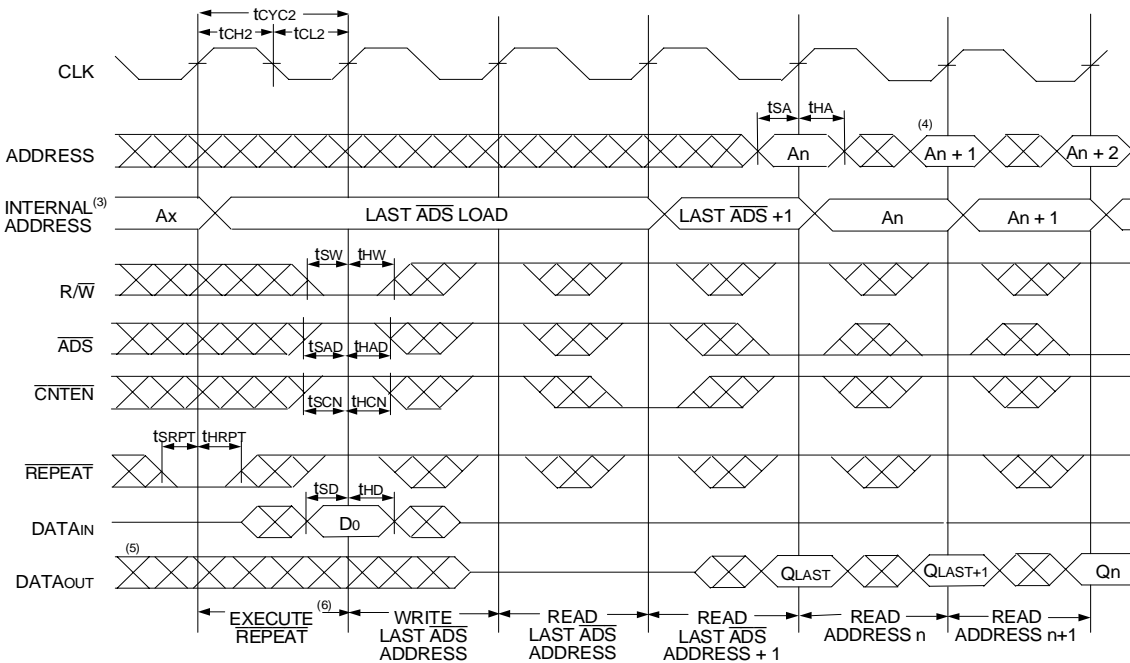
1.  $\overline{CE}_0$ ,  $\overline{OE}$ ,  $\overline{BE}_n = V_{IL}$ ;  $\overline{CE}_1$ ,  $R/\overline{W}$ , and  $\overline{REPEAT} = V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)<sup>(1)</sup>



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## Timing Waveform of Counter Repeat<sup>(2)</sup>



5617 drw 19

**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $R/\overline{W}$  =  $V_{IL}$ ;  $CE_1$  and  $\overline{REPEAT}$  =  $V_{IH}$ .
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$  =  $V_{IL}$ ;  $CE_1$  =  $V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during  $\overline{REPEAT}$  operation. A READ or WRITE cycle may be coincidental with the counter  $\overline{REPEAT}$  cycle: Address loaded by last valid  $\overline{ADS}$  load will be accessed. Extra cycles are shown here simply for clarification. For more information on  $\overline{REPEAT}$  function refer to Truth Table II.
7.  $CNTEN = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

### Functional Description

The IDT70V3599/89 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE0}$  or a LOW on CE1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3599/89s for depth expansion configurations. Two cycles are required with  $\overline{CE0}$  LOW and CE1 HIGH to re-activate the outputs.

### Depth and Width Expansion

The IDT70V3599/89 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3599/89 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

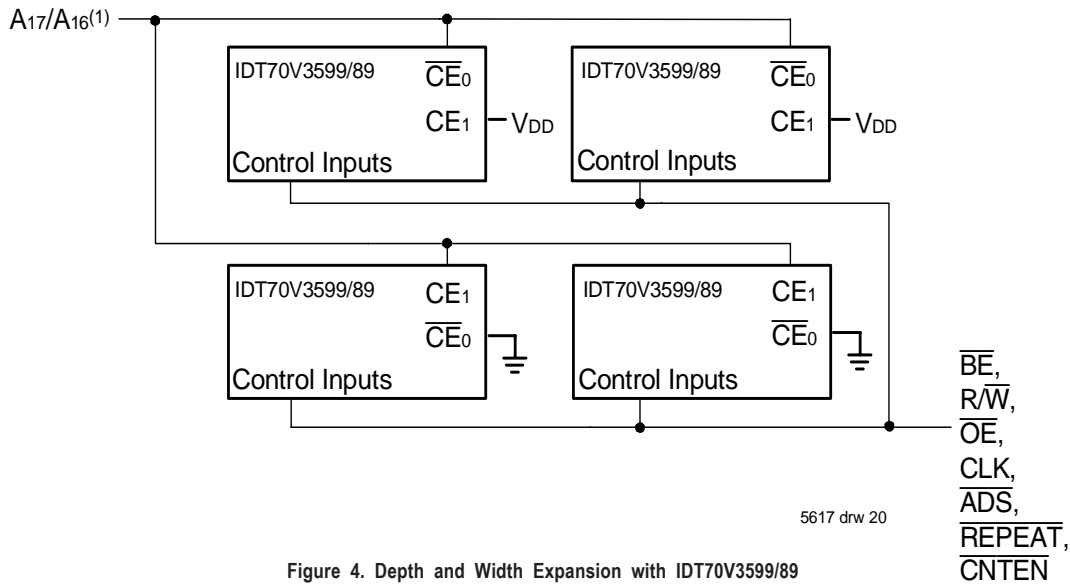


Figure 4. Depth and Width Expansion with IDT70V3599/89

**NOTE:**

- 1. A17 is for IDT70V3599, A16 is for IDT70V3589.

## JTAG Timing Specifications

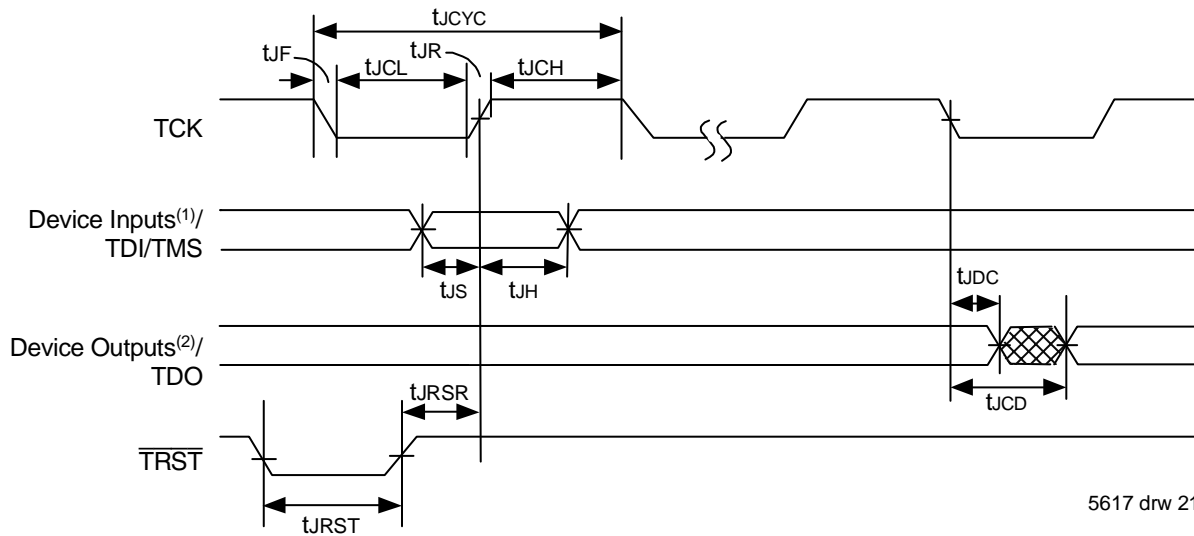


Figure 5. Standard JTAG Timing

**NOTES:**

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

## JTAG AC Electrical Characteristics<sup>(1,2,3,4)</sup>

Symbol	Parameter	70V3599/89		
		Min.	Max.	Units
t <sub>JCYC</sub>	JTAG Clock Input Period	100	—	ns
t <sub>JCH</sub>	JTAG Clock HIGH	40	—	ns
t <sub>JCL</sub>	JTAG Clock Low	40	—	ns
t <sub>JR</sub>	JTAG Clock Rise Time	—	3 <sup>(1)</sup>	ns
t <sub>JF</sub>	JTAG Clock Fall Time	—	3 <sup>(1)</sup>	ns
t <sub>JRST</sub>	JTAG Reset	50	—	ns
t <sub>JRSR</sub>	JTAG Reset Recovery	50	—	ns
t <sub>JCD</sub>	JTAG Data Output	—	25	ns
t <sub>JDC</sub>	JTAG Data Output Hold	0	—	ns
t <sub>JS</sub>	JTAG Setup	15	—	ns
t <sub>JH</sub>	JTAG Hold	15	—	ns

5617 tbl 12

**NOTES:**

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

## Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x0312 <sup>(1)</sup>	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

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### NOTE:

1. Device ID for IDT70V3589 is 0x0313.

## Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5617 tbl 14

## System Interface Parameters

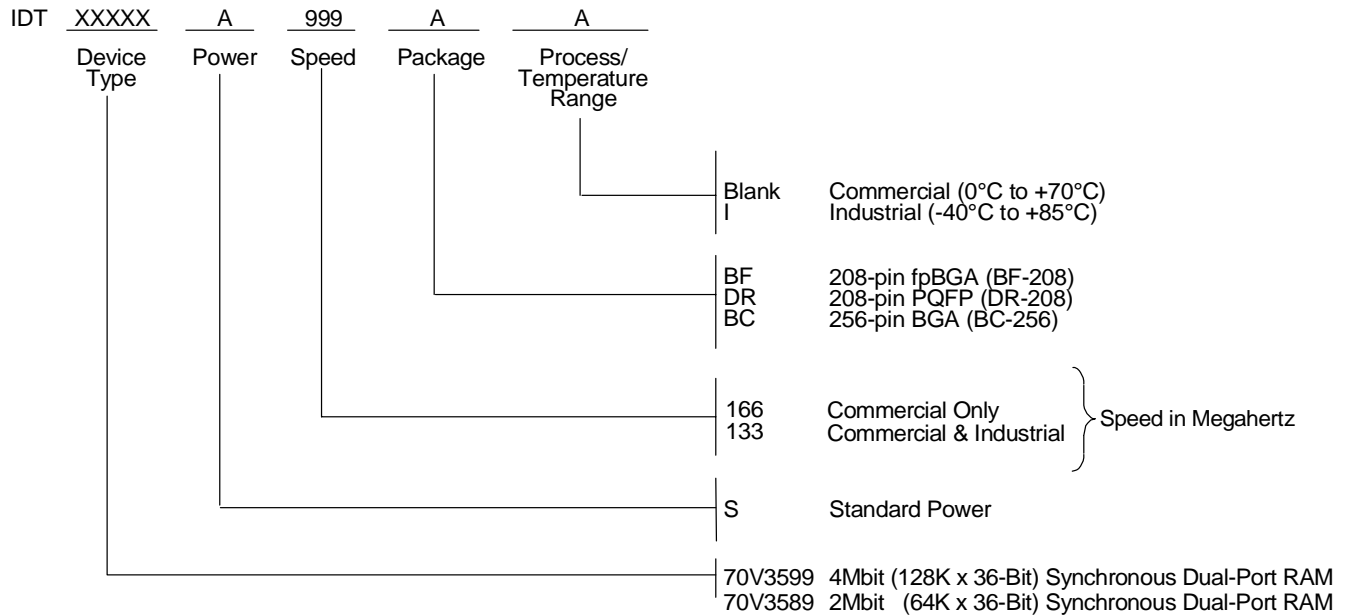
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs <sup>(1)</sup> . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0011	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs <sup>(2)</sup> to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5617 tbl 15

### NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and  $\overline{\text{TRST}}$ .
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website ([www.idt.com](http://www.idt.com)), or by contacting your local IDT sales representative.

## Ordering Information



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## IDT Clock Solution for IDT70V3599/89 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance	
70V3599/89	3.3/2.5	LVTTL	8pF	40%	166	75ps	IDT5V2528

5617 tbl16a

## Datasheet Document History:

6/2/00:	Initial Public Offering
7/12/00:	Added mux to functional block diagram
7/30/01:	Page 20 Changed maximum value for JTAG AC Electrical Characteristics for $t_{JCD}$ from 20ns to 25ns Page 9 Added Industrial Temperature DC Parameters
11/20/01:	Page 2, 3 & 4 Added date revision for pin configurations Page 11 Changed $t_{OE}$ value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05 Page 1 & 22 Replaced $\text{TM}$ logo with $\text{®}$ logo Page 10 Changed AC Test Conditions Input Rise/Fall Times
7/1/02:	Consolidated multiple devices into one datasheet Page 1 & 5 Added DCD capability for Pipelined Outputs Page 7 Clarified $T_{BIAS}$ and added $T_{JN}$ Page 9 Changed DC Electrical Parameters Page 11 Removed Clock Rise & Fall Time from AC Electrical Characteristics Table Removed Preliminary status
05/19/03:	Page 11 Added Byte Enable Setup Time & Byte Enable Hold Time to AC Electrical Characteristics Table Page 22 Added IDT Clock Solution Table


**CORPORATE HEADQUARTERS**

2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**

800-345-7015 or 408-727-5166  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**

831-754-4613  
DualPortHelp@idt.com

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