12-bit, 250kSPS Low-power ADCs with Single-ended and Differential Inputs and Multiple Input Channels

ISL26320, ISL26321, ISL26322, ISL26323, ISL26324, ISL26325, ISL26329

The ISL26320/21/22/23/24/25/29 family of sampling SAR-type ADCs feature excellent linearity over supply and temperature variations, and offer versions with 1-, 2-, 4- and 8-channel single-ended inputs, and 1-, 2- and 4-channel differential inputs.

A proprietary input multiplexer and combination buffer amplifier reduces the input drive requirements, resulting in lower cost and reduced board space. Specified measurement accuracy is maintained with input signals up to VDD.

Members of the ISL26320/21/22/23/24/25/29 family of Low-Power ADCs offer pinout intercompatibility, differing only in the analog inputs, to support quick replication of proven layouts across multiple design platforms.

The serial digital interface is SPI compatible and is easily interfaced to popular FPGAs and microcontrollers. Power consumption is limited to 15mW at a sampling rate of 250kSPS, and an operating current of just 8µA typical between conversions, when configured for Auto Powerdown mode.

The ISL26320/21/22/23/24/25/29 feature up to 5kV Human Body Model ESD survivability and are available in the popular SOIC and TSSOP packages. Performance is specified for operation over the full industrial temperature range (-40°C to +125°C).

Features

- Pin-compatible Family Allows Easy Design Upgrades
- Excellent Differential Non-Linearity (0.7LSB max)
- Low THD: -86dB (typ)
- Simple SPI-compatible Serial Digital Interface
- Low 3mA Operating Current
- Power-down Current between Conversions 8µA (typ)
- +5.25V to +2.7V Supply
- Excellent ESD Survivability: 5kV HBM, 350V MM, 2kV CDM

Applications

- Industrial Process Control
- Energy Measurement
- Multichannel Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

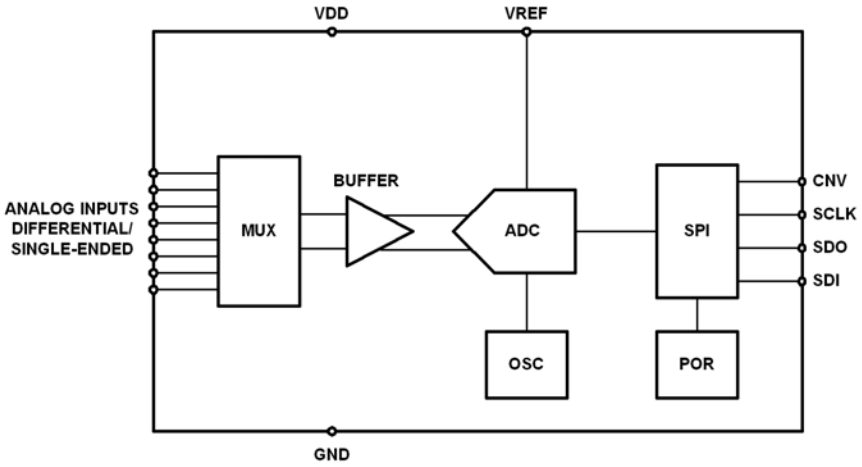
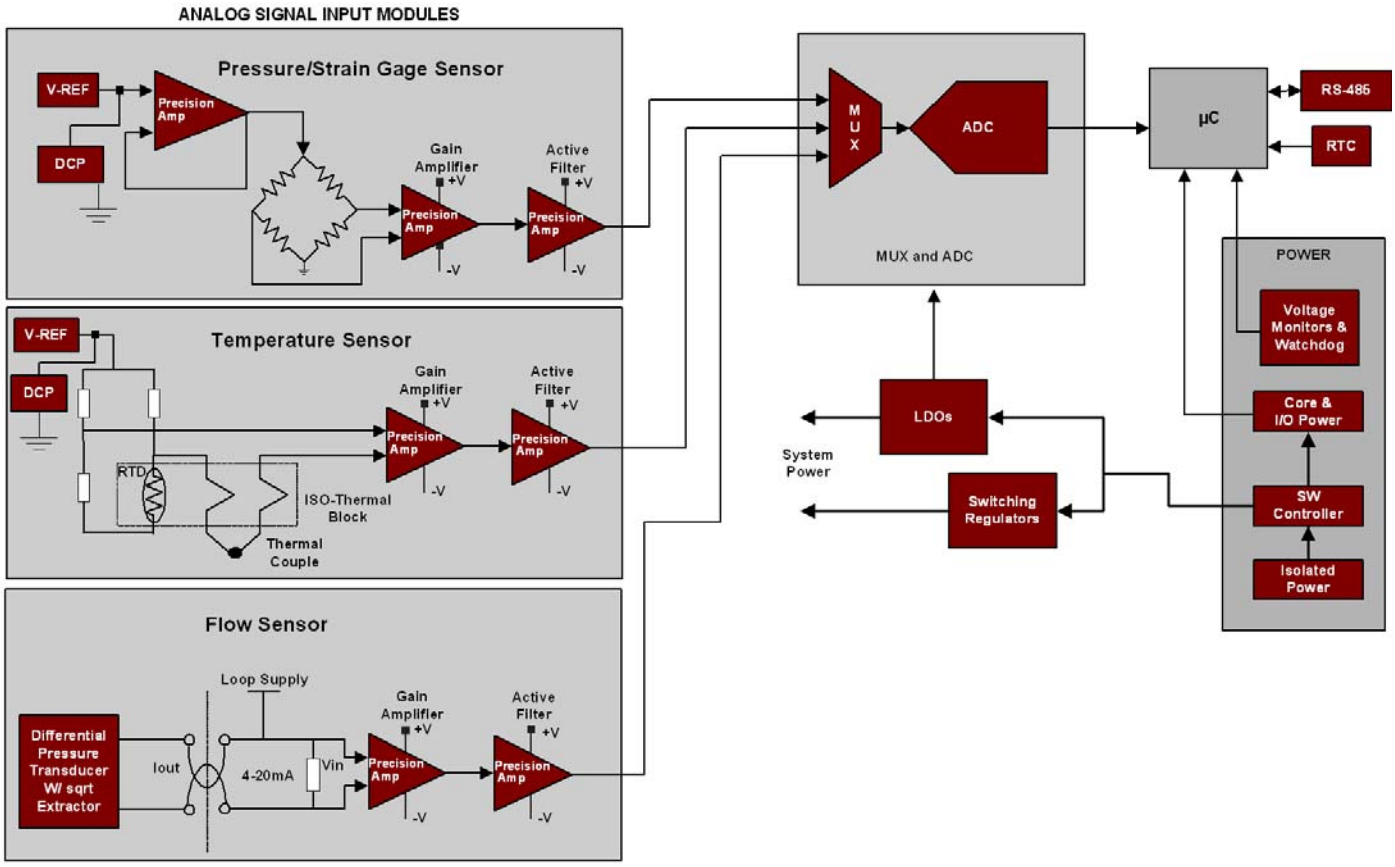


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Application Block Diagram



Pin-Compatible Family

MODEL	RESOLUTION (Bits)	SPEED (kHz)	ANALOG INPUT	INPUT CHANNELS
ISL26310	12	125	Differential	1
ISL26311	12	125	Single-Ended	1
ISL26312	12	125	Differential	2
ISL26313	12	125	Single-Ended	2
ISL26314	12	125	Differential	4
ISL26315	12	125	Single-Ended	4
ISL26319	12	125	Single-Ended	8
ISL26320	12	250	Differential	1
ISL26321	12	250	Single-Ended	1
ISL26322	12	250	Differential	2
ISL26323	12	250	Single-Ended	2
ISL26324	12	250	Differential	4
ISL26325	12	250	Single-Ended	4
ISL26329	12	250	Single-Ended	8

Ordering Information

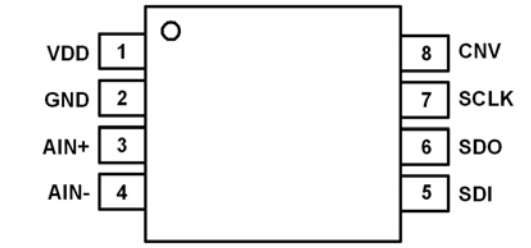
PART NUMBER (Notes 1, 2, 3)	PART MARKING	DESCRIPTION				TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG #
		RESOLUTION (Bits)	SPEED (kHz)	INPUT (SE/DIFF)	INPUT CHANNELS			
ISL26320FBZ	26320 FBZ	12	250	Diff	1	-40 to +125	8 Ld SOIC	M8.15
ISL26321FBZ	26321 FBZ	12	250	SE	1	-40 to +125	8 Ld SOIC	M8.15
ISL26322FVZ	26322 FVZ	12	250	Diff	2	-40 to +125	16 Ld TSSOP	M16.173
ISL26323FBZ	26323 FBZ	12	250	SE	2	-40 to +125	8 Ld SOIC	M8.15
ISL26324FVZ	26324 FVZ	12	250	Diff	4	-40 to +125	16 Ld TSSOP	M16.173
ISL26325FVZ	26325 FVZ	12	250	SE	4	-40 to +125	16 Ld TSSOP	M16.173
ISL26329FVZ	26329 FVZ	12	250	SE	8	-40 to +125	16 Ld TSSOP	M16.173

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL26320, ISL26321, ISL26322, ISL26323, ISL26324, ISL26325, ISL26329. For more information on MSL please see techbrief TB363.

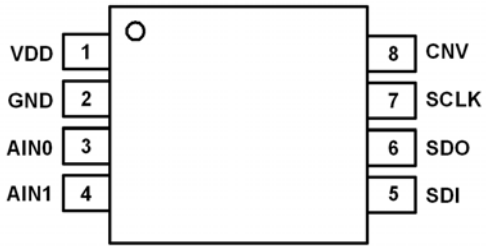
Pin Configurations

ISL26320
(8 LD SOIC)
TOP VIEW

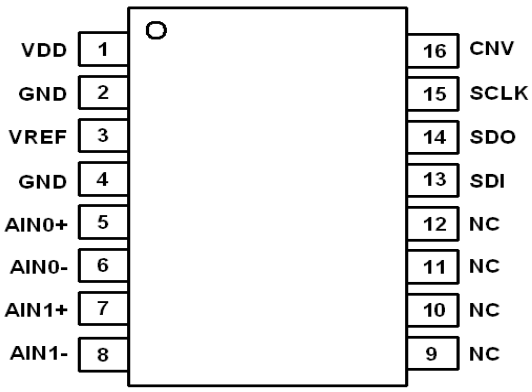


ISL26321
(8 LD SOIC)
TOP VIEW

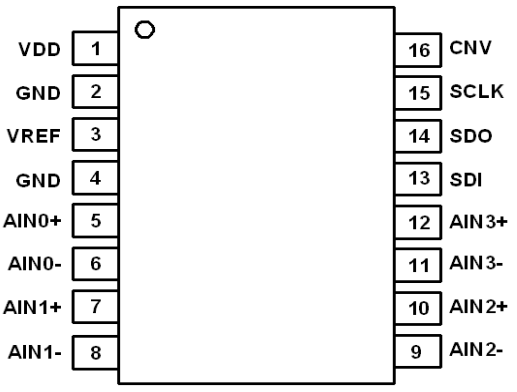
ISL26323
(8 LD SOIC)
TOP VIEW



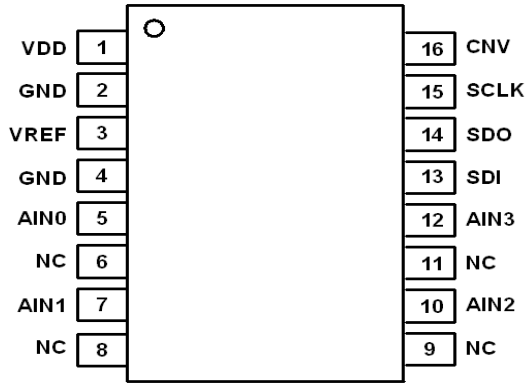
ISL26322
(16 LD TSSOP)
TOP VIEW



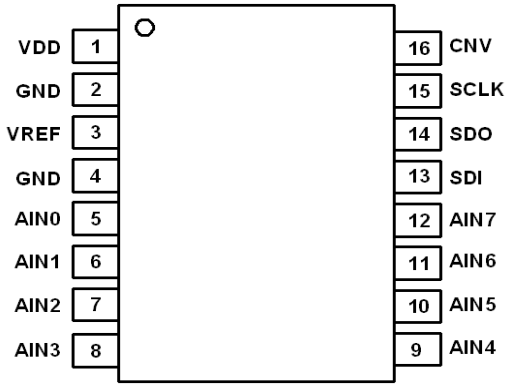
ISL26324
(16 LD TSSOP)
TOP VIEW



ISL26325
(16 LD TSSOP)
TOP VIEW



ISL26329
(16 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER							DESCRIPTION
	ISL26320	ISL26321	ISL26322	ISL26323	ISL26324	ISL26325	ISL26329	
VDD	1	1	1	1	1	1	1	Positive Supply Voltage
GND	2	2	2, 4	2	2, 4	2, 4	2, 4	Ground
VREF	-	3	3	-	3	3	3	Reference Voltage Input
AIN0+	-	-	5	-	5	-	-	Differential Analog Input, Positive
AIN0-	-	-	6	-	6	-	-	Differential Analog Input, Negative
AIN1+	-	-	7	-	7	-	-	Differential Analog Input, Positive
AIN1-	-	-	8	-	8	-	-	Differential Analog Input, Negative
AIN2+	-	-	-	-	10	-	-	Differential Analog Input, Positive
AIN2-	-	-	-	-	9	-	-	Differential Analog Input, Negative
AIN3+	-	-	-	-	12	-	-	Differential Analog Input, Positive
AIN3-	-	-	-	-	11	-	-	Differential Analog Input, Negative
AIN0	-	4	-	3	-	5	5	Single-Ended Analog Input
AIN1	-	-	-	4	-	7	6	Single-Ended Analog Input
AIN2	-	-	-	-	-	10	7	Single-Ended Analog Input
AIN3	-	-	-	-	-	12	8	Single-Ended Analog Input
AIN4	-	-	-	-	-	-	9	Single-Ended Analog Input
AIN5	-	-	-	-	-	-	10	Single-Ended Analog Input
AIN6	-	-	-	-	-	-	11	Single-Ended Analog Input
AIN7	-	-	-	-	-	-	12	Single-Ended Analog Input
SDI	5	5	13	5	13	13	13	Serial Interface Data Input
SDO	6	6	14	6	14	14	14	Serial Interface Data Output
SCLK	7	7	15	7	15	15	15	Serial Interface Clock Input
CNV	8	8	16	8	16	16	16	Conversion Control Input
NC	-	-	9, 10, 11, 12	-	-	6, 8, 9, 11	-	No Connect
AIN+	3	-	-	-	-	-	-	Differential Analog Input, Positive
AIN-	4	-	-	-	-	-	-	Differential Analog Input, Negative

Absolute Maximum Ratings

AIN+, AIN-, VREF . . . . . GND-0.3 to V_{DD}+0.3V
Digital Inputs . . . . . GND-0.3 to V_{DD}+0.3V
VDD . . . . . -0.3 to 6V
GND . . . . . GND-0.3 to +0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 5000V
Machine Model (Per JESD22-A115) 350V
Charged Device Model (Per JESD22-C101) 2000V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (Notes 4, 5)	98	48
16 Ld TSSOP (Notes 4, 5)	92	29

Maximum Power Dissipation 80mW
Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +125°C
V_{DD} to GND . . . . . 2.7V to +5.25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

VREF = VDD V, VDD = 2.7V to 5V, V_{CM} = VDD/2, SCLK = 20MHz and T_A = -40°C to +125°C (typical performance at +25°C), unless otherwise specified. Boldface limits apply over the operating temperature range, -40°C to +125°C.

SYMBOL	PARAMETER	TEST LEVEL OR NOTES	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
ANALOG INPUTS						
	Number of Input Channels	ISL26320, ISL26321		1		
		ISL26322		2		
		ISL26323		2		
		ISL26324, ISL26325		4		
		ISL26329		8		
	Input Voltage Range	Differential Inputs (AINX+ - AINX-) is $-V_{REF}$ (Min) and $+V_{REF}$ (Max)	0		V_{REF}	V
		AINX, Single-Ended Inputs	0		V_{REF}	V
	Common Mode Input Voltage Range	Differential Inputs	$V_{REF}/2 - 0.2$	$V_{REF/2}$	$V_{REF}/2 + 0.2$	V
	Average Input Current			2.5		µA
C_{IN}	Input Capacitance			4		pF
	Channel-Channel Crosstalk	f_{IN} = 100kHz V_{IN} = FS, other channels = 0V		-86		dB
VOLTAGE REFERENCE						
V_{REFEX}	External Reference Input Voltage Range		2	2.5	V_{DD}	V
I_{REFIN}	Average Input Current			200	220	µA
C_{REFIN}	Effective Input Capacitance			10		pF
DC ACCURACY						
	Resolution (No Missing Codes)		12			Bits
DNL	Differential Nonlinearity Error		-0.7		+0.7	LSB
INL	Integral Nonlinearity Error		-0.7		+0.7	LSB
	Gain Error		-6		6	LSB
	Gain Error Matching		-2		2	LSB
	Offset Error		-6		6	LSB

Electrical Specifications VREF = VDD V, VDD = 2.7V to 5V, V_{CM} = VDD/2, SCLK = 20MHz and T_A = -40°C to +125°C (typical performance at +25°C), unless otherwise specified. Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)

SYMBOL	PARAMETER	TEST LEVEL OR NOTES	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
	Offset Error Matching		-2		2	LSB
PSRR	Power Supply Rejection Ratio			70		dB
DYNAMIC PERFORMANCE						
SNR	Signal-to-Noise Notes: V_{IN} = FS-0.1dB, f_{IN} = 10kHz	Differential Inputs		73.4		dB
		Single-Ended Inputs		73.4		dB
SINAD	Signal-to-Noise + Distortion Notes: V_{IN} = FS-0.1dB, f_{IN} = 10kHz	Differential Inputs		73.1		dB
		Single-Ended Inputs		73.1		dB
THD	Total Harmonic Distortion Notes: V_{IN} = FS-0.1dB, f_{IN} = 10kHz	Differential Inputs		-86		dB
		Single-Ended Inputs		-86		dB
SFDR	Spurious-free Dynamic Range Notes: V_{IN} = FS-0.1dB	f_{IN} = 20kHz		96		dB
BW	-3dB Input Bandwidth			2.5		MHz
t_{AD}	Sampling Aperture Delay			12		ns
t_{jit}	Sampling Aperture Jitter			25		ps
POWER SUPPLY REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.25	V
I_{DD}	Supply Current			3	3.5	mA
PD	Power Consumption	Normal Operation		15	17.5	mW
IPD	Power-down Current	Auto Power-Down Mode		8	50	µA
Istby	Standby Mode Current	Auto Sleep Mode		0.4		mA
DIGITAL INPUTS						
V_{IH}			0.7 VDD			V
V_{IL}					0.2 V_{DD}	V
V_{OH}	I_{OH} = -1mA		VDD-0.4			V
V_{OL}	I_{OL} = 1mA				0.2 V_{DD}	V
I_{IH}, I_{IL}	Input Leakage Current		-100		100	nA
	Serial Clock Frequency				20	MHz
TIMING SPECIFICATIONS (Note 7)						
t_{SCLK}	SCLK Period (in RAC Mode)		50			ns
t_{SCLK}	SCLK Period (in RSC, RDC Modes)		50		100	ns
t_{DATA}	Safe Data Transfer Time After Conversion State Begins				1.6	µs
t_{CSB_SCLK}	CSB Falling Low to SCLK Rising Edge		40			ns
t_{SDI_SU}	SDI Setup Time with Respect to Positive Edge of SCLK		10			ns
t_{SDI_H}	SDI Hold Time with Respect to Positive Edge of SCLK		10			ns
t_{SDO_V}	SDOUT Valid Time with Respect to Negative Edge of SCLK				25	ns
t_{SDOZ_D}	SDOUT to High Impedance State After CNV Rising Edge (or last SCLK falling edge)	Note 8		85		ns
t_{ACQ}	Acquisition Time when Fully Powered Up		400			ns

Electrical Specifications VREF = VDD V, VDD = 2.7V to 5V, V_{CM} = VDD/2, SCLK = 20MHz and T_A = -40°C to +125°C (typical performance at +25°C), unless otherwise specified. Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)

SYMBOL	PARAMETER	TEST LEVEL OR NOTES	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{ACQ}	Acquisition Time in Auto Sleep Mode		1.7			µs
t_{ACQ}	Acquisition time in Auto Power Down Mode		150			µs
t_{SCLKH}	SCLK High Time		20			ns
t_{SCLKL}	SCLK Low Time		20			ns
t_{CNV}	CNV Pulse Width		100			ns

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. The device may become nonresponsive if the minimum acquisition times are not met in their respective modes, requiring a power cycle to restore normal operation.
8. Transition time to high impedance state is dominated by RC loading on the SDOUT pin. Specified value is measured using equivalent loading shown in Figure 2.

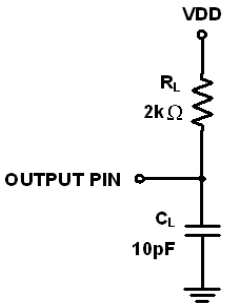


FIGURE 2. EQUIVALENT LOAD CIRCUIT FOR DIGITAL OUTPUT TESTING

Typical Performance Characteristics

$T_A = +25°C$, $V_{DD} = 5V$, $V_{REF} = 5V$, $f_{SAMPLE} = 250kHz$, $f_{SCLK} = 20MHz$, unless otherwise specified.

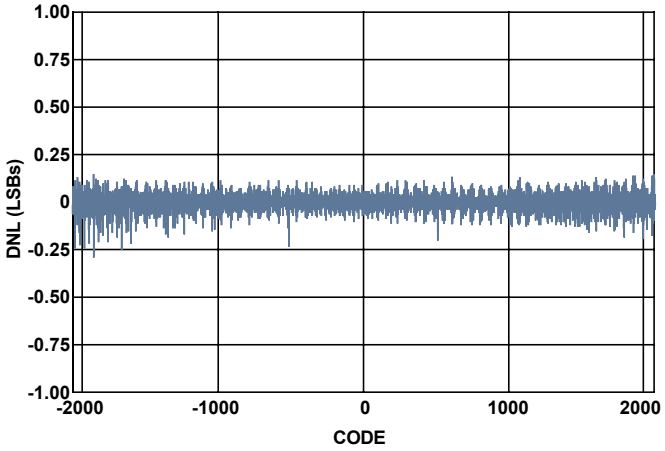


FIGURE 3. DIFFERENTIAL NONLINEARITY (DNL) vs CODE

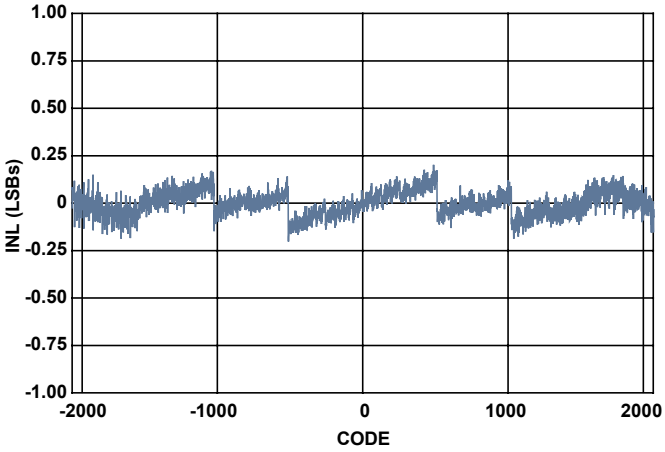


FIGURE 4. INTEGRAL NONLINEARITY (INL) vs CODE

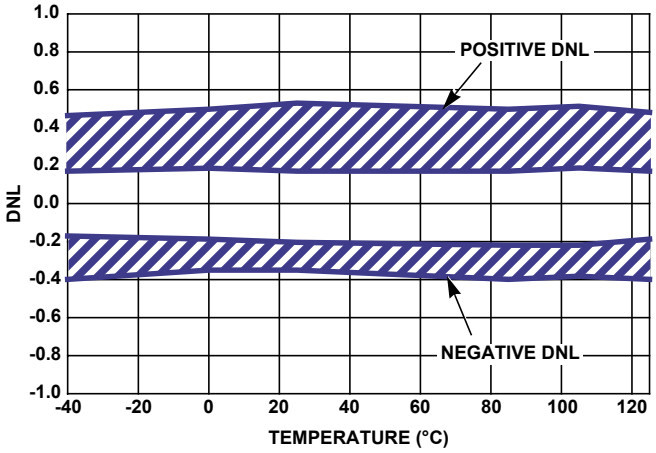


FIGURE 5. DNL DISTRIBUTION vs TEMPERATURE

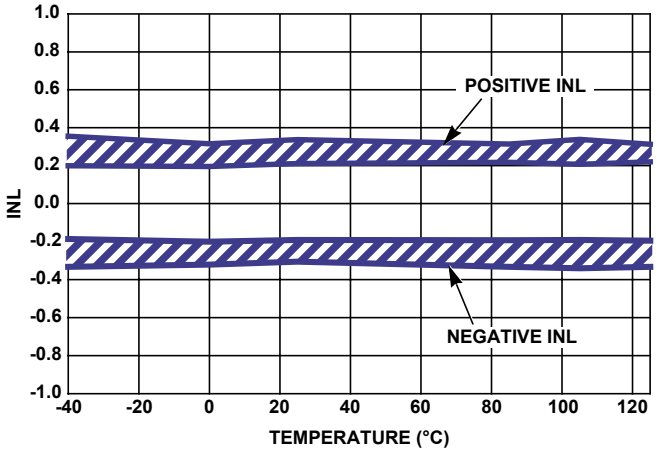


FIGURE 6. INL DISTRIBUTION vs TEMPERATURE

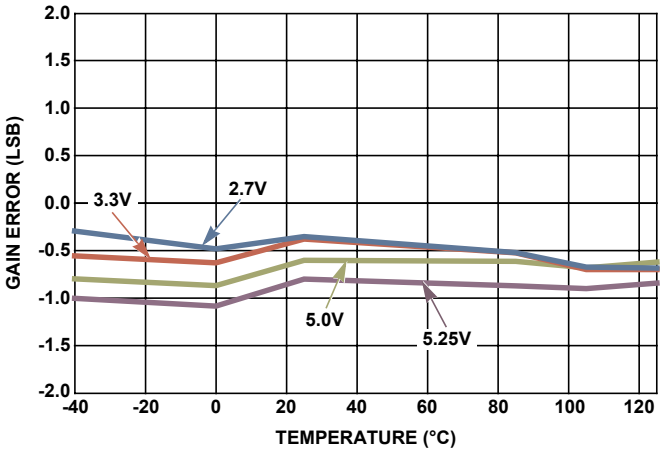


FIGURE 7. GAIN ERROR vs SUPPLY VOLTAGE AND TEMPERATURE

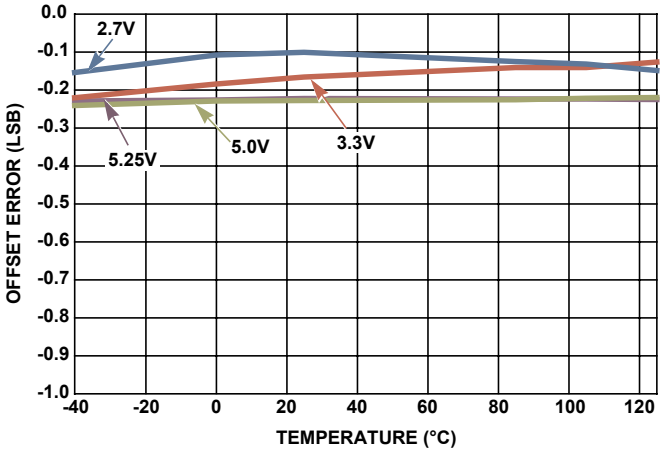


FIGURE 8. OFFSET ERROR vs SUPPLY VOLTAGE AND TEMPERATURE

Typical Performance Characteristics

$T_A = +25°C$, $V_{DD} = 5V$, $V_{REF} = 5V$, $f_{SAMPLE} = 250kHz$, $f_{SCLK} = 20MHz$, unless otherwise specified. (Continued)

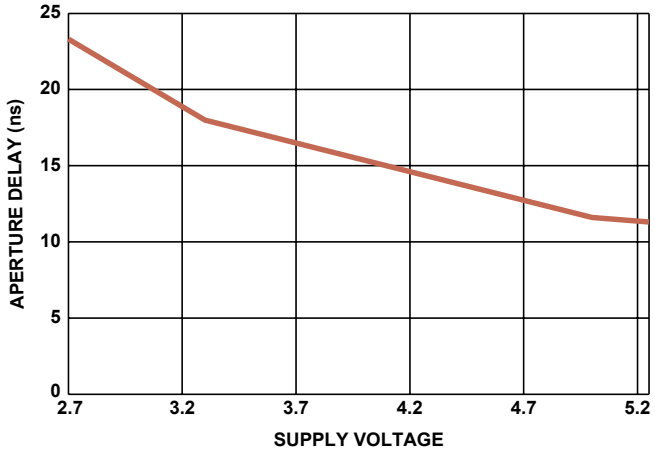


FIGURE 9. APERTURE DELAY vs SUPPLY VOLTAGE

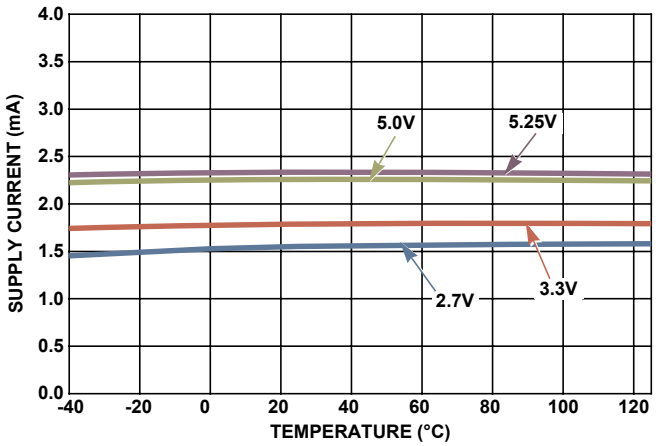


FIGURE 10. SUPPLY CURRENT vs VOLTAGE AND TEMPERATURE

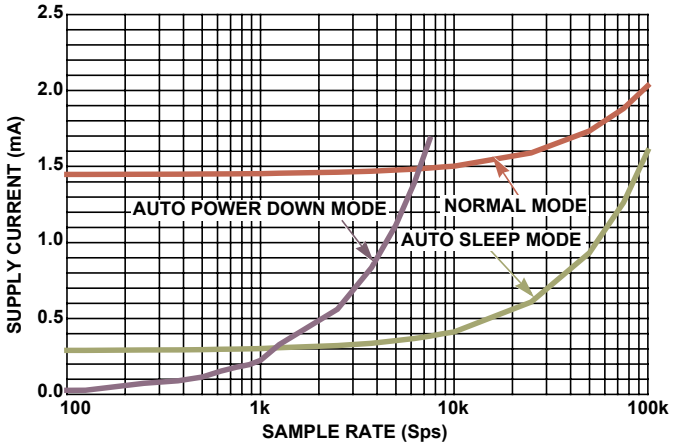


FIGURE 11. SUPPLY CURRENT vs SAMPLING RATE (V_{DD} = 5V)

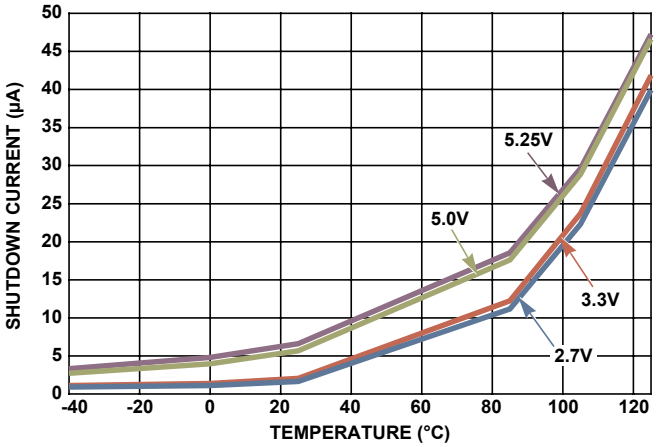


FIGURE 12. SHUTDOWN CURRENTS vs VOLTAGE AND TEMPERATURE

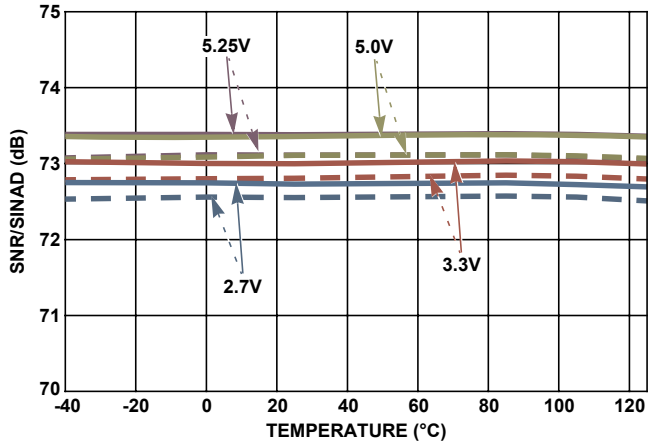


FIGURE 13. SNR AND SINAD vs SUPPLY VOLTAGE AND TEMPERATURE

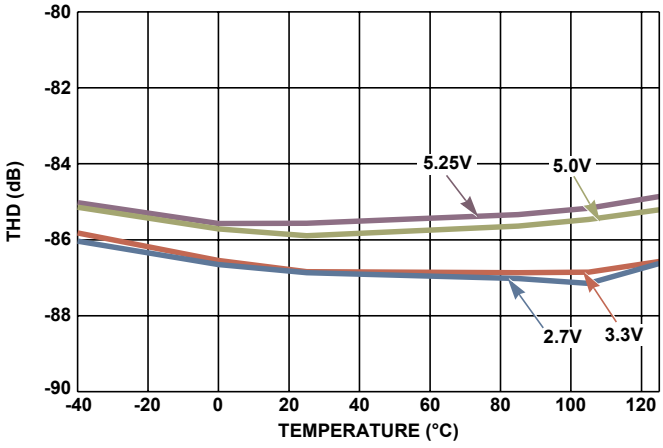


FIGURE 14. THD vs SUPPLY VOLTAGE AND TEMPERATURE

Typical Performance Characteristics

$T_A = +25°C$, $V_{DD} = 5V$, $V_{REF} = 5V$, $f_{SAMPLE} = 250kHz$, $f_{SCLK} = 20MHz$, unless otherwise specified. (Continued)

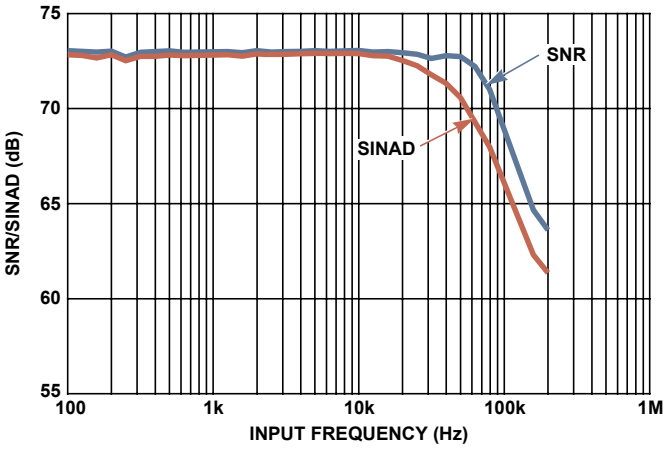


FIGURE 15. SNR AND SINAD vs INPUT FREQUENCY

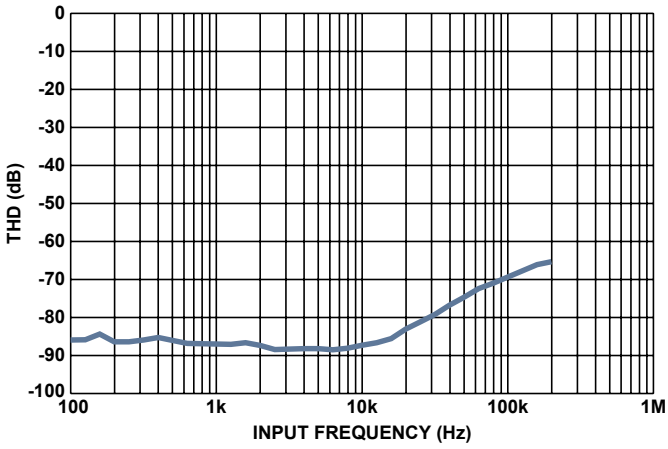


FIGURE 16. THD vs INPUT FREQUENCY

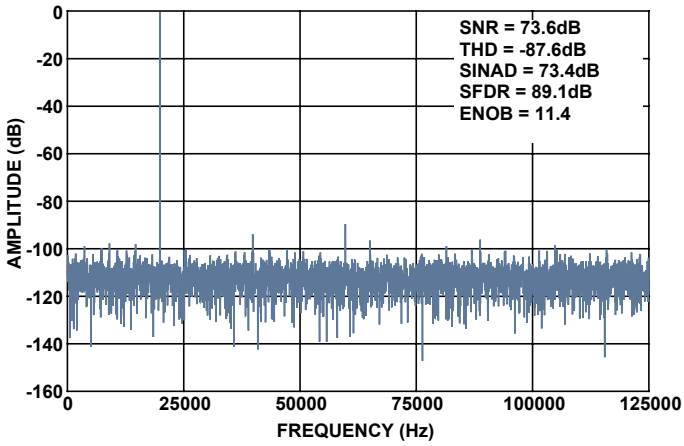


FIGURE 17. SINGLE-TONE FFT

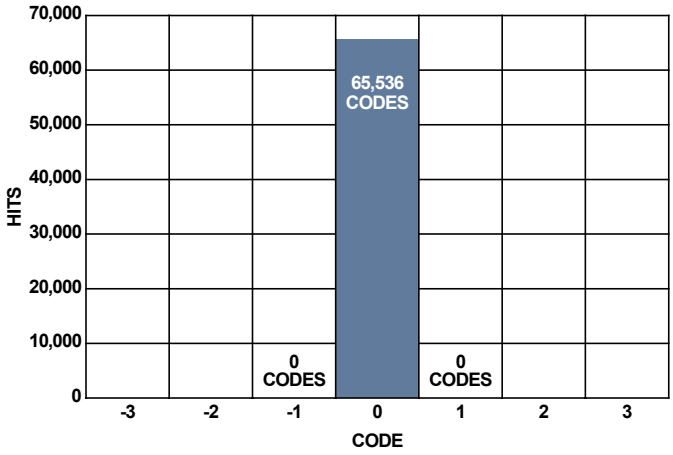


FIGURE 18. SHORTED INPUT HISTOGRAM

Circuit Description

The ISL26320/21/22/23/24/25/29 family of 12-bit ADCs are low-power Successive Approximation-type (SAR) ADCs with 1-, 2-, 4-, or 8-channels and a choice of single-ended or differential inputs. The high-impedance buffered input simplifies interfacing to sensors and external circuitry.

The entire ISL26320/21/22/23/24/25/29 family follows the same base pinout and differs only in the analog input pins, allowing the user to replicate the basic board layout across multiple platforms with a minimum redesign effort.

The simple serial digital interface is compatible with popular FPGAs and microcontrollers and allows direct conversion control by the CNV pin.

Functional Description

The ISL26320/21/22/23/24/25/29 devices are SAR (Successive Approximation Register) analog-to-digital converters that use capacitor-based charge redistribution as their conversion method.

These devices include an on-chip power-on reset (POR) circuit to initialize the internal digital logic when power is applied. An on-chip oscillator provides the master clock for the conversion logic. The CNV signal controls when the converter enters into its signal acquisition time (CNV = 0), and when it begins the conversion sequence after the signal has been captured (CNV = 1). The converters include a configuration register that can be accessed via the serial port. The configuration register has various bits to indicate which channel (where applicable) is selected, to activate the auto-power-down feature where the ADC is shut down between conversions, or to output the configuration register contents along with the data conversion word whenever a conversion word is read from the serial port. The serial port supports three different modes of reading the conversion data. These will be discussed later in this data sheet.

Figures 19 and 20 illustrate simplified representations of the converter analog section for differential and single-ended inputs, respectively. During the acquisition phase (CNV = 0) the input signal is presented to the Cs samples capacitors. To properly sample the signal, the CNV signal must remain low for the specified time. When CNV is taken high (CNV = 1), the switches that connect the sampling capacitors to the input are opened and the control logic begins the successive approximation sequence to convert the captured signal into a digital word. The conversion sequence timing is determined by the on-chip oscillator.

ADC Transfer Function

The ISL26320, the ISL26322, and the ISL26324 feature differential inputs with output data coding in two's complement format (see Table 1). The size of one LSB in these devices is (2*VREF)/4096. Figure 21 illustrates the ideal transfer function for these devices.

The ISL26321, ISL26323, ISL26325, and ISL26329 feature single-ended inputs with output coding in binary format (see Table 2). The size of one LSB in these devices is VREF/4096. Figure 22 illustrates the ideal transfer function for these devices.

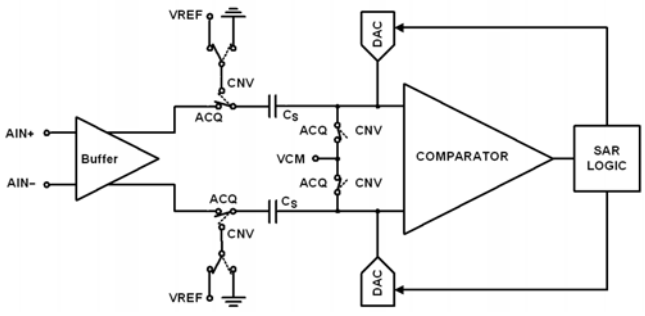


FIGURE 19. ARCHITECTURAL BLOCK DIAGRAM, DIFFERENTIAL INPUT

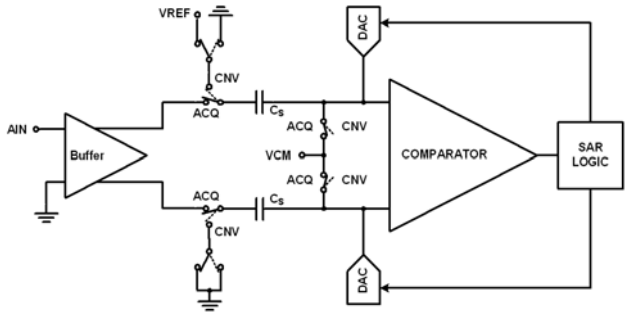


FIGURE 20. ARCHITECTURAL BLOCK DIAGRAM, SINGLE-ENDED

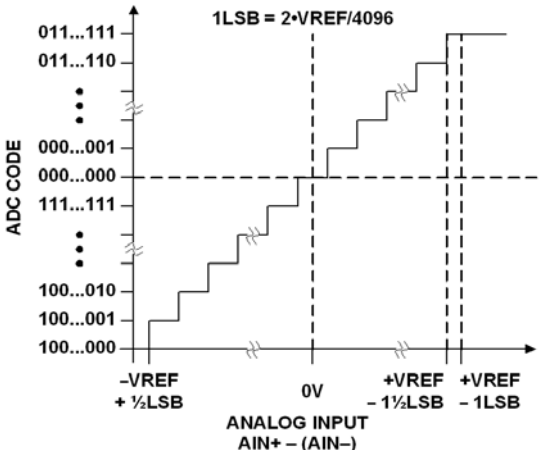


FIGURE 21. IDEAL TRANSFER CHARACTERISTICS, DIFFERENTIAL INPUT

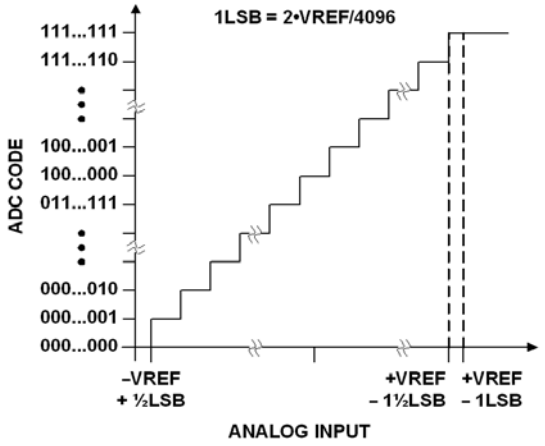


FIGURE 22. IDEAL TRANSFER CHARACTERISTICS, SINGLE-ENDED INPUT

Analog Inputs

Some members of the ISL26320/21/22/23/24/25/29 family feature a fully differential input with a nominal full-scale range equal to twice the applied VREF voltage. Those devices with differential inputs have a nominal full scale range equal to twice the applied VREF voltage. Each input swings VREF volts (peak-to-peak), 180° out of phase from one another for a total differential input of 2*VREF (refer to Figures 23 and 24).

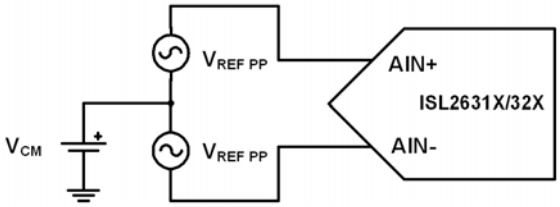


FIGURE 23. DIFFERENTIAL INPUT SIGNALING

Differential signaling offers several benefits over a single-ended input, such as:

- Doubling of the full-scale input range (and therefore the dynamic range)
- Improved even order harmonic distortion
- Better noise immunity due to common mode rejection

Figure 24 shows the relationship between the reference voltage and the full-scale differential input range for two different values of VREF. Note that the common-mode input voltage must be maintained within ±200mV of VREF/2 for differential inputs.

Those devices with singled-ended inputs have a ground-referenced peak-to-peak input voltage span equal to the reference voltage.

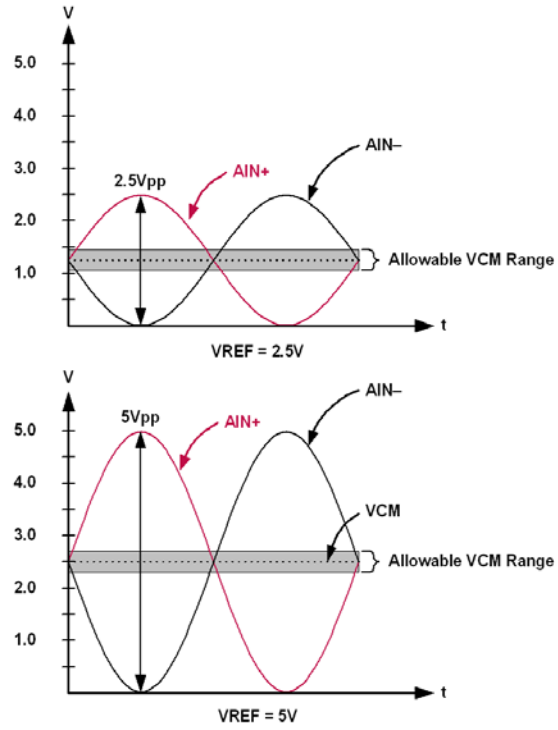


FIGURE 24. RELATIONSHIP BETWEEN VREF AND FULL-SCALE RANGE FOR DIFFERENTIAL INPUTS

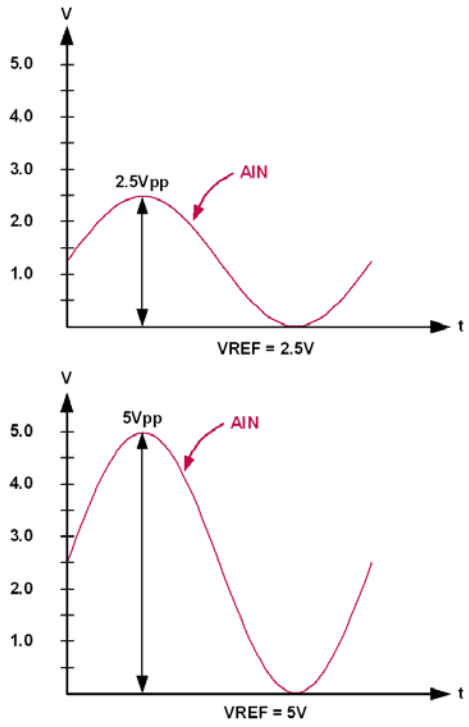


FIGURE 25. RELATIONSHIP BETWEEN VREF AND FULL-SCALE RANGE FOR SINGLE-ENDED INPUTS

Input Multiplexer

The input of the multiplexer connects the selected analog input pins to the ADC input. A proprietary sampling circuit significantly reduces the input drive requirements, resulting in lower overall cost and board space in addition to improved performance. Note that the input capacitance is only 2-3pF during the Sampling phase, changing to 40pF during the Settling phase, resulting in an average input current of 2.5µA and an effective input capacitance of only 4pF. See Figure 26.

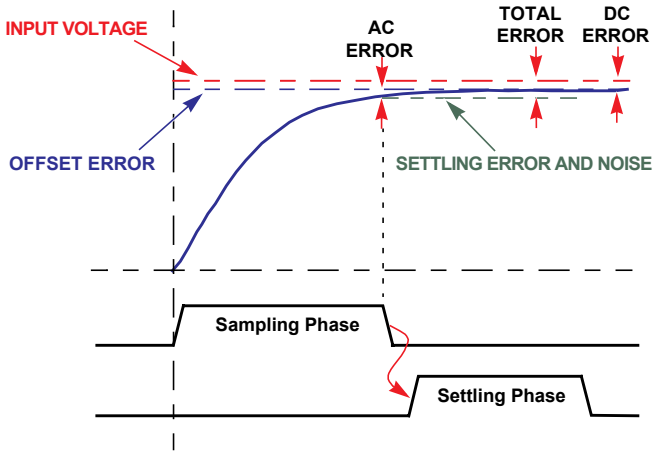


FIGURE 26. INPUT SAMPLING OPERATION

Voltage Reference Input

An external reference voltage must be supplied to the VREF pin to set the full-scale input range of the converter. The VREF input on these devices can accept voltages ranging from 2V (nominal) to VDD, however, they are specified with VREF at a voltage of 5V with VDD at 5V. Note that exceeding VDD by more than 100mV can forward bias the ESD protection diodes and degrade measurement accuracy due to leakage current. A lower value voltage reference must be used if the device is operated with VDD at voltages lower than 5V. If the VREF pin is tied to the VDD pin, the VREF pin should be decoupled with a local 1µF ceramic capacitor as described in a later paragraph.

Figures 27 and 28 illustrate possible voltage reference options for these ADCs. Figure 27 uses the precision ISL21090 voltage reference, which exhibits exceptionally low drift and low noise. The ISL21090 must be powered from a supply greater than 4.7V.

Figure 28 illustrates the ISL21010 voltage reference used with these ADCs. The ISL21010 series voltage references have higher noise and drift than the ISL21090 devices, but operate at lower supply voltages. Therefore, these devices can readily be used when these SAR ADCs operate with VDD at voltages less than 5V.

The outputs of ISL21090 or the ISL21010 devices should be decoupled with a 1µF ceramic capacitor. A 1µF, 6.3 V, X7R, 0603 (1608 metric) MLCC type capacitor is recommended for its high frequency performance. The trace length from the VREF pin to this capacitor and the voltage reference output should be as short as possible.

The ISL26320 and ISL26323 devices (packaged in 8 pin SOIC packages) derive their voltage reference from the VDD pin. To achieve best performance, the VDD pin of these devices should be bypassed with the 1µF ceramic capacitor mentioned above.

Power-Down/Standby Modes

In order to reduce power consumption between conversions, a number of user-selectable modes can be utilized by setting the appropriate bits in the Configuration Register.

Auto Power-down (PD0 = 0) reduces power consumption by shutting down all portions of the device except the oscillator and digital interface after completion of a conversion. There is a short recovery period after CNV is asserted Low (150µs with external reference).

In Auto Sleep mode (PD1 = 1), the device will automatically enter the low-power Sleep mode at the end of the current conversion. Recovery from this mode involves only 2.1µs and may offer an alternative to Power-down mode in some applications.

Output Data Format

The converter output word is delivered in two's complement format in differential input mode, and straight binary in single-ended input mode of operation respectively, all MSB-first. Input exceeding the specified full-scale voltage results in a clipped output which will not return to in-range values until after the input signal has returned to the specified allowable voltage range.

Data must be read prior to the completion of the current conversion to avoid conflict and loss of data, due to overwriting of the new conversion data into the output register.

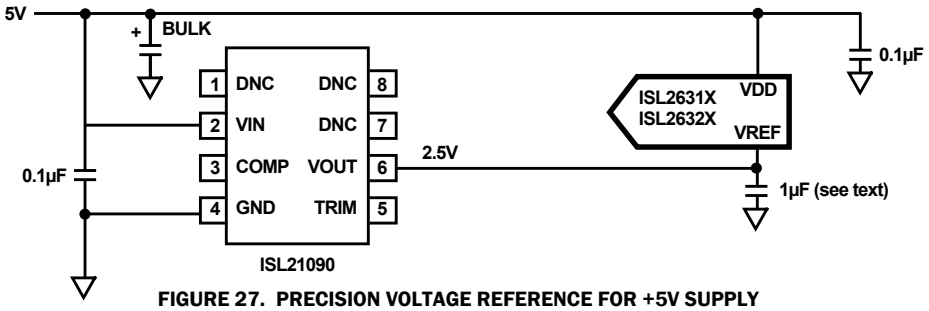


FIGURE 27. PRECISION VOLTAGE REFERENCE FOR +5V SUPPLY

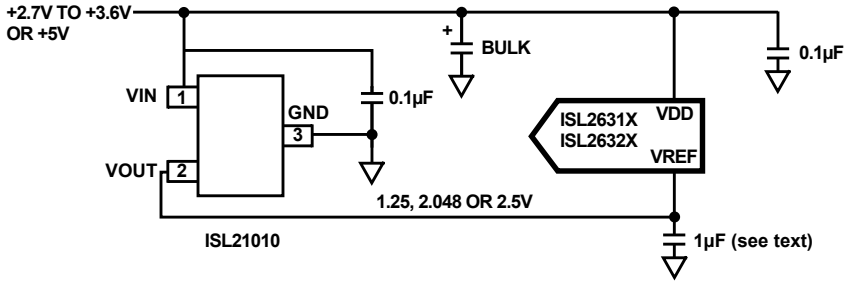


FIGURE 28. VOLTAGE REFERENCE FOR +2.7V TO +3.6V, OR FOR +5V SUPPLY

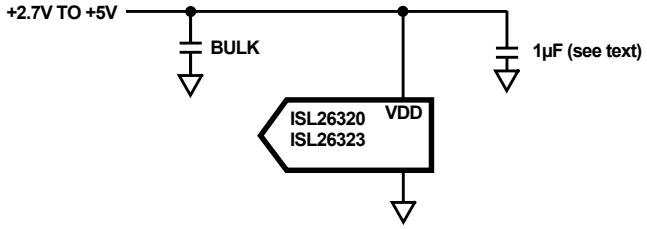


FIGURE 29. VOLTAGE REFERENCE FOR ISL26320/ISL26323 IS DERIVED FROM VDD

TABLE 1. OUTPUT CODES - DIFFERENTIAL

Input Voltage	Two's Complement (12-bit)
>(VFS-1.5 LSB)	7FF
VFS-1.5 LSB	7FF ... 7FE
-0.5 LSB	000 ... FFF
-VFS +0.5 LSB	801 ... 800

NOTE: VFS in the table above equals the voltage between AIN+ and AIN-. Differential full scale is equal to 2* VREF.

TABLE 2. OUTPUT CODES - SINGLE-ENDED

Input Voltage	Binary (12 bit)
>AIN-1.5 LSB	FFF
AIN-1.5 LSB	FFF ... FFE
0.5 LSB	001 ... 000
<0.5 LSB	000

NOTE: Single-ended full scale is equal to VREF.

Serial Digital Interface

The ISL26320/21/22/23/24/25/29 family utilizes an SPI-compatible interface to set the device configuration and read conversion data. This flexible interface provides 3 modes of operation: Reading After Conversion (RAC), Reading During Conversion (RDC), and Reading Spanning Conversions (RSC), with an additional option providing an End of Conversion (EOC) indication on the SDO output in all 3 modes. The choice of operating mode is determined by the timing of the signals on the serial interface.

The interface consists of the data clock (SCLK), serial digital input (SDI), serial digital output (SDO), and the conversion control input (CNV). From the Idle state (after completion of a prior conversion), a High-to-Low transition on CNV indicates the beginning of input signal acquisition, with the Conversion then initiated by a subsequent Low-to-High transition. When CNV is Low, input data presented to SDI is latched on the rising edge of SCLK. Output data will be present at SDO on the falling edge of SCLK. SDO is in the high-impedance state whenever CNV is High, and activity on SCLK should be avoided during this time to avoid corruption of the conversion process. SCLK should be Low when CNV is High.

During the Nth conversion, output data indicates the conversion data and configuration settings for the N-1th conversion, while the current configuration settings apply to the N+1th conversion.

In order to minimize errors due to digital noise coupling, there should be no activity on the serial interface after the specified t_{DATA} period. Data should be read before the conversion is completed to avoid the newer results being overwritten resulting in a permanent loss of data.

Reading After Conversion Mode Without EOC

In this mode, data transfer always occurs during the Acquisition phase, supporting the widest variety of interface data rates. Figure 30 depicts a timing waveform in this mode. From Idle, the device enters the Acquisition phase when CNV is taken Low. SDO emerges High from a high-impedance state, waiting for an SCLK to present the MSB of the current output data word. The configuration settings can be updated using SDI and at the same time previous conversion results can be read from SDO. After the communication is completed or the required acquisition time (t_{ACQ}) has elapsed – whichever is later – CNV transitions High indicating the start of conversion. CNV must be held High continuously for a minimum of 3.6µs (at 250kSPS) so that the conversion is completed without enabling EOC. Subsequently CNV may be asserted Low at any time so that the next Acquisition phase can begin. This method is suitable for hosts which operate with lower frequency SCLK.

Note that when using slower SPI rates the data transfer time can exceed the minimum acquisition time, which will limit the conversion throughput to less than the maximum specified rate. For example, a 12-bit data transfer takes 12µs with a 1MHz SPI clock. This adds to the 3.6µs conversion time for an effective throughput of 64ksps.

Reading During Conversion Mode Without EOC

From Idle, the user initiates the input signal Acquisition mode by taking CNV Low, and then initiates a conversion after t_{ACQ} by pulsing CNV High. After the conversion starts, data is exchanged on the serial interface while CNV is held Low (as shown in Figure 31). CNV must also be asserted High before t_{DATA} to avoid enabling EOC. This method is ideal for hosts with high SCLK communication rates to operate the device at the highest conversion rates.

At the end of conversion the device enters the Idle state. After the host is certain that the conversion is completed (3.6µs after conversion is initiated at 250kSPS) a new acquisition can be initiated by pulling CNV Low which will initiate the Acquisition state.

Reading Spanning Conversion Mode Without EOC

In applications desiring slower interface data rates and while still maintaining maximum possible throughput, RSC mode can be used to transfer data during both the Acquisition and Conversion phases, as shown in Figure 32.

Data exchange begins during the Acquisition phase until CNV is asserted High to initiate a conversion and SDO returns to the high-impedance state, interrupting the exchange. After CNV is returned Low, SDO will return to the state prior to the CNV pulse in order to avoid data loss. Once again data exchange occurs when CNV is Low. CNV must be asserted High before t_{DATA} in order to avoid enabling EOC.

At the end of conversion the device enters the Idle state. After the host is certain that the conversion is completed (3.6µs after conversion is initiated at 250kSPS) a new acquisition can be initiated by pulling CNV Low, which will take the device back to Acquisition state from Idle state.

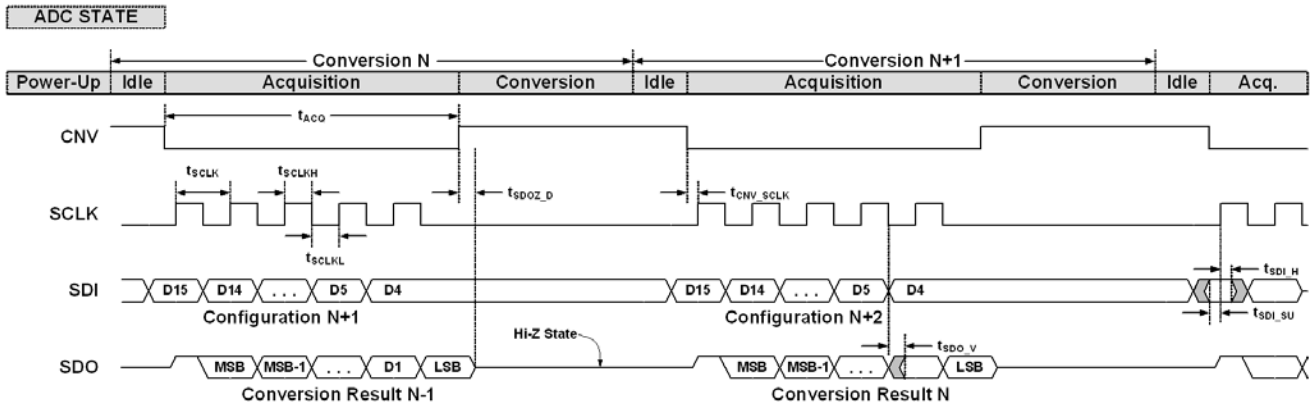


FIGURE 30. TIMING DIAGRAM FOR READING AFTER CONVERSION MODE, WITHOUT EOC

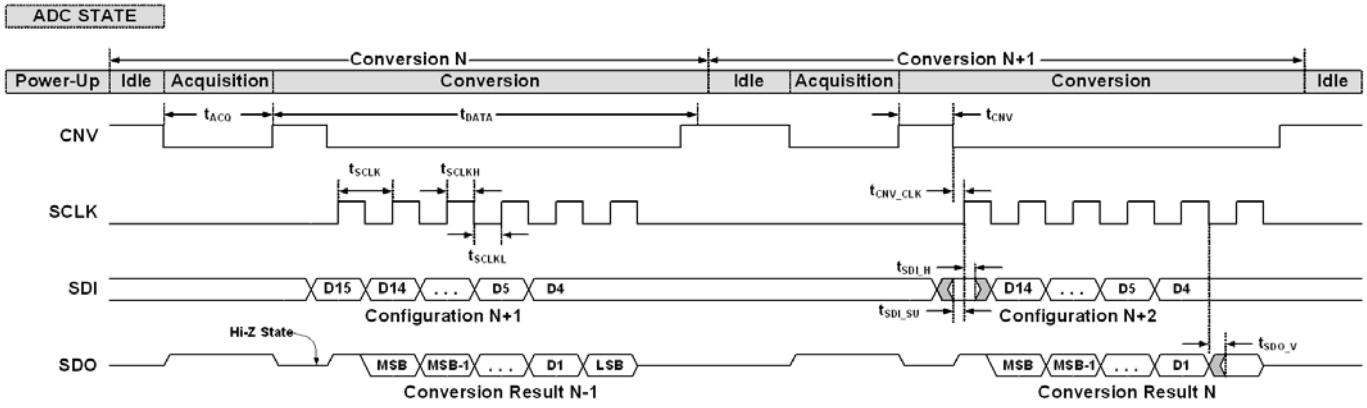
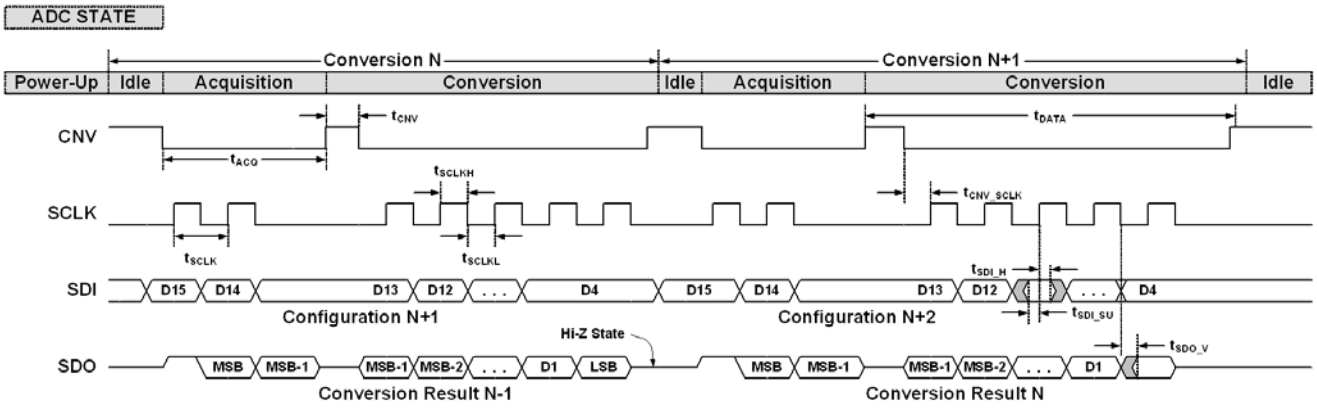


FIGURE 31. TIMING DIAGRAM FOR READING DURING CONVERSION MODE, WITHOUT EOC



Note: Transition from Acquisition to Conversion mode may occur after any integer number of clock cycles (provided that the minimum t_{ACQ} is satisfied).

FIGURE 32. TIMING DIAGRAM FOR READING SPANNING CONVERSION MODE, WITHOUT EOC

Reading After Conversion Mode, with EOC

In this mode (Figure 33), after CNV is asserted Low to start input acquisition, a data exchange is executed by SCLK during the Acquisition period. CNV is asserted High briefly to initiate a Conversion, forcing SDO to a high-impedance state. SDO returns HIGH when CNV is asserted Low during the entire conversion period.

At the end of conversion, the device asserts SDO Low to indicate that the conversion is complete. This may be used as an interrupt to start the Acquisition phase. It should be noted (as indicated in Figure 33) that an additional pulse on CNV is required at the end of conversion to take the part back to Acquisition from Idle state.

As discussed in the "Reading After Conversion Mode Without EOC" section, the acquisition time (t_{ACQ}) may limit the conversion throughput at slower SPI clock rates.

Reading During Conversion Mode, with EOC

From Idle, a falling edge on CNV initiates the Acquisition mode, and then a rising edge initiates a Conversion. After the conversion is initiated, CNV is asserted Low once again. Data exchange across SDI and SDO can proceed while CNV is Low, again observing the requirements of the t_{DATA} period in order to minimize the effects of digital noise on sensitive portions of the conversion. In this mode, an additional pulse is required on SCLK after the completion of the data exchange, to transition SDO to the high-impedance state. Later, SDO is asserted low by the device indicating end of conversion. The device then returns to Idle. The falling edge of SDO may be used as an interrupt to start the Acquisition phase. See Figure 34.

Reading Spanning Conversion Mode, with EOC

After initiating an Acquisition by bringing CNV Low, the user begins exchanging data as previously mentioned, until CNV is asserted High to initiate a conversion and SDO returns to a high-impedance state, interrupting the exchange. And, after CNV is returned Low, SDO will return to the state prior to the CNV pulse in order to avoid losing data interrupted by the conversion pulse. See Figure 35. The user should take care to observe the t_{DATA} period in order to minimize the effects of digital noise on sensitive portions of conversion. After completion of the data exchange, an additional pulse on SCLK forces SDO to a high-impedance state. At the end of conversion, the device asserts SDO Low indicating the end of conversion. The device then returns to Idle, waiting for a pulse on CNV to initiate a new Acquisition cycle.

Accessing the Configuration Register During Data Readback

The Configuration Register contains the channel address of the current conversion data. The contents can be accessed during a normal data output sequence by continuing to clock data from SDO if the register readback mode is enabled. Both 12-bit output data words and the 16-bit configuration word are output in 28 SCLK periods, as shown in Figure 36, which demonstrates an example sequence. Note that SDO goes into the high-impedance state when CNV is High. The Configuration Register can be read during any Read Sequence by generating the additional SCLKs, with the restriction that the sequence must be completed prior to the end of the current conversion. This will prevent loss of data due to overwriting of the new conversion data into the output and configuration registers.

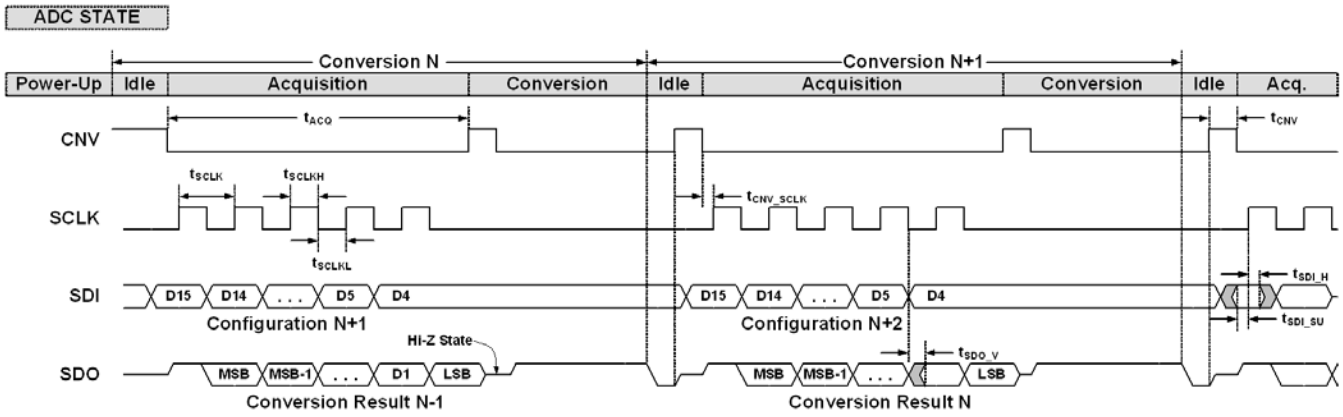


FIGURE 33. TIMING DIAGRAM FOR READING AFTER CONVERSION MODE WITH EOC ON SDO OUTPUT

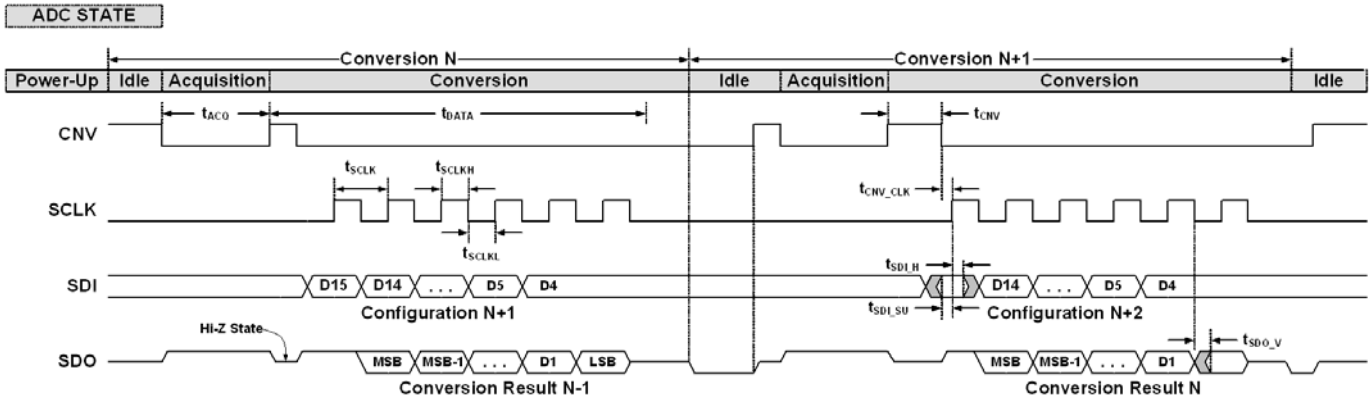
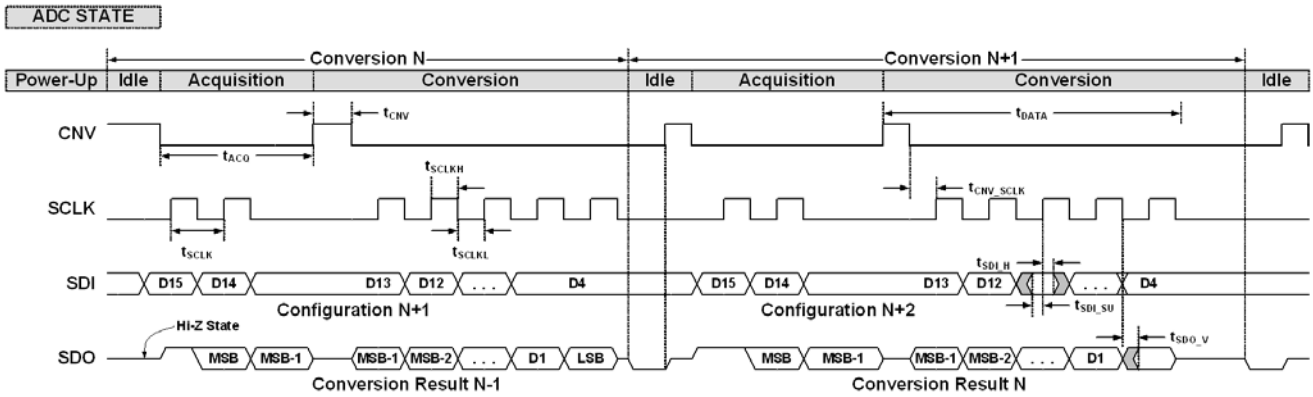


FIGURE 34. TIMING DIAGRAM FOR READING DURING CONVERSION MODE WITH EOC ON SDO OUTPUT



Note: Transition from Acquisition to Conversion mode may occur after any integer number of clock cycles (provided that the minimum t_{ACQ} is satisfied).

FIGURE 35. TIMING DIAGRAM FOR READING SPANNING CONVERSIONS MODE WITH EOC ON SDO OUTPUT

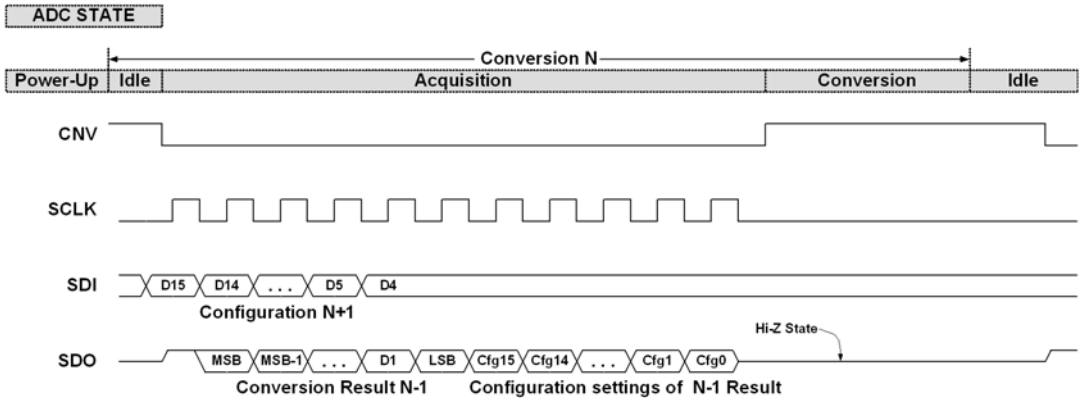


FIGURE 36. TIMING DIAGRAM FOR READING AFTER CONVERSION WITH REGISTER READBACK, WITHOUT EOC

Device Configuration Registers

The Input Multiplexer Channel Select and power management features are controlled by loading the appropriate bits into the 16-bit Configuration Register through the serial port, MSB-first, as shown below. The first two Load bits LD1-LD0 must be set to "11" in order to perform a Register update: any other setting will leave the Register unchanged. Changes to the Configuration Register will be implemented internally immediately following the completion of the current conversion, or require a dummy conversion in order to take effect. Also, in the case of all power management features, a recovery time will be incurred when returning to normal operation, as indicated.

TABLE 3. CONFIGURATION REGISTER

BIT 15 (MSB)	14	13	12	11	10	9	8
LD1	LD0	ADDR2	ADDR1	ADDR0	PM1	PM0	Unused

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RGRD	Unused						

TABLE 4. CONFIGURATION REGISTER 2

BIT(S)	DESCRIPTION
15:14	Register Load word, set to "11" to update registers, otherwise previous settings are retained.
13:11	Multiplexer Channel Select word ADDR2:0.
	000H: Channel AIN0 (single-ended input devices) or AIN0+/AIN0- (differential input devices)
	001H: Channel AIN1 or AIN1+/AIN1-
	010H: Channel AIN2 or AIN2+/AIN2-
	011H: Channel AIN3 or AIN3+/AIN3-
	100H: Channel AIN4
	101H: Channel AIN5
	110H: Channel AIN6
	111H: Channel AIN7
10:9	Power Management Configuration Control
	00H: Auto Power-Down mode. Device will go into Power-down mode automatically at the end of the next conversion cycle.
	01H: Continuous Operation mode (default). Device remains fully powered at all times.
	1xH: Auto Sleep Mode. Device will enter reduced-power Sleep mode automatically at the end of the next conversion cycle. A "1" in PM1 overrides the setting in PM0.
8	Unused
7	Register readback mode. "1" means register readback is enabled resulting in configuration settings to be output along with conversion results. "0" (default) mode of operation register settings are not output.
6:0	Unused

Power Management Modes

In all SPI interface modes (RAC, RDC, etc.) the device has three states of operation: Acquisition, Conversion and Idle. Power management modes decide the state of the ADC in Idle mode and are selected by the PM bits in the Configuration Register as shown in Table 3 and Table 4.

In the default mode (Continuous Operation) the ADC is fully powered in the Idle state and can be taken back to the Acquisition state instantaneously. In this mode the ADC can be operated with maximum throughput and hence is ideally suitable for applications where the ADC is operated continuously.

In Auto Sleep Mode the ISL263XX will be in a sleep state consuming less than 0.4mA. However, it should be noted that the requirements on t_{ACQ} are more stringent in Auto Sleep mode since the device must wake up and then perform the Acquisition.

In Auto Power Down Mode (as selected by PM bits) the ADC will be in power-down condition during the Idle period, consuming less than 5µA of current. Wake-up time takes 150µs. The acquisition time (t_{ACQ}) must be increased to account for this delay.

The power management modes provide a high degree of flexibility in trading average power consumption versus the required throughput. Significant power savings can be achieved by operating in either Auto Sleep Mode or Auto Power-Down mode depending on the throughput requirements.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
June 8, 2012	FN8273.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL26320, ISL26321, ISL26322, ISL26323, ISL26324, ISL26325, ISL26329 .

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

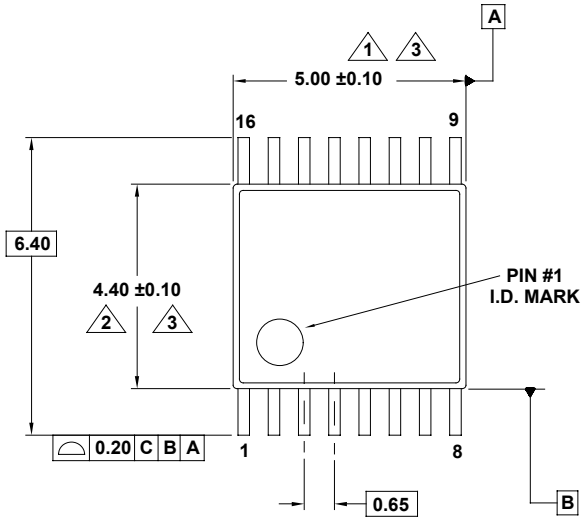
FITs are available from our website at: http://rel.intersil.com/reports/sear

Package Outline Drawing

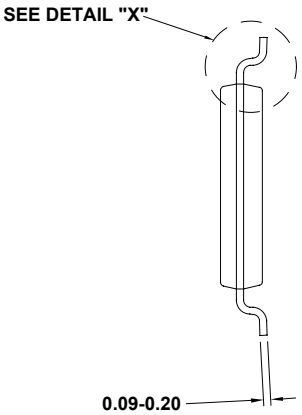
M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

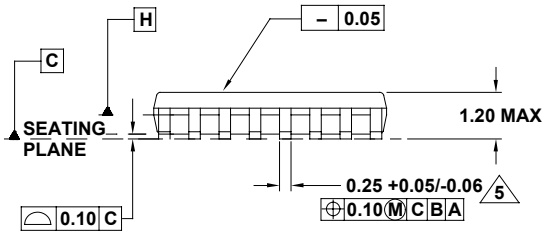
Rev 2, 5/10



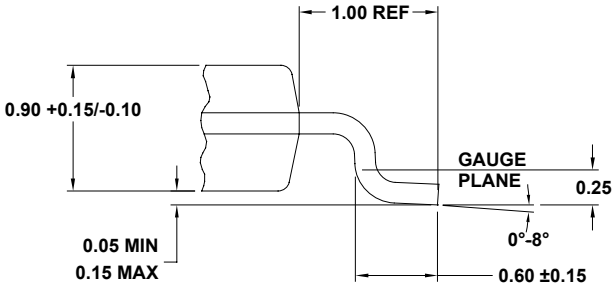
TOP VIEW



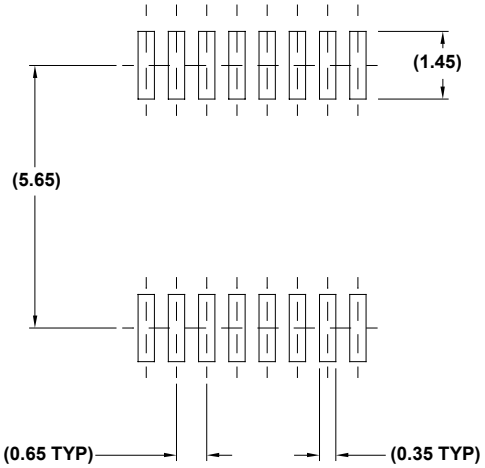
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

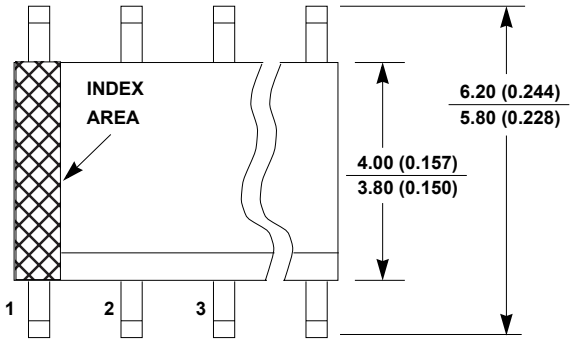
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

Package Outline Drawing

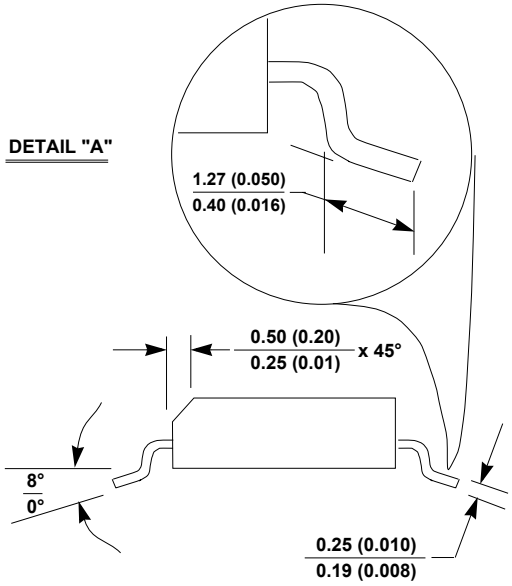
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

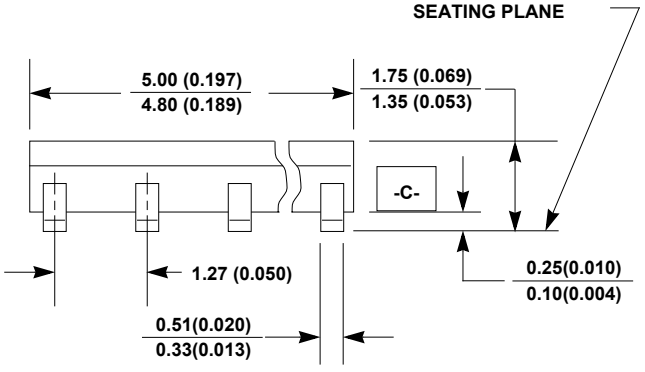
Rev 4, 1/12



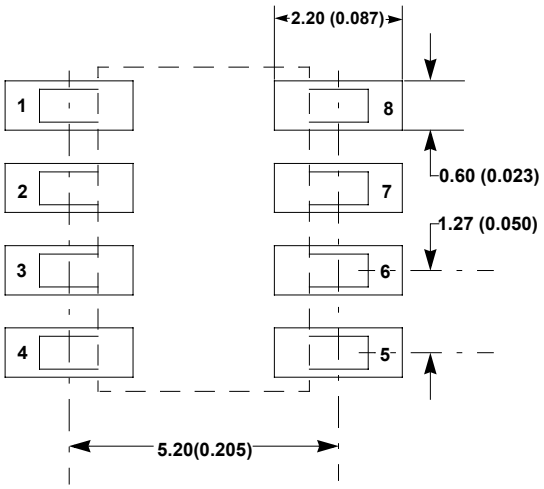
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.