# 6/3 X 8 PORT EXPANDER

## FEATURES

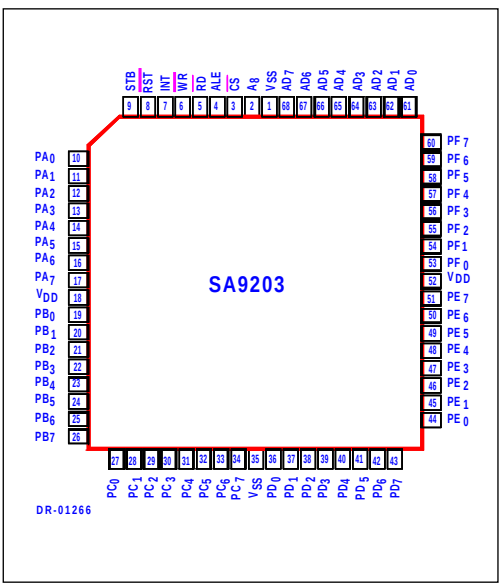
- Six (SA9203) or three (SA9205) 8-Bit I/O Ports
- Each bit of one port independently programmable as input or output
- Five (SA9203) or two (SA9205) remaining ports can be individually configured as input or output. (Direction applicable to all 8 pins of each port.)
- One 8-Bit port programmable as either atched or transparent inputs
- Supports byte-wide and bit-wide I/O port addressing modes on all ports
- Readback of all control and port registers
- Interfaces directly with multiplexed address and data bus microprocessors/ microcontrollers
- Internal address latch
- Single +5V power supply
- Low power CMOS
- Completely static operation
- TTL-level compatibility

## DESCRIPTION

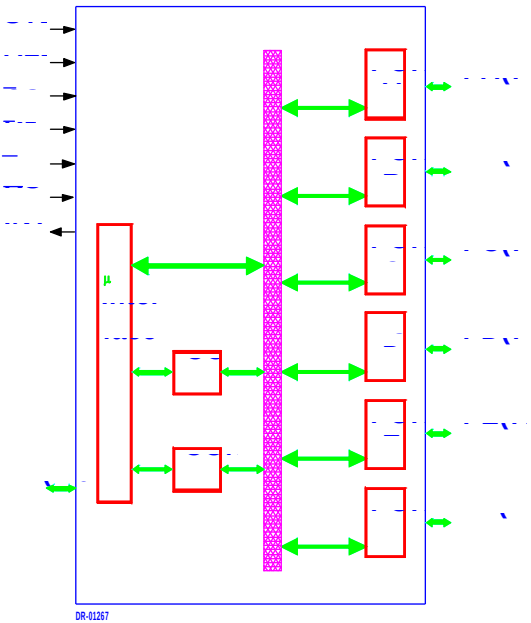
The SAMES SA9203/5 Port Expander is a CMOS device suited to microprocessor based applications requiring input/output port expansion. The device interfaces very simply to any microcontroller/microprocessor with a multiplexed address/data bus structure.

The SA9203 includes 8 independently programmable I/O pins for Port A and Port B to F (5 ports) independently programmable as I/O. It is packaged in a PCB efficient 68 pin PLCC package. The SA9205 includes 8 independently programmable I/O pins for Port A with Port B and Port C as independently programmable I/O, packaged in a cost effective 44 pin PLCC package.

## FIGURE 1: PIN CONNECTION FOR SA9203



## FIGURE 2: BLOCK DIAGRAM FOR SA9203




## FIGURE 3: PIN CONNECTION FOR SA9205

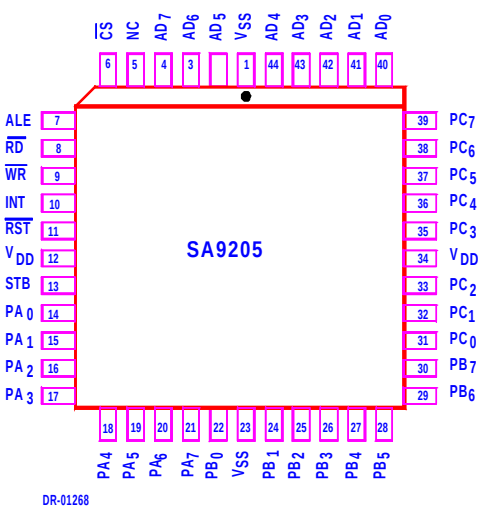
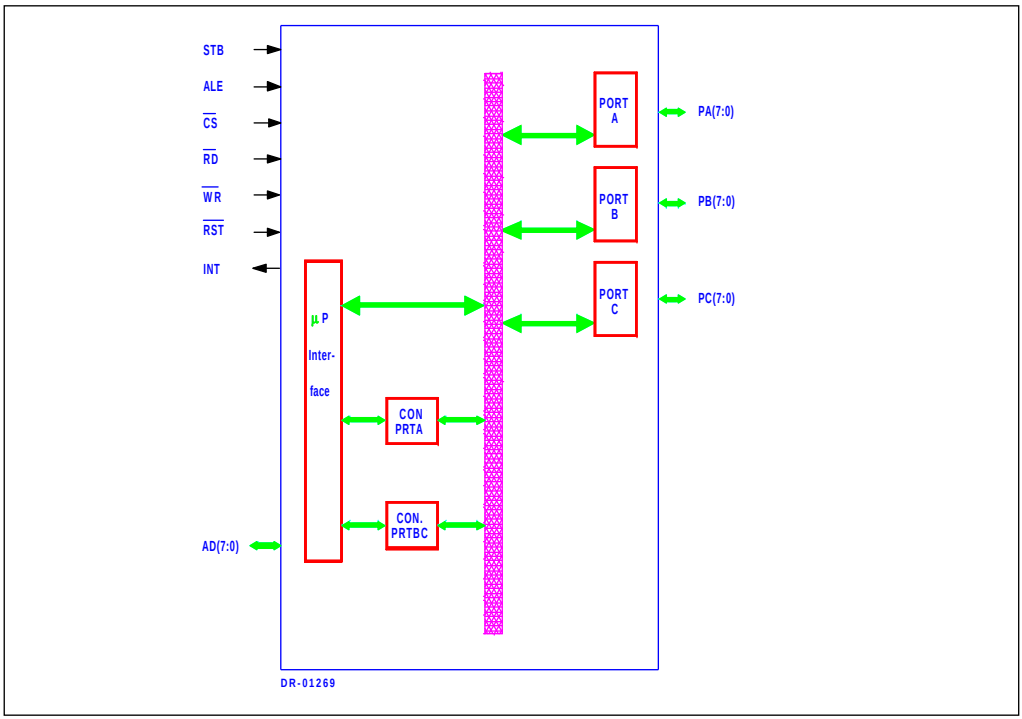


**FIGURE 4: BLOCK DIAGRAM FOR SA9205**




## ABSOLUTE MAXIMUM RATINGS*

(All voltages are with respect to VSS)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$-$V_{SS}$ | $V_{SS}$ | 7,0 | V |
| Voltage on any pin | $V_M$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| Current at any pin | $I_M$ | | 100 | mA |
| Storage Temperature | $T_{STG}$ | -40 | +125 | °C |
| Operating Temperature | $T_O$ | 0 | +70 | °C |

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(All measurements with respect to VSS, at 25°C, unless otherwise specified)

| Parameters | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V | |
| Static Current | $I_{DDS}$ | | 15 | 50 | µA | VDD = 5.0V (See Note1) |
| Dynamic Current | $I_{DDD}$ | | | 20 | mA | VDD = 5.0V |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | VDD = 5.0V |
| Input Low Voltage | $V_{IL}$ | | | 1.0 | V | VDD = 5.0V |
| Output High Voltage | $V_{OH}$ | 4.5 | 4.7 | | V | VDD = 5.0V $I_{OH}$ = 5mA |
| Output Low Voltage | $V_{OL}$ | | 0.25 | 0.5 | V | VDD = 5.0V $I_{OH}$ = 5mA |
| Input Leakage Current | $I_{IN}$ | | <1.0 | 3.0 | µA | VDD = 5.0V |
| Tristate Leakage Current | $I_{TL}$ | | <1.0 | 3.0 | µA | VDD = 5.0V |

**Note 1**: All inputs tied to VDD or VSS with outputs not loaded. Measurements made after RST applied.

## PIN DESCRIPTION for SA9203

| Pin | Type | Designation | Description |
|---|---|---|---|
| 18,52 | | VDD | +5V Supply Input |
| 1,35 | | VSS | 0V ground Reference |
| 61..68 | I/O | AD0..AD7 | 3-state address/data lines that interface with the CPU lower 8-bit address/data bus. The 8-bit address is latched into the SA9203 internal address latch on the falling edge of ALE. The 8-bit data is respectively written into and read out of the SA9203 on $\overline{WR}$ and $\overline{RD}$ signals. |
| 2 | | N/C | Not connected. |
| 3 | I | $\overline{CS}$ | Active low input signal used to select the device. |
| 4 | I | ALE | This control signal latches the address on the AD0..7 lines on the falling edge of ALE. |
| 5 | I | $\overline{RD}$ | Input low on this line enables the data bus buffers. |
| 6 | I | $\overline{WR}$ | Input low on this line causes the data on the address/ data bus to be written to the I/O ports and, control registers. |
| 7 | O | INT | If enabled via A.6, this output will be set (active edge polarity programmed by D6 and output polarity programmed via D7 of the Port B-F direction control register) after data has been latched into PORT A. |
| 8 | I | $\overline{RST}$ | Input low on this line resets the chip and all internal registers and all ports to input mode (The register contents after a reset pulse will be described later). |
| 9 | I | STB | Input data on PORT A pins will be latched when STB is active and transparent otherwise (polarity programmed by D5 of the Port B-F direction control register) |
| 10..17 | I/O | PA0..PA7 | 8 general purpose I/O pins comprising PORT A. This port supports individual input or latched output configuration of each pin. In addition,each pin of PORT A selected as an input can be programmed to be latched or transparent. |
| 19..26 | I/O | PB0..PB7 | 8 general purpose I/O pins comprising PORT B. All 8 pins are programmed to be either latched outputs or transparent inputs. |
| 27..34 | I/O | PC0..PC7 | Identical to PORT B |
| 36..43 | I/O | PD0..PD7 | Identical to PORT B |
| 44..51 | I/O | PE0..PE7 | Identical to PORT B |
| 53..60 | I/O | PF0..PF7 | Identical to PORT B |

## PIN DESCRIPTION for SA9205

| Pin | Type | Designation | Description |
|---|---|---|---|
| 2,35 | | VDD | +5V Supply Input |
| 1,23 | | VSS | 0V ground Reference |
| 40..44 | I/O | AD0..AD7 | 3-state address/data lines that interface with the CPU lower 8-bit address/data bus. The 8-bit address is latched into the SA9203 internal address latch on the falling edge of ALE. The 8-bit data is respectively written into and read out of the SA9203 on $\overline{WR}$ and $\overline{RD}$ signals. |
| 5 | | N/C | Not connected. |
| 6 | I | CS | Active low input signal used to select the device. |
| 7 | I | ALE | This control signal latches the address on the AD0..7 lines on the falling edge of ALE. |
| 8 | I | RD | Input low on this line enables the data bus buffers. |
| 9 | I | WR | Input low on this line causes the data on the address/ data bus to be written to the I/O ports and, control registers. |
| 10 | O | INT | If enabled via A.6, this output will be set (active edge polarity programmed by D6 and output polarity programmed via D7 of the Port B-F direction control register) after data has been latched into PORT A. |
| 11 | I | RST | Input low on this line resets the chip and all internal registers and all ports to input mode (The register contents after a reset pulse will be described later). |
| 13 | I | STB | Input data on PORT A pins will be latched when STB is active and transparent otherwise (polarity programmed by D5 of the Port B-F direction control register) |
| 14..21 | I/O | PA0..PA7 | 8 general purpose I/O pins comprising PORT A. This port supports individual input or latched output configuration of each pin . In addition,each pin of PORT A selected as an input can be programmed to be latched or transparent. |
| 22, 24.30 | I/O | PB0..PB7 | 8 general purpose I/O pins comprising PORT B. All 8 pins are programmed to be either latched outputs or transparent inputs. |
| 31..39 | I/O | PC0..PC7 | Identical to PORT B |

## FUNCTIONAL DESCRIPTION

The SA9203 contains the following:

- Six 8-bit general purpose I/O ports programmable to be either byte or bit addressable.
- Two control registers for configuring the device. These control registers can be read back.
- An internal address latch for accessing a multiplexed CPU address/data bus.
- The SA9203 appears to the CPU as a peripheral device occupying 256 bytes of memory space. Certain locations in the memory map are occupied by the six I/O ports and two control registers.

The SA9203 supports two basic I/O port addressing modes, via; byte-addressing and bit-addressing. Any of the six I/O ports can be configured as byte-addressable /or bit-addressable. In bit-addressing, individual bits of any I/O port can be addressed independently. In a bit- addressing CPU read operation, D0 contains valid data while D1..D7 should be ignored. In a bit-addressing CPU write operation, D0 will be written to the addressed output pin while D1..D7 will be ignored. The Address Memory map is shown in Figure 5. The bit-addressing mode applies to both the I/O ports and the control registers. The SA9205 is a three port device with operation is identical to the SA9203.

**FIGURE 5: Address Memory Map**

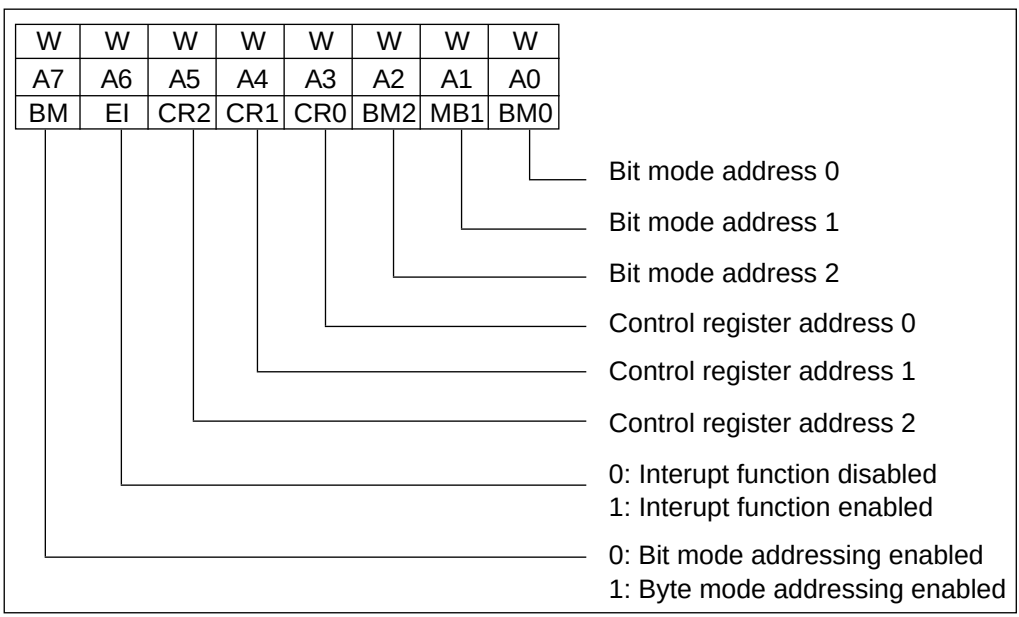


**FIGURE 6: PORT A Direction Control Register Address.**

| A5 | A4 | A3 |
|---|---|---|
| 1 | 1 | 0 |

**FIGURE 7: PORT B..F Direction Control Register / Strobe Control Register Address**

| A5 | A4 | A3 |
|---|---|---|
| 1 | 1 | 1 |

**FIGURE 8: PORT Addresses**

| A5 | A4 | A3 | PORT |
|---|---|---|---|
| 0 | 0 | 0 | PORT A |
| 0 | 0 | 1 | PORT B |
| 0 | 1 | 0 | PORT C |
| 0 | 1 | 1 | PORT D * |
| 1 | 0 | 0 | PORT E * |
| 1 | 0 | 1 | PORT F * |

* - n/a for the SA9205

**FIGURE 9: Port Pin Addresses (Bit Mode Only).**

| A2 | A1 | A0 | PORT PIN |
|---|---|---|---|
| 0 | 0 | 0 | PORT A-F.0 |
| 0 | 0 | 1 | PORT A-F.1 |
| 0 | 1 | 0 | PORT A-F.2 |
| 0 | 1 | 1 | PORT A-F.3 |
| 1 | 0 | 0 | PORT A-F.4 |
| 1 | 0 | 1 | PORT A-F.5 |
| 1 | 1 | 0 | PORT A-F.6 |
| 1 | 1 | 1 | PORT A-F.7 |

Note : PORT A-C for SA9205

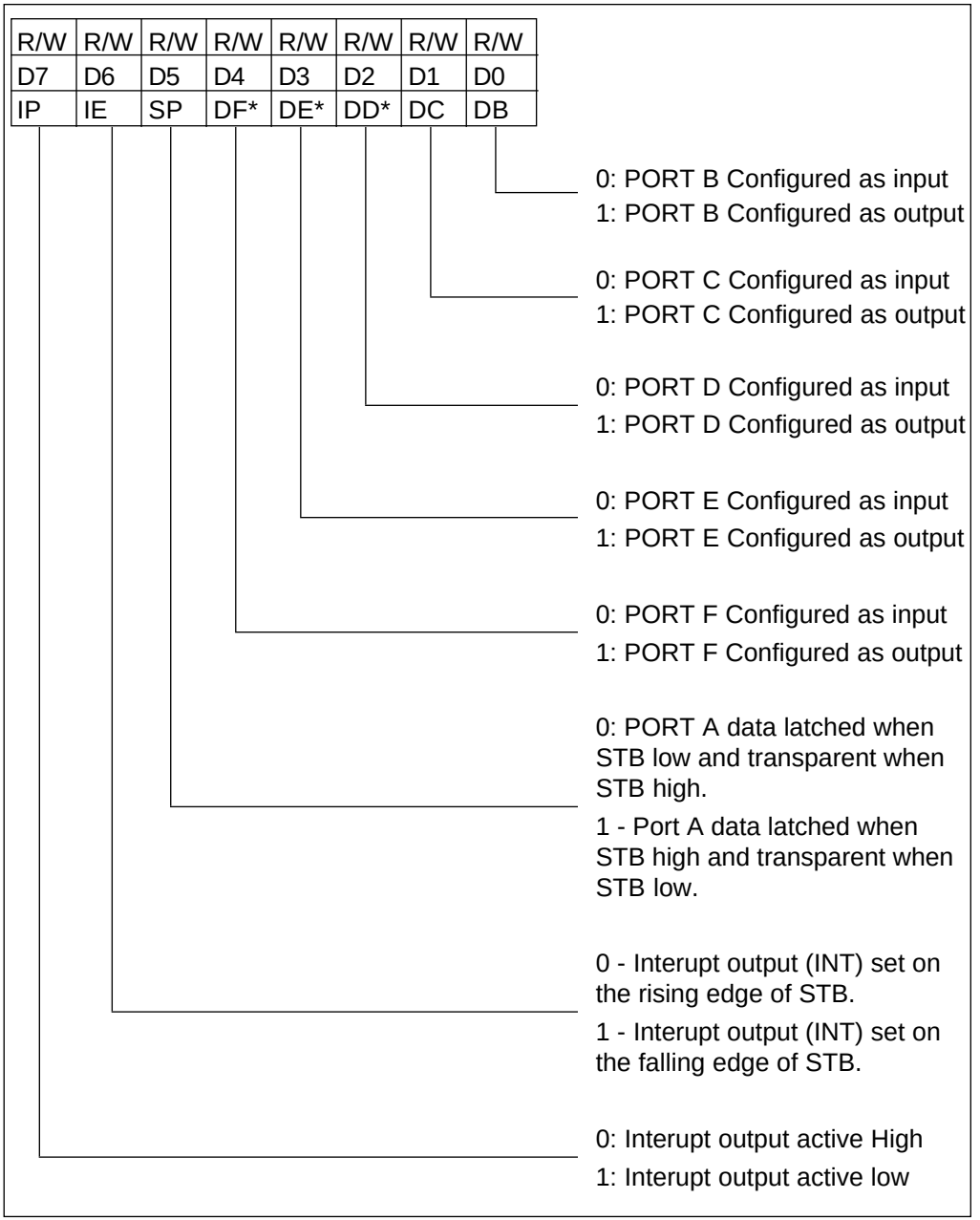
**CONTROL REGISTERS**

**FIGURE 10: PORT A Direction Control Register**

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PA.7 | PA.6 | PA.5 | PA.4 | PA.3 | PA.2 | PA.1 | PA.0 |

D = 1 Port A Pin configured as output
D = 0 Port A Pin configured as input.

**FIGURE 11: PORT B-F Direction Control / Strobe Control Register Address**




* n/a for the SA9205

**INT**

This active high output (default after reset) operates as follows:
When disabled (via A6), INT remains reset. On either the rising or trailing edge of STB (programmable via D6 of Port B-F direction control register), INT is set. INT remains set until Port A (or any bit of PORT A if in bit- addressing mode) is read by the microprocessor at which point INT is reset, remaining so until the next active edge of STB. (See figure 14 for timing diagram). The output polarity of INT is programmed via D7 of the Port B- F dirction control register (See Figure 11).

**RST**

This active low reset signal resets the contents of all registers to zero. Sets all ports to input mode and the bi-directional data/address bus to input. A valid RST signal is specified as an active low pulse of 100ns minimum duration.

**CS**

The active low CS signal is internally latched by the trailing edge of ALE.

## TIMING DIAGRAMS

**FIGURE 12: µP Read Waveforms**

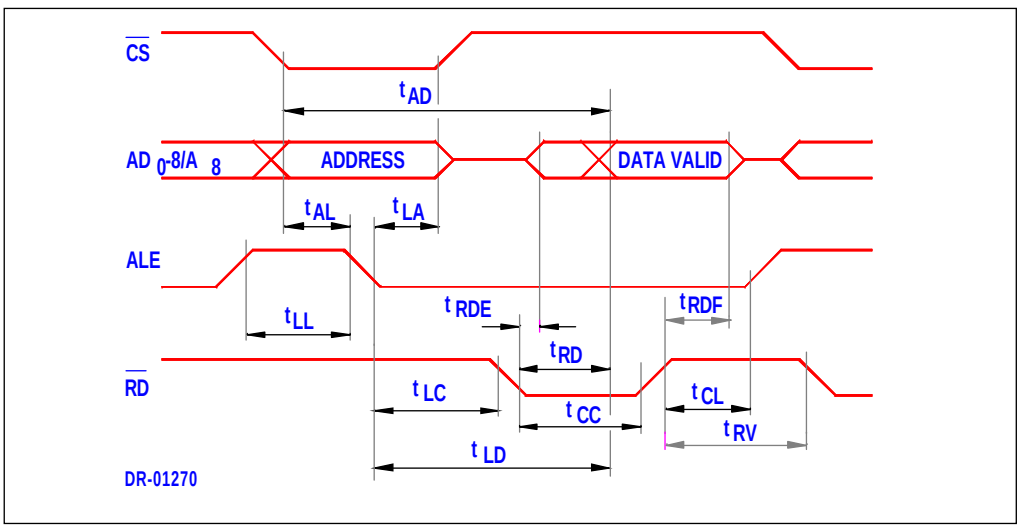


**FIGURE 13: µP Write Waveforms**

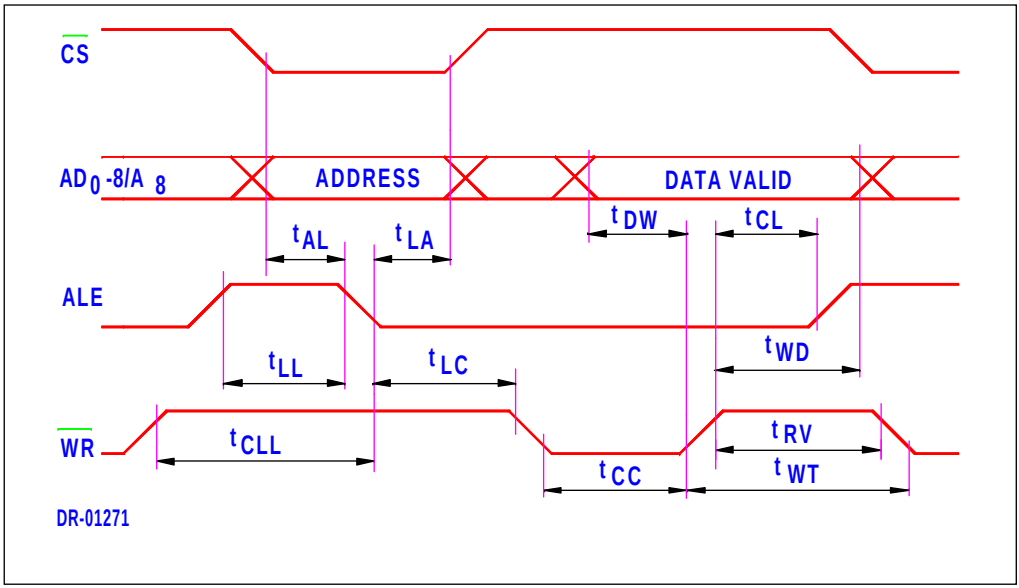



**FIGURE 14: µP Strobe/Interrupt Waveforms**

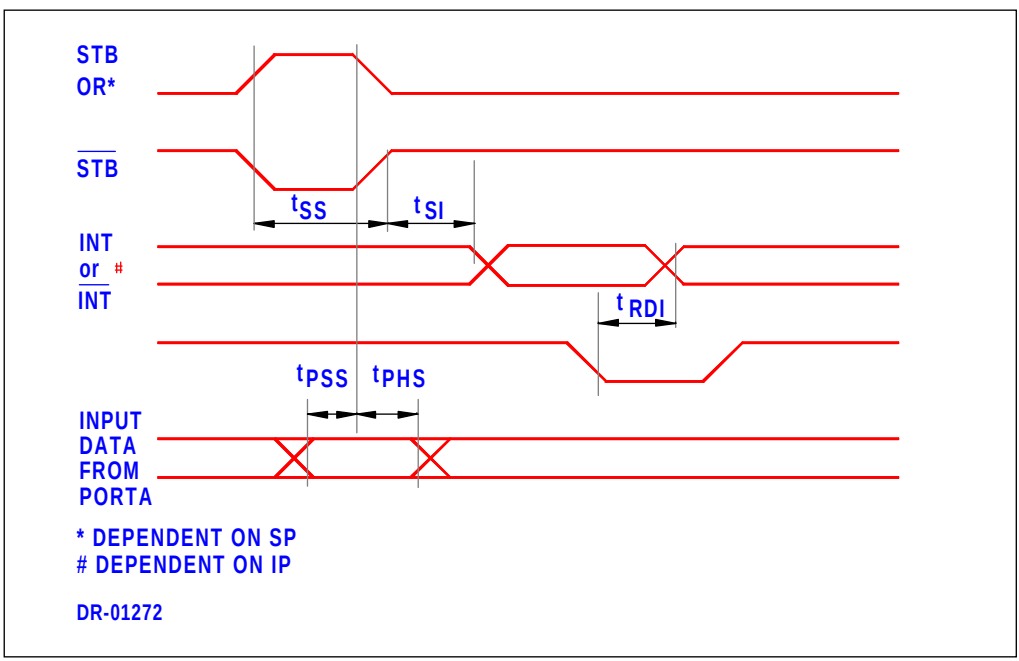


**FIGURE 15: I/O Port Waveforms Transparent Output**

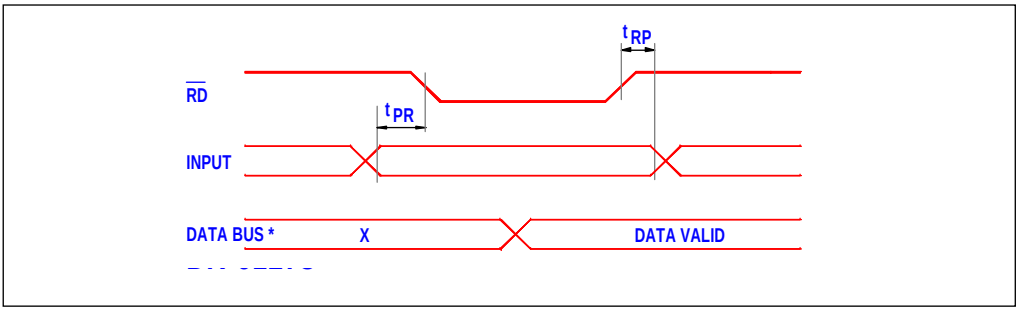



**FIGURE 16: µP Read Waveforms Latched Output**

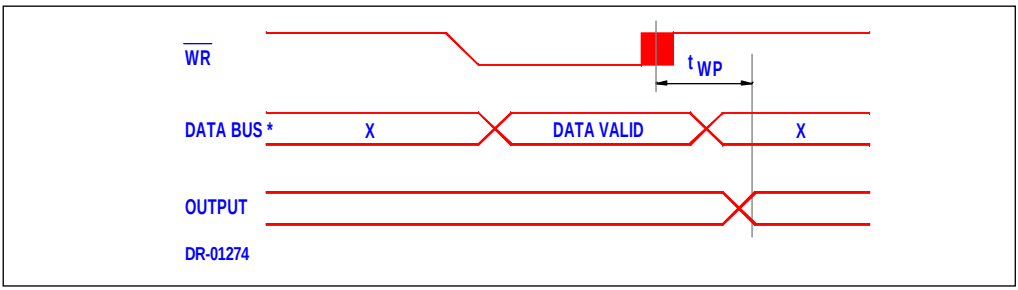



**Table 1: AC Characteristics for µP Interface1 - TA = 0°C to 70°C, VDD = 5V 10%**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AL}$ | Address to Latch Setup Time | 10 | | ns |
| $t_{LA}$ | Address Hold Time after Latch | 10 | | ns |
| $t_{LC}$ | Latch to READ/WRITE Control | 10 | | ns |
| $t_{RD}$ | Valid Data Out Delay from READ Control | | 50 | ns |
| $t_{LD}$ | Latch to Data Out Valid | | 50 | ns |
| $t_{AD}$ | Address Stable to Data Out Valid | | 100 | ns |
| $t_{LL}$ | Latch Enable Width | 30 | | ns |
| $t_{RDF}$ | Data Bus Float after READ | 0 | 40 | ns |
| $t_{CL}$ | READ/WRITE Control to Latch Enable | 10 | | ns |
| $t_{CLL}$ | WRITE Control to Latch Enable | 50 | | ns |
| $t_{CC}$ | READ/WRITE Control Width | 60 | | ns |
| $t_{DW}$ | Data in to WRITE Setup Time | 20 | | ns |
| $t_{WD}$ | Data in Hold Time after WRITE | 20 | | ns |
| $t_{RV}$ | Recovery Time between READ/WRITE | 50 | | ns |
| $t_{RDE}$ | Data Bus Enable from READ Control | 10 | | ns |

**Table 2: A.C. Characteristics for I/O Ports**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{PR}$ | Port Input Setup Time | 20 | | ns |
| $t_{RP}$ | Port Input Hold Time | 0 | | ns |
| $t_{SS}$ | Strobe Width | 100 | | ns |
| $t_{SI}$ | Strobe to INT Set | | 100 | ns |
| $t_{RD}$ | READ to INT Reset | | 100 | ns |
| $t_{PSS}$ | Port Setup Time to Strobe | 50 | | ns |
| $t_{PHS}$ | Port Hold Time After Strobe | 120 | | ns |
| $t_{WP}$ | WRITE to Port Output | | 80 | ns |

**Note 1:** Timing parameters are preliminary and subject to change.

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