

FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- ECL and TTL enable inputs
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H600
- Available in 28-pin PLCC package

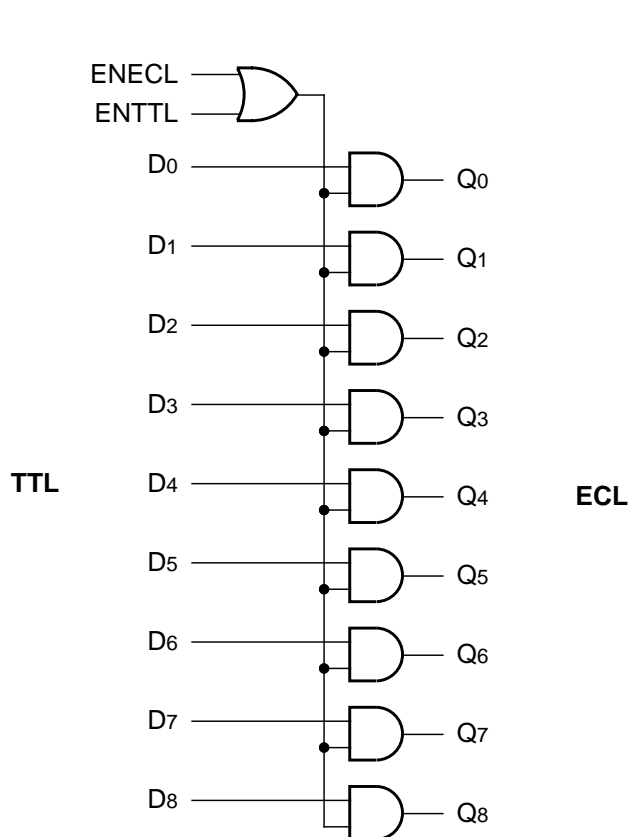
DESCRIPTION

The SY10/100H600 are 9-bit, dual supply TTL-to-ECL translators. Devices in the Micrel-Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

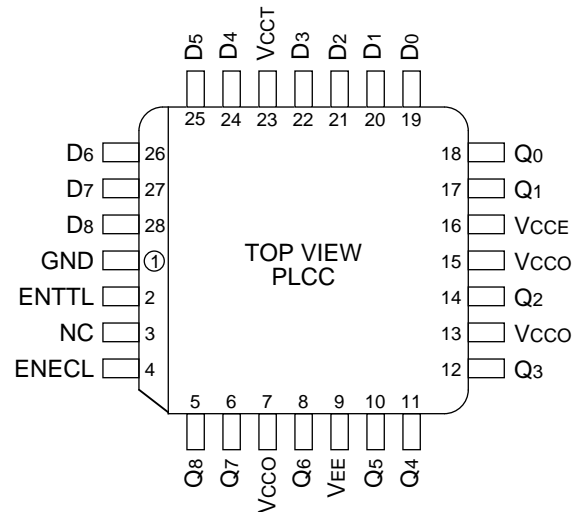
The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

| Pin | Function |
|-------|-------------------------|
| GND | TTL Ground (0V) |
| VcCE | ECL Vcc (0V) |
| VcCO | ECL Vcc (0V) — Outputs |
| VcCT | TTL Supply (+5.0V) |
| VEE | ECL Supply (-5.2/-4.5V) |
| D0-D8 | Data Inputs (TTL) |
| Q0-Q8 | Data Outputs (ECL) |
| ENECL | Enable Control (ECL) |
| ENTTL | Enable Control (TTL) |

TRUTH TABLE

| ENECL | ENTTL | D | Q |
|-------|-------|---|---|
| H | X | H | H |
| H | X | L | L |
| X | H | H | H |
| X | H | L | L |
| L | L | X | L |

DC ELECTRICAL CHARACTERISTICS

V_{CC}T = 5.0V ± 10%; V_{EE} = -4.75V to -5.5V (10H Version); V_{EE} = -4.2V to -5.5V (100H Version)

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +85°C | | Unit | Condition |
|------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| I _{EE} | Power Supply Current, ECL 10H 100H | — | 125 | — | 125 | — | 125 | mA | — |
| | | — | 122 | — | 123 | — | 132 | | |
| I _{CC} I _{CL} | Power Supply Current, TTL | — | 48 | — | 48 | — | 48 | mA | — |
| | | — | 50 | — | 50 | — | 50 | | |

AC ELECTRICAL CHARACTERISTICS

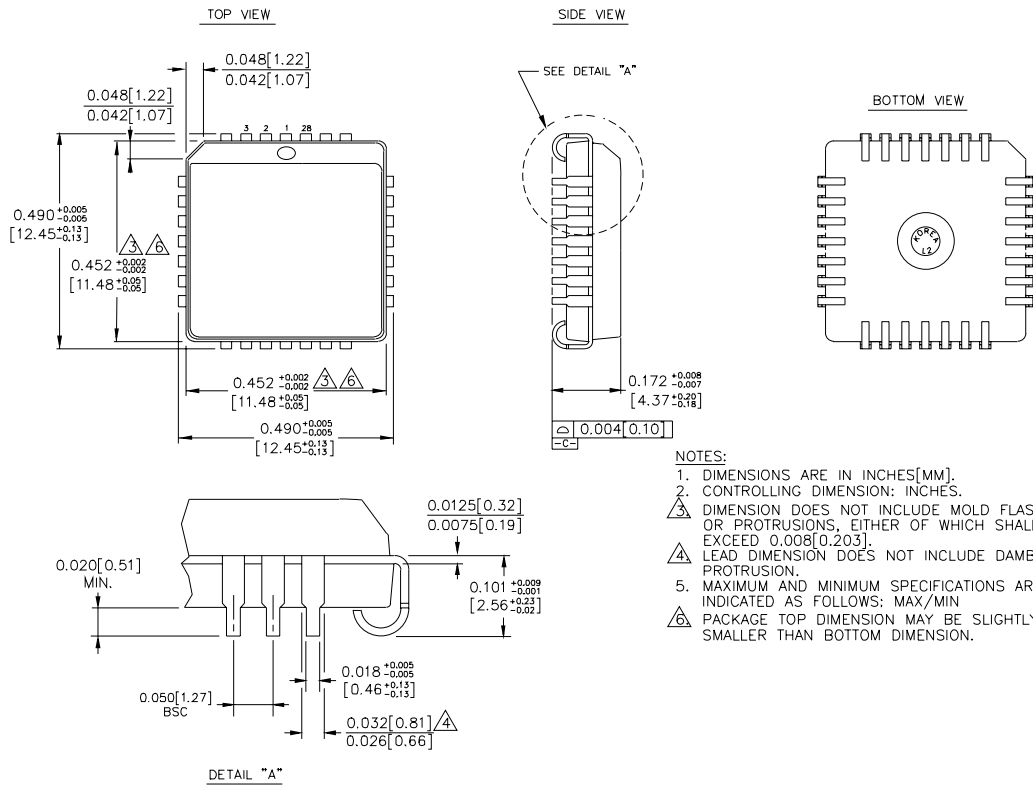
V_{CC}T = 5.0V ± 10%; V_{EE} = -4.75V to -5.5V (10H Version); V_{EE} = -4.2V to -5.5V (100H Version)

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +85°C | | Unit | Condition |
|--------------------------------------|---|----------------------|------------|------------------------|------------|------------------------|------------|------|--------------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay to Output D ENECL/ENTTL | 1.4 1.8 | 3.0 3.7 | 1.5 1.9 | 3.2 3.9 | 1.7 2.0 | 3.5 4.1 | ns | 50Ω to -2.0V |
| t _r t _f | Output Rise/Fall Time 20% to 80%, 80% to 20% | 0.5 | 1.5 | 0.5 | 1.5 | 0.5 | 1.5 | | |

PRODUCT ORDERING CODE

| Ordering Code | Package Type | Operating Range |
|---------------|--------------|-----------------|
| SY10H600JC | J28-1 | Commercial |
| SY10H600JCTR | J28-1 | Commercial |
| SY100H600JC | J28-1 | Commercial |
| SY100H600JCTR | J28-1 | Commercial |

28 LEAD PLCC (J28-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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