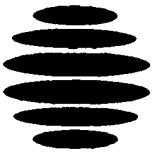

UNIVERSAL SEMICONDUCTOR INC.

ANALOG-DIGITAL CMOS

SEMI-CUSTOM SYSTEMS

ON A CHIP

USI-6000

SEMI-CUSTOM ARRAY

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HIGH PERFORMANCE, HIGH RELIABILITY, CMOS ARRAY FAMILY ACHIEVES TRUE ANALOG/DIGITAL SYSTEMS-ON-A CHIP

INTRODUCTION

MOS VLSI technology have ushered in an era of increased integration capability. The push is on to combine more and more circuitry, analog, as well as digital, onto a single integrated circuit.

Attempts to combine analog and digital functions on first generation metal-gate CMOS arrays suffered from the lack of the proper types of components needed for the analog circuitry. These arrays contained transistors optimized for digital performance. Components such as high value resistors and true MOS capacitors were completely missing. This tended to result in analog circuits which required many external components. In addition, whole classes of important sampled data analog circuitry using switched capacitor techniques could not be accommodated at all.

A new family of advanced oxide isolated silicon-gate CMOS arrays, the USI-6000 series offered by Universal Semiconductor, Inc. San Jose, California, was designed to overcome the performance limitations of the first generation arrays. The basic philosophy was to provide the fullest possible spectrum of available uncommitted components tailored to optimize both analog and digital circuit performance. To maximize flexibility, design is accomplished at the transistor or component level. The same transistor which is part of a CMOS operational amplifier in one circuit, might be part of a precision voltage-to- frequency converter in another circuit. An MOS capacitor might be used to form the timing capacitor in a CMOS RC oscillator in one circuit or perhaps be part of a switched capacitor filter in yet another design. This concept provides the ideal interface solution.

FAMILY

The USI-6000 array series consists of 6 different family member (USI- 6001 through USI-6006). Architecturally, each member can be broken into a mixture of two distinct area types:

1. A predominantly digital area characterized by MOS transistors with 4 micron and 6 micron channel lengths.

2. A predominantly analog area characterized by 12 micron and 24 micron channel length MOS transistors and passive elements such as resistors and capacitors.

A breakdown of each member in terms of a classical "average of 2 1/2 input" gate count of the predominantly digital area and a percentage of chip area devoted to the predominantly analog section appears below:

FAMILY MEMBER	DIGITAL GATE COUNT	ANALOG AREA PERCENTAGE
USI-6001	415	30
USI-6003	250	60
USI-6004	660	30
USI-6005	230	30
USI-6006	135	60

Since a large number of different arrays are available, most applications can be integrated efficiently (greater than 80% component utilization) on at least one member of the family. The family is specified over an operating voltage range of 2 volts to 15 volts, and an operating temperature range of -55 degrees C. to +125 degrees C.

AVAILABLE COMPONENTS

A list of available USI-6000 series component types with a brief description of each appears below:

1. Digital core transistors (PMOS width/length ratio = 44u/4u, NMOS = 44u/4u)

Designed for purely digital applications. The gates of each NMOS transistor and its corresponding PMOS transistor share a common gate. This is not a normal connection for analog circuit design.

2. Dedicated D type flip-flops

Requires one-half the die area required to configure a D type flip-flop than would be required if formed by digital core transistors. Toggles at frequencies up to 20 MHZ.

3. 4 Micron split-gate analog/digital transistors (PMOS = 68u/4u, NMOS = 32u/4u)

Designed for both analog and digital applications. Each transistor has a separate gate. The W/L ratios are matched for equal transconductance rather than equal size. For the NMOS transistors, an abundance of isolated P-wells are available. This is useful for eliminating body effect problems which are particularly severe for NMOS transistors. Separate wells also allow for multi-supply applications and enable the NMOS transistor to be configured as a multi-emitter bipolar transistor with collector committed to VDD. Typical transistor beta is 250.

4. 6 Micron split-gate analog/digital transistors (PMOS = 68u/4u, NMOS = 32u/4u).

Same idea as the 4 micron split-gate transistors except that the channel lengths are increased to 6 microns. Increasing the channel length improves device matching and increases the output resistance of the transistor in its saturation region. For example, a 4u channel length yields an output current variation in the saturation region of 6% per volt and 3% per volt for the PMOS and NMOS transistors, respectively. A 6u channel length yields 2% per volt and 1% per volt. The increase in output resistance carries over to the 12 micron and 24 micron channel length transistors.

5. 12u split-gate analog transistors (PMOS = 92u/4u, NMOS = 46u/12u).

This transistor tends to be the workhorse of most analog designs on the USI-6000 family. The 12 micron channel length results in the best compromise between analog precision and analog speed. The transistors are ratioed in size for equal transconductance.

6. 24 Micron split-gate analog/digital transistors (PMOS = 188u/12u, NMOS = 92u/12u).

7. Analog switch transistors (PMOS = 15u/4u, NMOS = 15u/4u).

These transistors are optimized for switched capacitor applications as dual transmission gates. The transistors are uncommitted and may be used for many other digital or analog applications as required.

8. High-impedance transistors

Both NMOS and PMOS, very long channel length transistors, are available in limited quantities. These devices are particularly useful in start- up circuits. Each device is tapped so that any resistance between a few hundred kilohms and 15 megohms can be realized.

9. Peripheral Transistors

Both NMOS and PMOS transistors with large widths and 4 micron channel lengths are available around the chip periphery. "On" resistances down to 50 ohms may be realized by these devices. The NMOS transistors are each in isolated P-wells.

10. MOS capacitors

Unit capacitors of .75 pf exist in abundance. These capacitors have the structure polysilicon-oxide-heavy P+ implant. They may be used with either terminal to any circuit node. The P+ implant node has some parasitic junction capacitance which must be considered.

11. Diffused P-well resistors

P-well resistors are available in strings of typically 5 tapped resistors. The taps occur in 20 kilohm increments. This resistance is characterized by an absolute tolerance of +/-25 percent and a voltage coefficient of resistance of about 1 percent per volt. Metal interconnect traces are not normally allowed to cross these resistors in a layout as this will cause a small amount of resistance modulation.

12. Polysilicon Resistors

The interconnect "cross-unders" are all polysilicon on the USI6000 family. These resistors are typically 150 ohms for a cross-under which is 78 microns long by 12 microns wide. They have no measurable voltage coefficient of resistance. Since they are formed on top of oxide (not as part of a P-N junction) they have effectively zero parasitic capacitance. This is in dramatic contrast to the diffused P+ cross- unders in the metal gate arrays of which each has a .5pf parasitic capacitance. Because these resistors are not formed by a P-N junction, they can be operated at potentials both above and below the maximum and minimum chip supply potentials.

13. Zener diodes

A buried zener diode with a sharp breakdown at 6.2 volts +/-.2 volts is available. The intrinsic series resistance is about 500 ohms. The measured temperature coefficient is +1100 parts per million per degree centigrade.

KIT PARTS

In order to provide the greatest expectation of first time working silicon, Universal Semiconductor, Inc. has a library of proven analog/digital circuits that function as off the shelf solutions to the application. After a paper design has been completed, and critical areas have been simulated, the circuit may be breadboarded with these kit parts. Since these kits are metal mask circuits on the USI-6001, USI-6005 and USI-6006, they will function closely to the final chip. Performance is generally superior on the final chip because of the elimination of all wiring between kits and kit output buffers.

The 25 kits are designed to give most of the basic functions required to build a single chip system solution. Various kit functions are described to show the breadth of the available circuitry. A complete listing of available kit parts is shown on the last page of this document.

OPERATIONAL AMPLIFIERS

Kit 128 contains 3 general purpose PMOS input CMOS operational amplifiers featuring 6, 12, and 24 micron channel lengths. The amplifiers have externally adjustable frequency compensation and operating currents, and may also be used in analog comparator applications.

Kit 124 contains 3 general purpose NMOS input CMOS operational amplifiers featuring 6, 12 and 24 micron channel lengths. The amplifiers have externally adjustable frequency compensation and operating currents and may also be used in analog comparator applications.

COMPARATOR

Kit 506 contains 4 analog comparators, two with PMOS inputs and 2 with NMOS inputs. All use 6 micron channel length split gate transistors to minimize input-output delay. The operating currents of each comparator is externally adjustable.

SWITCHED CAPACITOR FILTERS

Kit 614 contains low pass and high pass second order filters that operate over the range from 5Hz to 20KHz. They have a tunable corner frequency as a function of the clock. When placed in series, they may be used as band pass filters.

A/D AND D/A CONVERTERS

Kit 102 is an 8 bit linear and monotonic resistor string DAC with a voltage output with conversion rates up to 5MHz.

Kit 108 is a 4 bit flash A/D converter with conversion rates to 6MHz and reference string resistance of 3K ohms.

VOLTAGE CONTROLLED OSCILLATOR

Kit 604 is a linear VCO with very low temperature drift. Operating range is .01Hz to 500KHz. Only 2 pins are required for timing components.

MISCELLANEOUS

Band gap reference (Kit 609) as well as 6 micron and 12 micron N and P- channel transistors are supplied (Kits 510, 511, 626, 627) to determine MOS characteristics.

ANALOG BUILDING BLOCKS

An endless variety of analog circuit elements can be realized on the USI-6000 family. The USI-6000 implementation of some of the more important analog building blocks is now discussed:

1. CMOS OPERATIONAL AMPLIFIERS

A large variety of CMOS operational amplifier designs are possible using the 4, 6, 12 and 24 micron channel length separated gate MOS transistors. For applications requiring large bandwidths and high speed, 4 and 6 micron channel length transistors should be used. Two stage designs with a gain-bandwidth of up to 6 MHZ are achievable with these transistors. The most commonly used layout configuration uses the 12 micron channel length transistors. These transistors provide a moderate gain-bandwidth (up to 2.5 MHZ for a two stage design) and good DC performance specifications. Examples of two such layouts appear in Figure 2. The layout of Figure 2a requires just two 12 micron analog cells and is the most commonly used CMOS operational amplifier layout. This layout is limited to applications where a worst case VOS of 14 millivolts is acceptable. To achieve lower offset voltages without the use of auto-zeroing techniques, cross-coupling of the input differential pair and resistive source degeneration of the active current mirror loads is incorporated in the layout (see Figure 2b). Such a layout achieves a typical VOS of 2 millivolts and a worst case of 6 millivolts.

Noise performance of operational amplifiers configured on the USI-6000 family is an order of magnitude better than anything achievable on the older metal-gate arrays. This improvement is due to both process improvements and optimization of the basic uncommitted transistors for analog performance. Figure 3 graphically depicts this improvement. The response of a metal gate CMOS operational amplifier to a 50 microvolt test signal is contrasted to the silicon gate USI-6001 (12u and 24u analog cell) CMOS operational amplifier. Note that the test signal is completely lost in the noise on the metal-gate operational amplifier, but appears with good signal to noise ratio on the USI-6001 operational amplifiers.

Another major advantage of the silicon-gate process over the metal-gate process concerns threshold drift. With applied voltages, metal-gate transistor thresholds are observed to change many millivolts over extended periods of time. For analog differential comparator applications, the input stage transistors usually sit at different voltage levels and thus the comparator's trip point will change somewhat over time. This potential drift problem does not occur in the USI-6000 silicon-gate process.

Table 1 gives a breakdown summary of the quantities of available components on each member of the USI-6000 family. The transistors are quantized in terms of cells. Each cell contains an equal number of NMOS and PMOS transistors:

CELL TYPE	AVERAGE NUMBER OF TRANSISTORS PER CELL
1. Digital core cells	2.5
2. L = 4u split-gate cells	2.5
3. L-6u split-gate cells	2.5
4. L = 12u split-gate cells	4
5. L = 24u split-gate cells	4

This guide is particularly useful in determining which array a particular design is best suited for. A die photo of the USI-6001 showing locations of the available components appears in Figure 1.

FAMILY MEMBER	DIGITAL CORE CELLS	DEDICATED D FLIP FLOPS	L = 4u ANALOG DIGITAL CELLS	L = 6u ANALOG DIGITAL CELLS	L = 12u ANALOG DIGITAL CELLS	L = 24u ANALOG DIGITAL CELLS	4u SWITCH CELLS
6001	236	32	0	60	24	12	16
6003	160	0	64	32	64	8	50
6004	304	40	128	66	40	4	52
6005	80	0	80	68	16	0	16
6006	0	0	88	44	40	0	40

FAMILY MEMBER	P-WELL RESISTORS Meg Ohm	ZENER DIODES	Hi-Z TRANSISTER PAIRS	MOS CAPACITOR UNITS 1 UNIT = .75 pf	BOND PADS	DIE SIZE
6001	3.6	2	4	160	42	.138x.195
6003	8.9	2	1	986	46	.191x.202
6004	5.8	4	4	512	62	.215x.217
6005	3.3	2	2	156	39	.133x.154
6006	5.4	2	2	528	40	.136x.102

USI-6000 ARRAY FAMILY
TABLE 1: AVAILABLE COMPONENTS

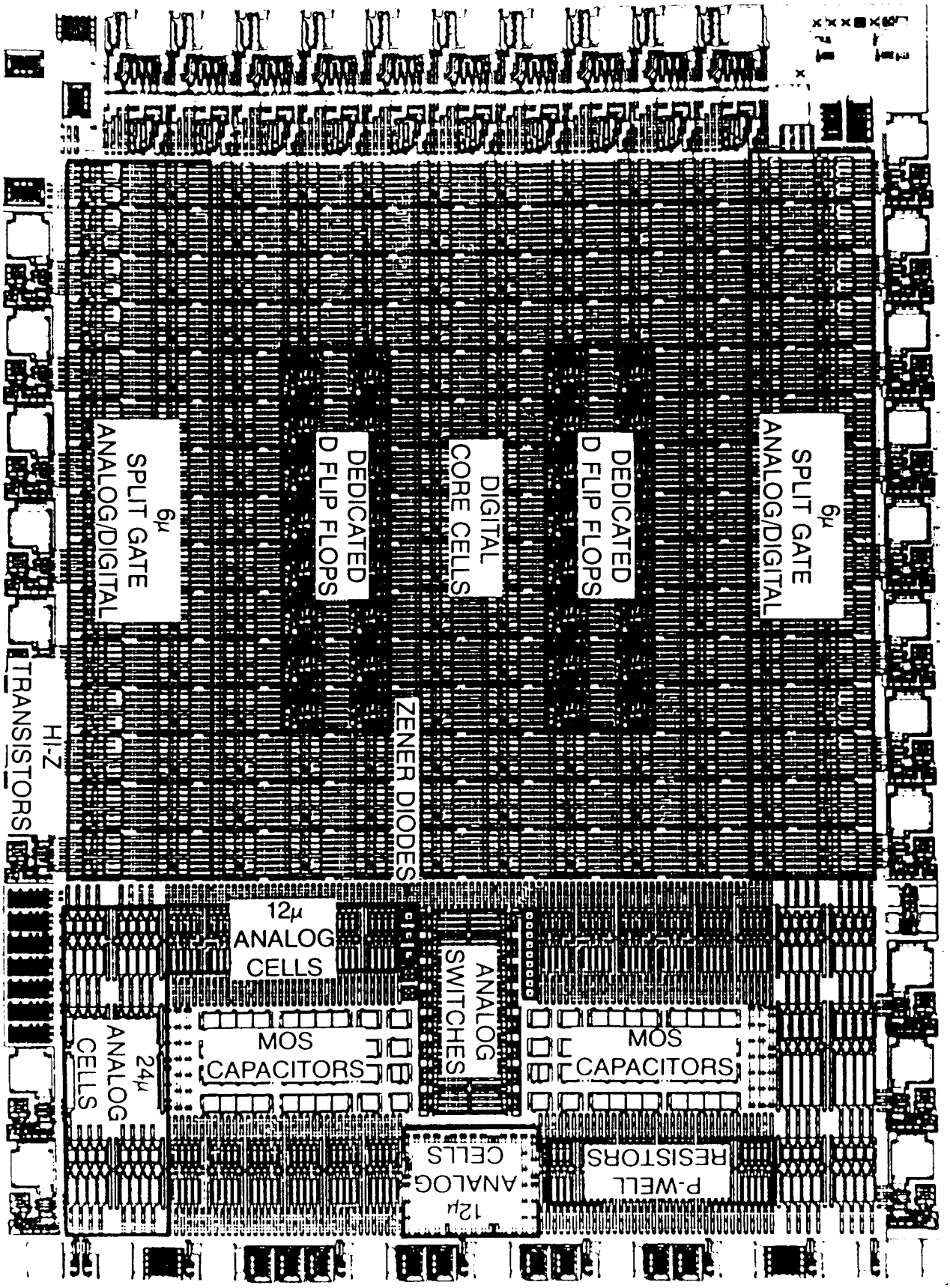
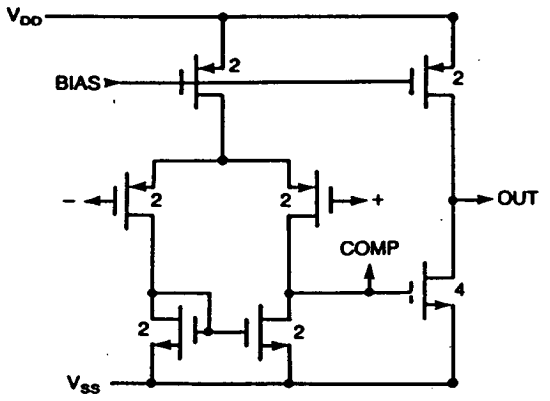
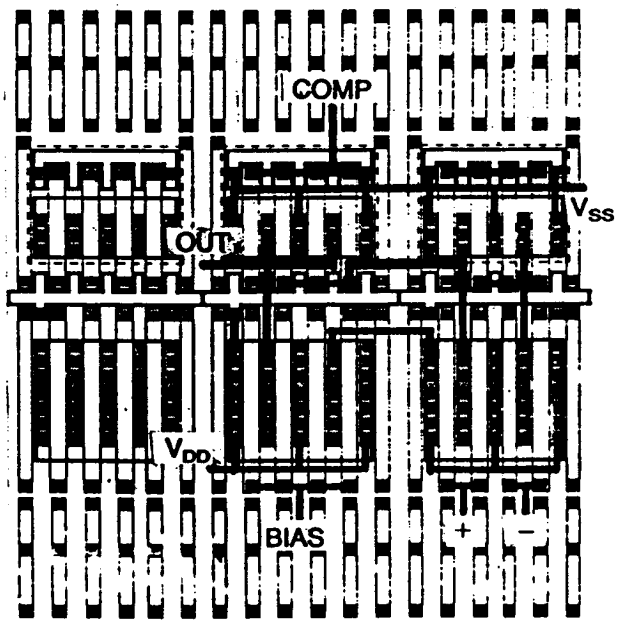


FIGURE 1

SIMPLE CMOS OP-AMP

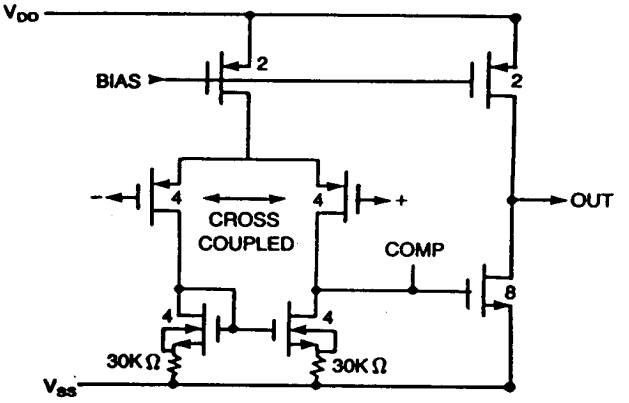


WORST CASE
V_{OS}=14mV

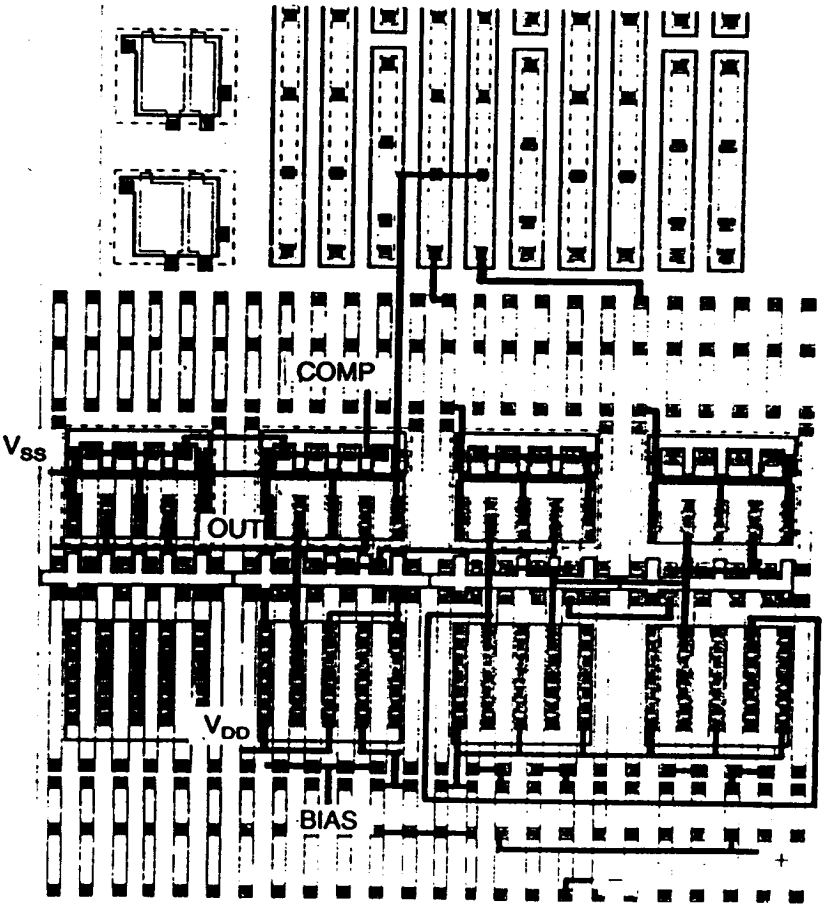


2a

CROSS-COUPLED
CMOS OP-AMP WITH
RESISTOR SOURCE DEGENERATION



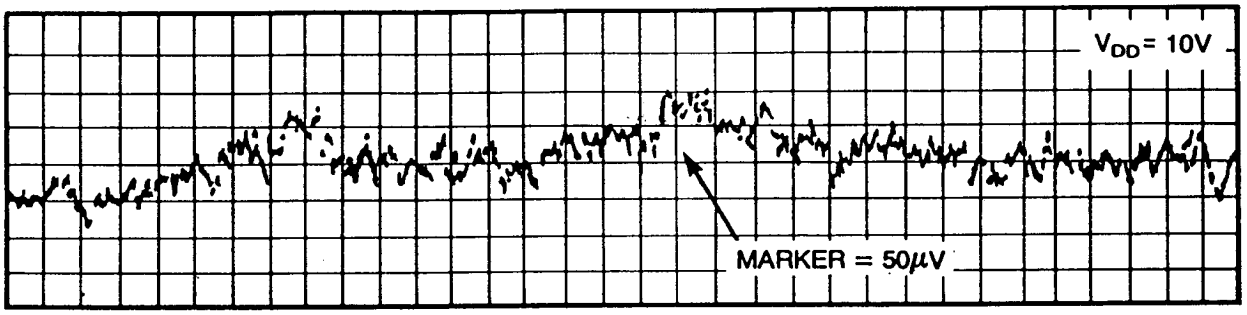
WORST CASE
V_{OS}=6mV



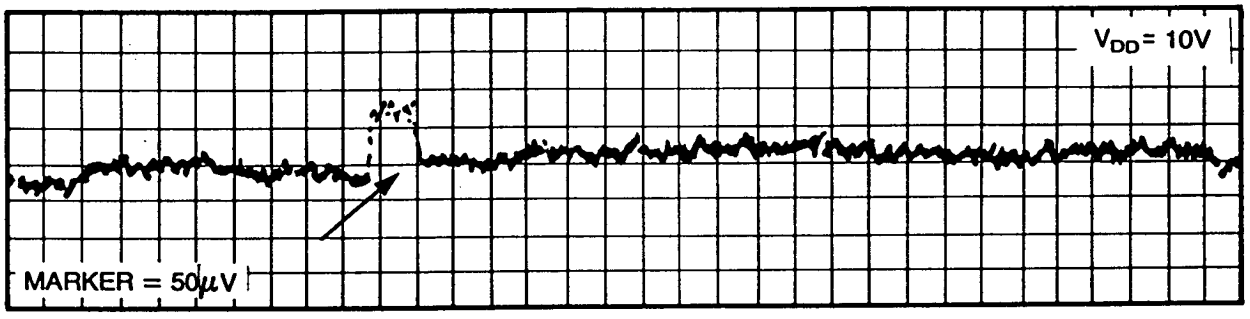
2b

FIGURE 2

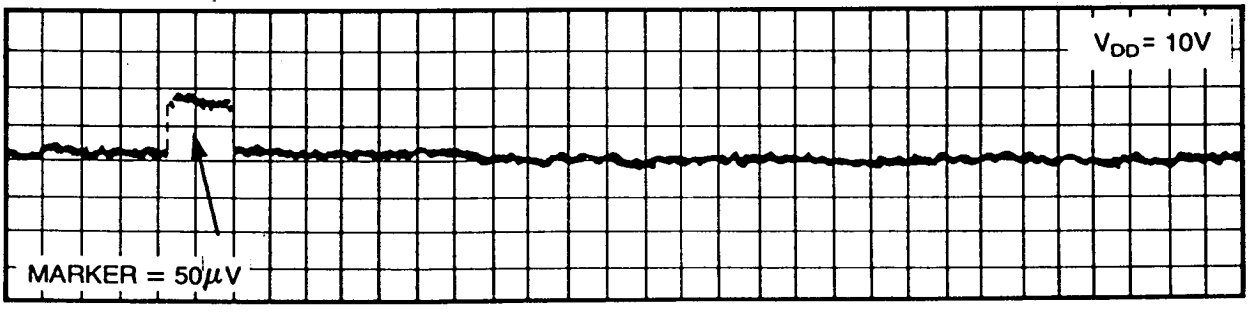
CMOS OPERATIONAL AMPLIFIER NOISE PERFORMANCE



METAL GATE CMOS OP-AMP



SILICON GATE CMOS OP-AMP



SILICON GATE CMOS OP-AMP

FIGURE 3

2. 8 BIT DAC (VOLTAGE OUTPUT)

The circuit of Figure 4 shows the electrical schematic of an 8 bit resistor string DAC which is also available as a standard kit part (Kit 10). The layout is extremely compact and requires just 62 cells to implement (24 4u core cells, 38 split-gate 6u cells).

Each polysilicon resistor R carries a voltage (+REF - (-REF))/16. These 16 levels are each subdivided into 16 additional levels by action of the 14 "on" analog transmission gates and 2 poly select analog transmission gates. For example, subdivision of the poly resistor nearest to -REF is accomplished by selecting (turning "on") only the two poly-select analog transmission gates controlled by Ho. A string of 16 identical analog transmission gates now shunts this polysilicon resistor. Each tap point of this string is gated to the DAC output by the 16 to 1 demultiplexor controlled by the four lower order bits.

Because of this shunting action, the resistance R must be much less than 16Rt (where Rt is the resistance of a single 6u split-gate transmission gate) if full 1/2 LSB linearity is to be maintained. In practice, this is guaranteed up to supply voltages of 15 volts if a single 6u split-gate cell is used for the analog transmission gates and two polysilicon cross-unders (less than 400 ohms) is the maximum resistance used for R. To maintain full linearity, the matching of polysilicon resistors must also match to better than +/- 1/2 LSB. An 8 bit converter requires matching to .2 percent. The USI-6000 process uses a plasma etching techniques for the polysilicon resistors. This results in matching which is consistently better than .2 percent.

The monotonicity of this type of converter is always guaranteed by Ohms Law regardless of the relative impedance values of the polysilicon resistors to the 6u analog transmission gates or the matching of the polysilicon resistors. For this reason, the design technique may be extended to more than 8 bits if monotonicity is the only important parameter.

Maximum frequency of operation tends to be limited by the settling time plus slew rate of the output buffer operational amplifier. This in turn depends upon the voltage difference between +REF and -REF. This limitation usually results in a conversion rate limitation of a few hundred kilohertz. Assuming no capacitive output loading, the resistor string itself is capable of conversion rates in excess of 5MHZ.

By making the polysilicon resistor values unequal, a piecewise non- linear DAC with any arbitrary shape can be generated. This is particularly useful in control applications where a non-linear sensor is used. Additionally, this DAC in conjunction with a digital successive approximation register and an analog comparator form a very useful 8 bit ADC.

3. MICROPOWER BANDGAP REFERENCE

The CMOS micropower bandgap voltage reference schematic and layout of Figure 5 is shown as an illustrative example of a typical analog building block and its USI-6000 realization. The entire reference which draws just 7ua requires no external components.

Q101-Q102, Q1-Q2 form a current regulator. The reference current in NMOS transistor Q1 is set up by the voltage drop across the bipolar transistor QN1 divided by 520K p-well referenced resistor. QN1 is formed by a peripheral NMOS transistor which as with all NMOS peripherals is in its own isolated p-well. This reference current sets the quiescent operating current to the reference operational amplifier at about 1ua and would also be used as a current bias reference to bias any other functions on the final IC. The leakage in large NMOS transistor Q3 assures start-up of the current reference.

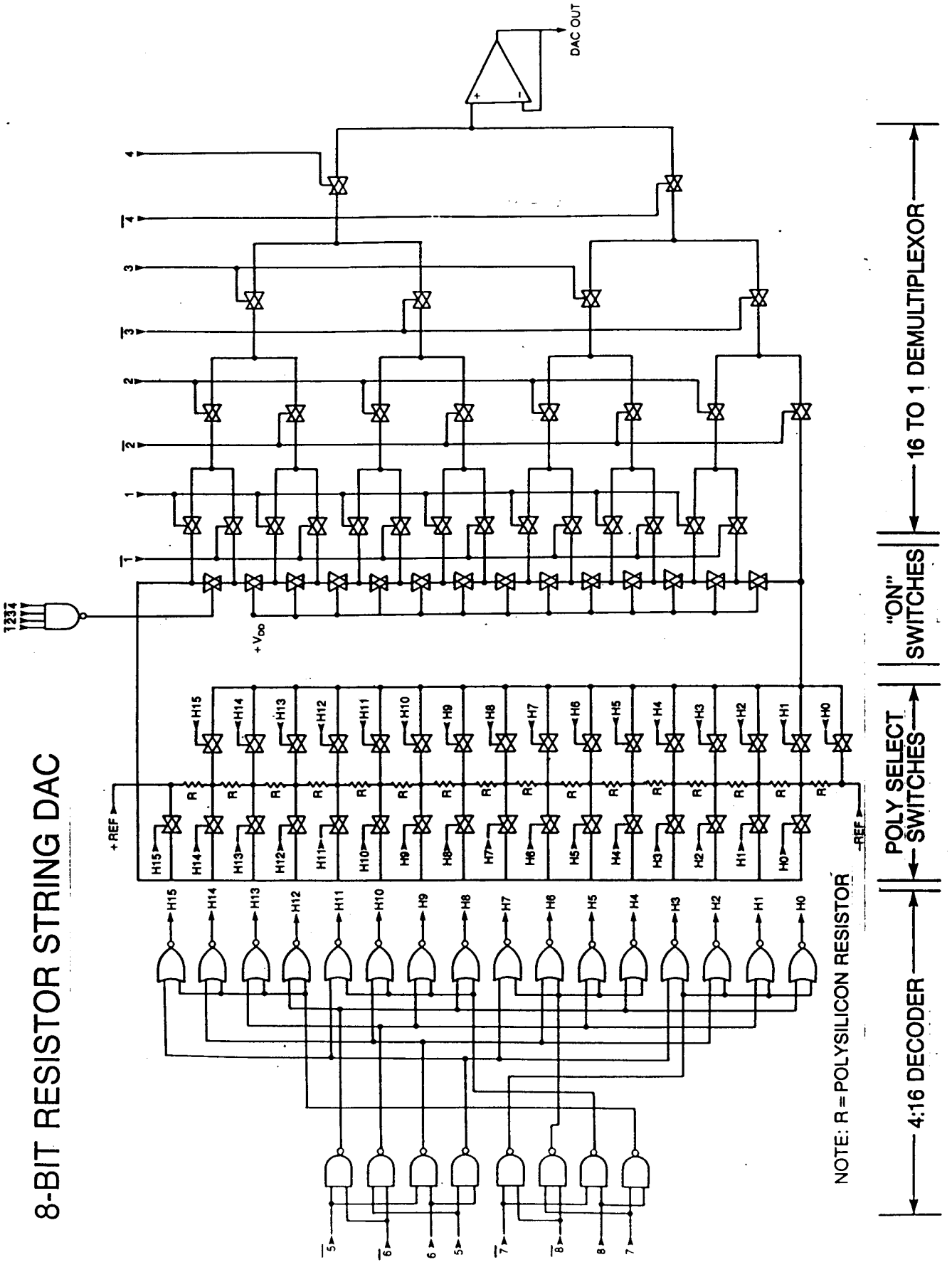
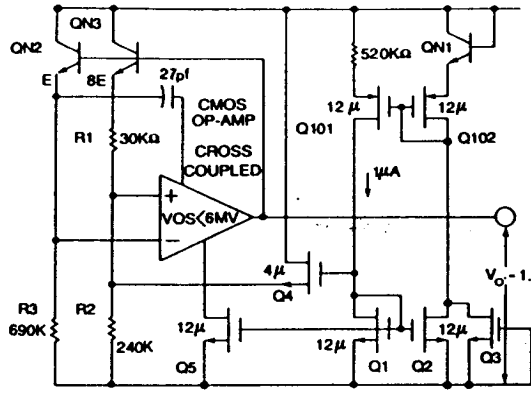
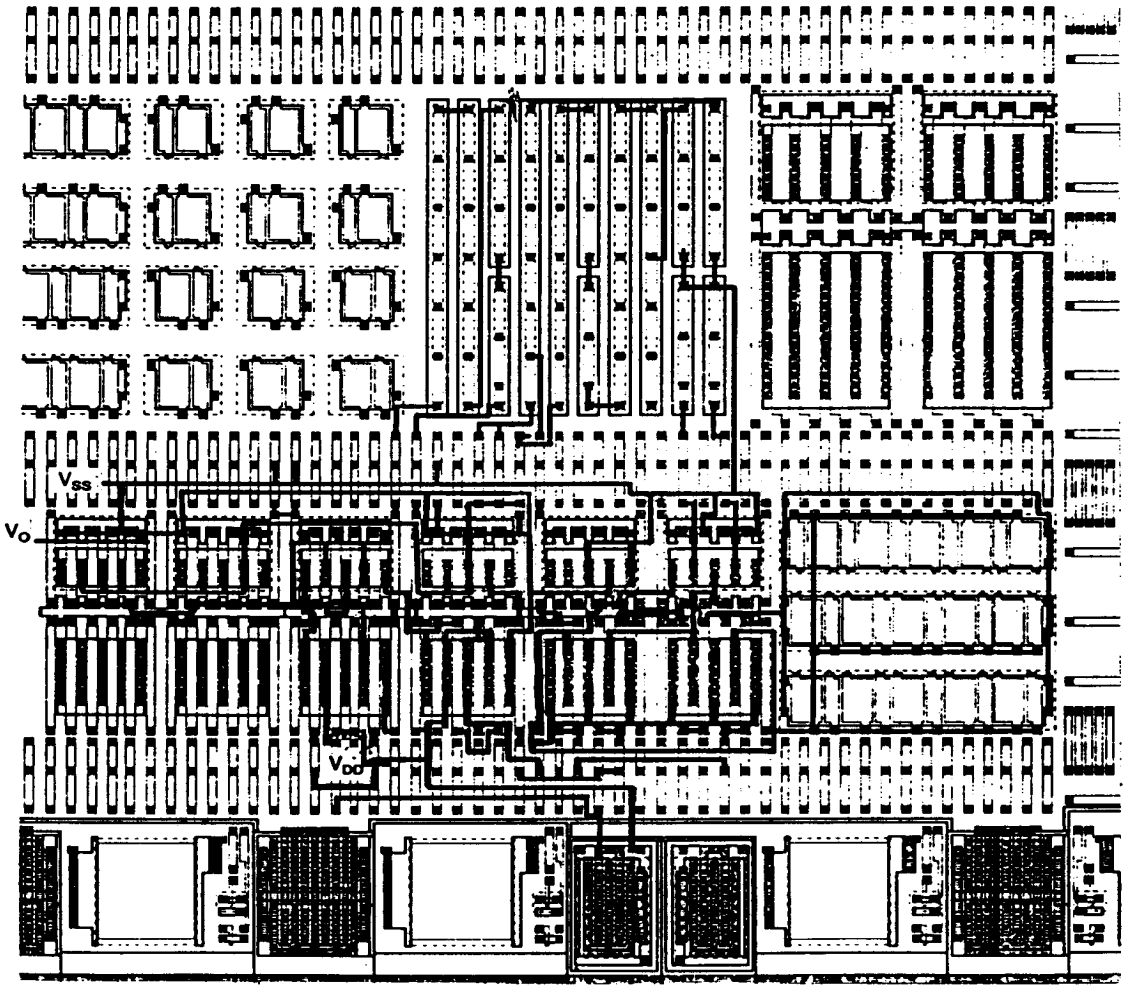


FIGURE 4

MICROPOWER BANDGAP REFERENCE



SCHEMATIC



LAYOUT ON 6004

FIGURE 5

A cross-coupled PMOS input operational amplifier (see Figure 2b) is used as the voltage reference amplifier. The emitter current density difference in multiple emitter structure QN2, QN3 results in a voltage Vrl = (KT/q) 1n (8x690/240) + VOS across resistor R1. VOS is the collective offset voltage of the reference amplifier (6mV worst case) and QN2, QN3, (2mV worst case). VR1 = .075V + VOS. Note that the multiple emitter transistor QN2, QN3 is formed by using the sources of the NMOS transistors in a 12u split-gate analog cell as the matched emitter fingers. The voltage VR1 is multiplied by the ratio R2/R1 and when added to the base to emitter voltage of QN2 produces a temperature stable 1.25V at the reference output. The reference amplifier is unity gain stabilized by 30pf (20 units) of internal MOS capacitance. The 4u channel length peripheral NMOS transistor Q4 serves to start up the voltage reference. This transistor by virtue of its short channel length, has approximately a .150V lower threshold voltage than the 12u transistor Q1. If the reference fails to start-up Q4 will inject a slightly positive voltage with respect to ground on the non-inverting input of the reference amplifier. This forces the output of the reference amplifier to go positive. Once QN2 and QN3 become active, the circuit pops into regulation. The worst case output voltage variation with respect to the ideal 1.25 volts considering unit to unit matching variations, is +/-85mV. Of this total, +/-20mV is due to the absolute value of the base to emitter voltage of QN3 and +/- 65mV is caused by individual transistor offset voltages. This error results in a worst case temperature coefficient of +/-250 parts per million per degree C.

4. HIGH SPEED STROBED COMPARATOR

The comparator shown in Figure 6 offers extremely fast differential voltage comparisons under control of a digital clock input. This comparator is available as one of the comparators in Kit Part, 506. In this kit part, the 6u split-gate transistors and 4u digital core cells are used exclusively in the layout so as to maximize the conversion speed. Conversion times of 50 nanoseconds can be achieved with this technique on the array.

High speed is achieved by the use of local positive feedback in the input differential gain stage formed by Q1 and Q2 with active loads Q101 and Q102. With the clock input low, Q103 and Q104 are "on" forcing nodes N1 and N2 to VDD. Q9 is also "on" causing the input to inverter I1 to be low.

When the clock undergoes a positive transition, Q103, Q104, and Q9 turn "off". The bias current ID1 + ID4 discharges node N1 towards VSS while the bias current ID2 + ID7 discharges node N2 towards VSS. The capacitance of each of these nodes is matched on the layout.

Whichever of the two nodes, N1 or N2 discharges to a voltage level VDD- VTP first causes the load transistor (Q101 or Q102) whose drain is on the slowest node to begin conduction. This reduces the discharge rate on this node. Both nodes continue discharging towards VSS at increasingly more unequal rates until the voltage on the fastest discharge node reaches a critical level where the positive feedback caused by the load transistors has enough loop gain to latch. The actual voltage at which this occurs depends on the bias currents. Q4 and Q7 assure that the output will hold its final state until the next reset command, even if the input voltages change radically after the conversion is complete.

The output of the input stage at N2 is taken single sided to a second gain stage consisting of common source PMOS transistor Q106 with current source load Q8. Common source transistor Q106 with current source load Q5 acting as a dummy load to node N1 to insure that nodes N1 and N2 will match in capacitance.

The conversion rates of this comparator are at least 5 times faster than a similar design attempted on the first generation metal-gate arrays. Finally, it must be noted that the layout of this comparator uses the same transistor cell types used to configure the 8 bit resistor string DAC as previously discussed. This points out the tremendous flexibility of this approach where design is accomplished at the transistor level.

5. SWITCHED CAPACITOR BUILDING BLOCKS

Switched capacitor sampled data analog building blocks have begun to appear in standard and full custom MOS integrated circuits. The USI- 6000 series is the first truly general purpose semi-custom array to offer the necessary elements required to implement this important class of functions. The necessary ingredients which exist in varying quantities in each member of the USI-6000 family are:

1. Analog switches
2. Clock logic
3. Operational amplifiers
4. Matched MOS capacitors

As a simple example, consider a typical pulse width demodulator (Figure 7) which consists of a peak detector, a low pass filter and a threshold detector.

In the classical approach, the low pass filter would be formed by an external trimmed resistor R and capacitor C to yield a decay time constant T = RC. In the switched capacitor approach, the resistor is replaced by a capacitor C2 which has its non-grounded node switched between the capacitor C1 and ground by a non-overlapping clock (break before make) set at a frequency f0 On each clock cycle C2 removes a discrete packet of charge which is proportional to the initial voltage on C1 and the value of C2.

C2 behaves like a bleed resistor of value R = 1/C2f0. The decay time constant is therefore T = (C1/C2) 1/F0. T is a function of the ratio of two on-chip capacitors (C1/C2) and f0. If f0 is generated by a crystal oscillator then the time constant T can be generated extremely accurately without the use of any external components or trimming. This represents a major manufacturing advantage for the integrated circuit user.

A more complex class of functions involves the replacement of active RC filters by switched capacitor filters. Figures 8 and 9 show the schematic and photomicrograph of a test bandpass filter that was built and evaluated on the USI-6001. The filter was modeled after an active RC bi-quad configuration. The photomicrograph shows the location of the major circuit elements which make up the filter.

The test circuit was designed for a Q of 20 and a passband voltage gain of unity. The filter worked well over the clock sample frequency spectrum of 10Hz to 500KHz. Distributional measurements on a sample of 75 test filters showed that the Q was always within 1 percent and the center frequency was within .3 percent of their respective theoretical values. This data indicates that the worst case mismatch of two unit capacitors is about +/- .3%.

The ability to implement switched capacitor functions on the USI-6000 family represents a major step forward in the evolution of combinational analog/digital CMOS gate arrays.

6. DESIGN EXAMPLE

The chip photograph of a design integrated on the USI-6001 appears in Figure 10. The integrated circuit which was used in a battery operated infra-red proximity detector application, features the incorporation of the following circuit elements:

HIGH SPEED DIFFERENTIAL STROBED COMPARATOR

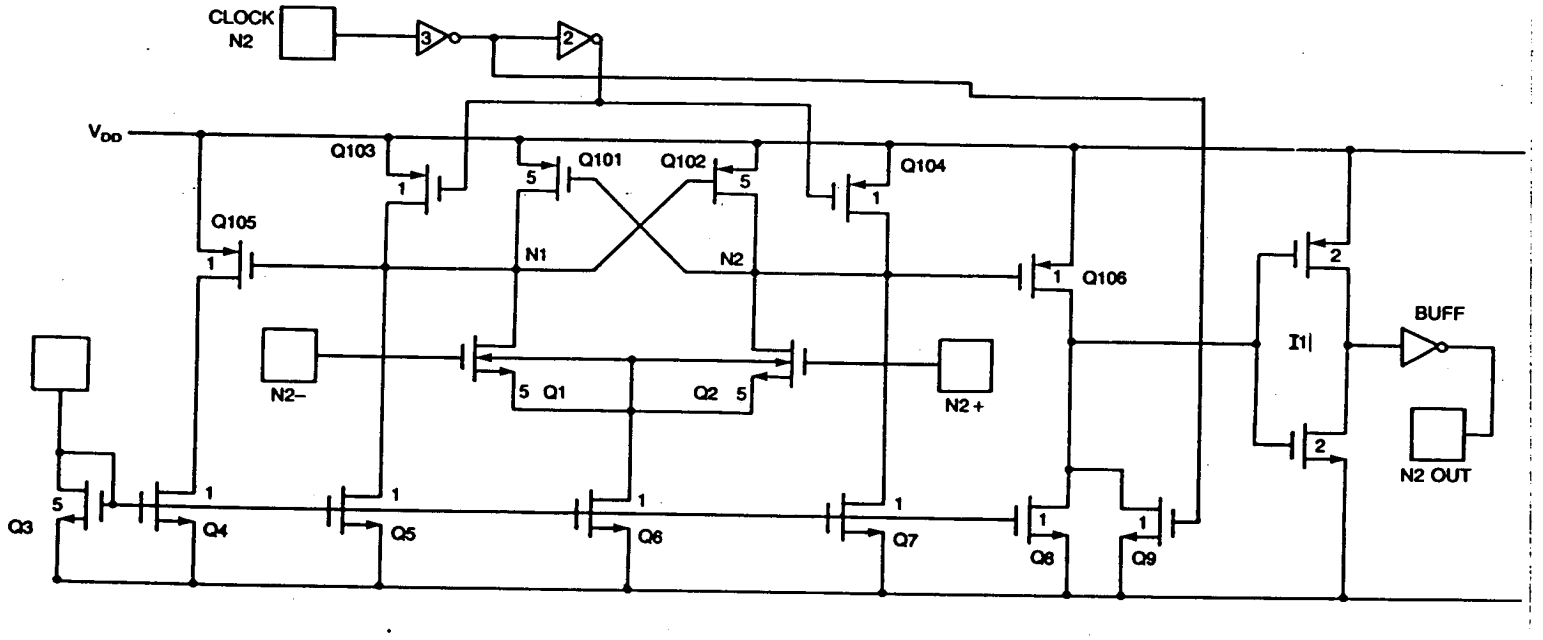
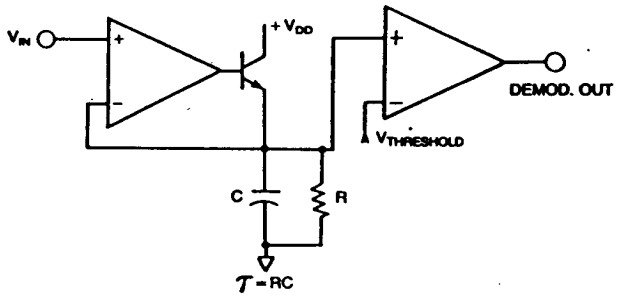


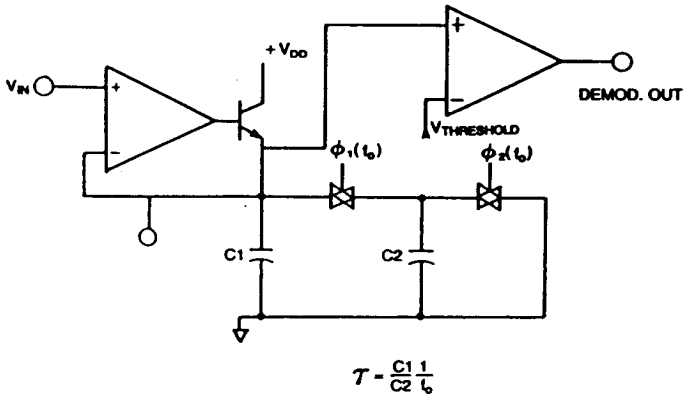
FIGURE 6

PEAK DETECTOR/DEMODULATOR

CLASSICAL RC APPROACH



SWITCHED CAPACITOR APPROACH

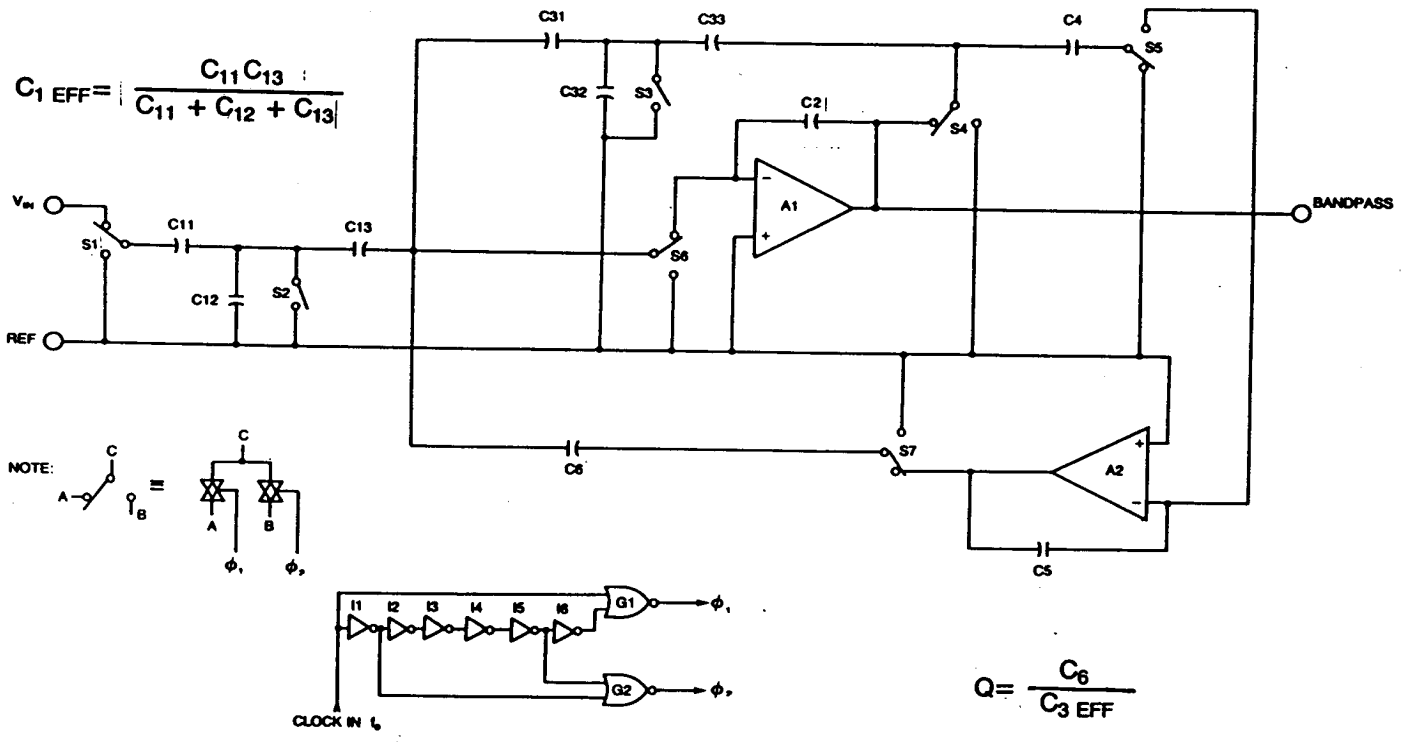


NOTE: ϕ_1, ϕ_2 ARE NON-OVERLAPPING CLOCKS, EACH INVERTED WITH RESPECT TO THE OTHER. (BREAK BEFORE MAKE).
f_o = CLOCK FREQUENCY

FIGURE 7

HI-Q BIQUAD BANDPASS FILTER

$$C_{3\,EFF} = \frac{C_{31} C_{33}}{C_{31} + C_{32} + C_{33}}$$



$$Q = \frac{C_6}{C_{3\,EFF}}$$

$$A_{VO} = \frac{C_{1\,EFF}}{C_{3\,EFF}}$$

$$f = \frac{f_o}{2\pi\sqrt{\frac{C_5 C_2}{C_6 C_4}}}$$

FIGURE 8

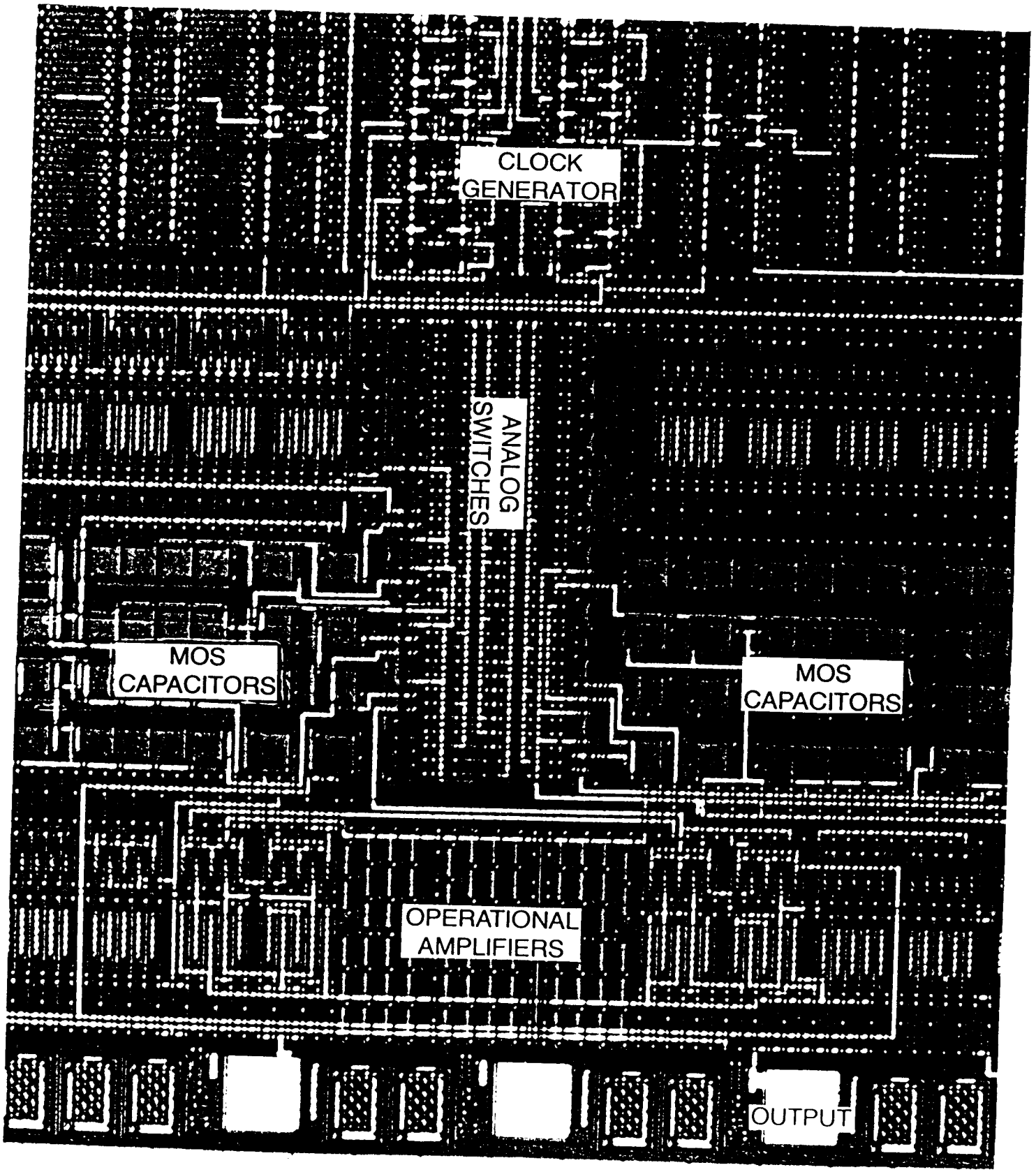


FIGURE 9

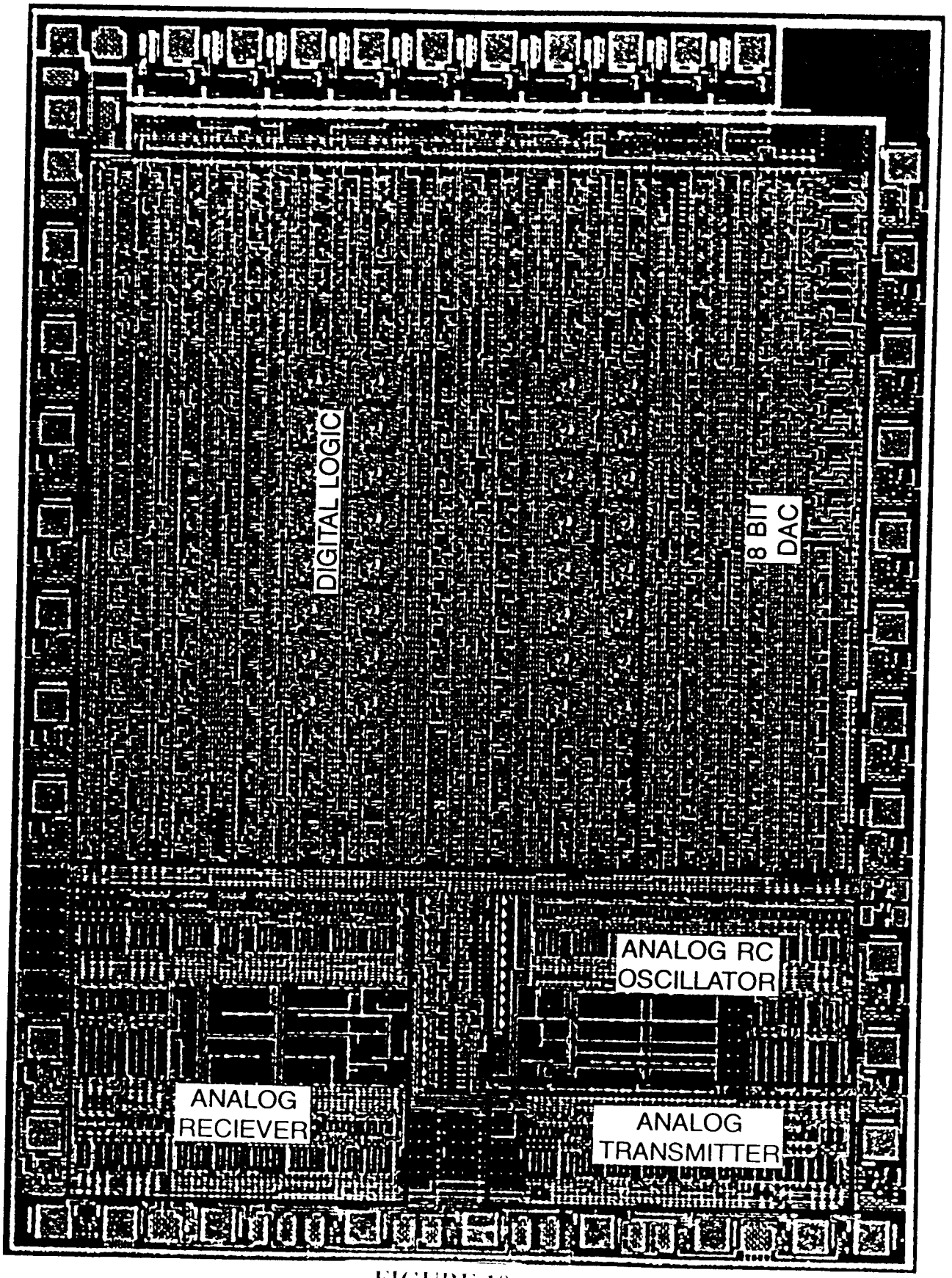


FIGURE 10