Dual Input Network Clock Generator/Synchronizer

Preliminary Technical Data

AD9549

FEATURES

Flexible Reference Inputs
Input frequencies 8 kHz to 750 MHz
Two reference inputs
Loss of Reference indicators
Auto and Manual Holdover modes
Auto and Manual Switchover modes
Smooth A to B phase transition on outputs
Excellent stability in holdover mode
Programmable 16+1-bit Input Divider, R
Differential HSTL Clock Output
Output frequencies to 750 MHz
Low Jitter clock doubler for frequencies > 400 MHz
Single-ended CMOS output; frequencies < 50MHz
Programmable Digital Loop Filter (< 1 Hz to ~100 kHz)
High Speed Digitally Controlled Oscillator (DCO) core
DDS with integrated 14 bit DAC
Excellent Dynamic Performance
Programmable 16+1-bit Feedback Divider, S
Software controlled power-down
64-lead LFCSP package

APPLICATIONS

Network Synchronization
Reference Clock Jitter Cleanup
SONET/SDH Clocks up to OC-192, Including FEC
Stratum 3/3E Reference Clocks
Wireless Base Stations, Controllers
Cable Infrastructure
Data Communications

GENERAL DESCRIPTION

The AD9549 provides synchronization for many systems including synchronous optical networks (SONET/SDH). The AD9549 generates an output clock, synchronized to one of two external input references. The external references may contain significant time jitter, also specified as phase noise. Using a digitally controlled loop and holdover circuitry, the AD9549 continues to generate a clean (low jitter), valid output clock during a 'loss of reference' condition, even when both references have failed.

The AD9549 operates over an industrial temperature range, spanning -40°C to +85°C.

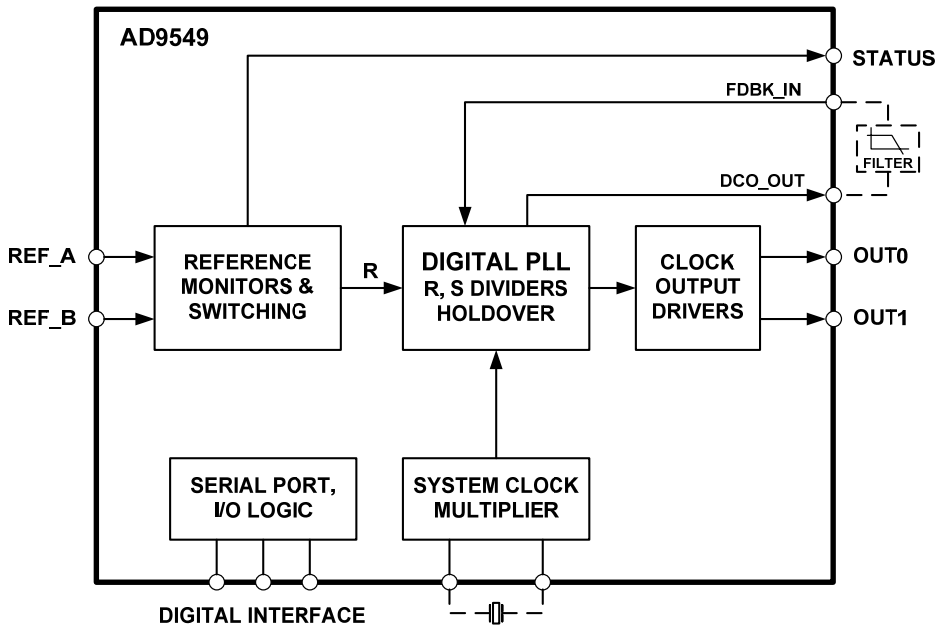

Figure 1: Basic Block Diagram

Rev. PrB

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SAMPLE APPLICATION CIRCUIT

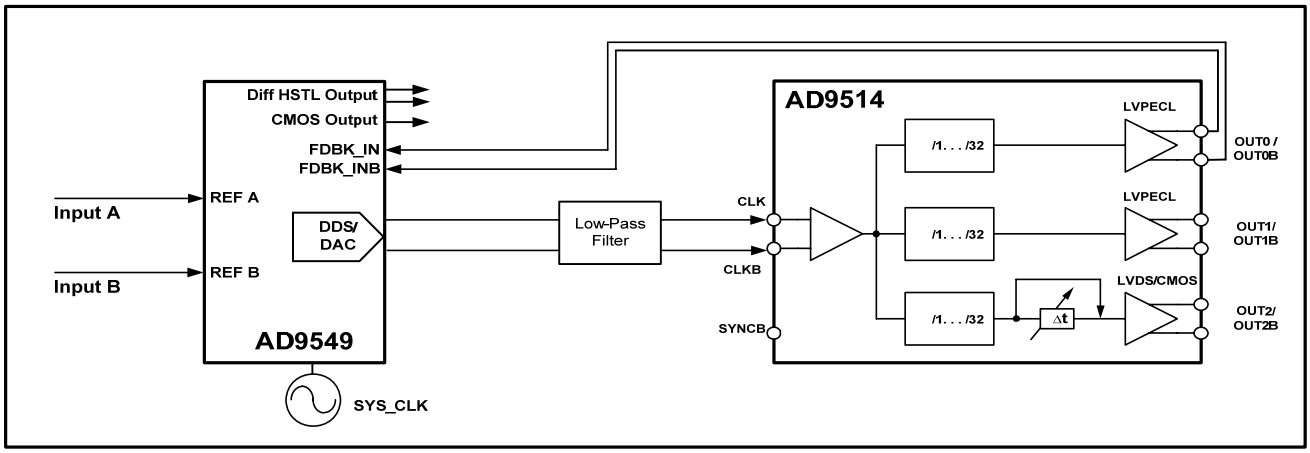


Figure 2: AD9549 + AD9514 Precision Clock Distribution Circuit

Features:

Input Frequencies Down to 8 kHz. Output Frequencies Up to 400 MHz.

Programmable Loop Bandwidth Down to < 1 Hz

Automatic Redundant Clock Switchover with User Selectable Rate of Phase Adjustment.

Automatic Stratum 2/3/3E Clock Holdover, Depending on Configuration.

Phase Noise (Fc=122.3 MHz & 100 Hz loop BW): 100 Hz offset: -107 dBc/Hz. 1 KHz offset: -142 dBc/Hz. 100 kHz offset: -157 dBc/Hz.

Two Zero-delay Outputs with Programmable Post-Divider and Synchronization.

Two Additional Outputs (non-zero delay) on AD9549.

Programmable Skew Adjustment on One AD9514 Output.

TABLE OF CONTENTS

DC SPECIFICATIONS

Unless otherwise noted, AVDD=1.8±5%, AVDD3=3.3±5%, DVDD=1.8±5%, DVDD_I/O=3.3±5%.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O (pin 1)	3.135	3.30	3.465	V	(with respect to DVSS)
DVDD (pin 3, 5, 7)	1.71	1.80	1.89	V	(with respect to DVSS)
AVDD3 (pin 14, 46, 47, 49)	3.135	3.30	3.465	V	(with respect to AVSS)
AVDD3 (pin 37)	1.71	3.30	3.465	V	(with respect to AVSS)
AVDD (pin 11,19, 23-26,29,30,36,42,44,45,53)	1.71	1.80	1.89	V	(with respect to AVSS)
SUPPLY CURRENT					
I-AVDD3 (pin 14)		6	TBD	mA	REFA, REFB Buffers
I-AVDD3 (pin 37)			TBD	mA	CMOS Output Clock Driver at 3.3V
I-AVDD3 (pin 46, 47, 49)		25	TBD	mA	DAC output current source
I-AVDD (pin 36)		8	TBD	mA	HSTL Output Clock Driver
I-AVDD (pin 42)		10	TBD	mA	FDBK
I-AVDD (pin 11)		10	TBD	mA	SYSCLK
I-AVDD (pin 19, 23-26, 29, 30, 44, 45)		170	TBD	mA	aggregate analog supply
I-AVDD (pin 53)		35	TBD	mA	DAC Power Supply
I-DVDD (pin 3, 5, 7)		200	TBD	mA	Digital Core
I-DVDD_I/O (pin 1)		3	TBD	mA	Digital I/O (varies dynamically)
LOGIC INPUTS (Except Pin 32)					Pins 56-61, 64, 9, 10, 54, 55, 63
Input High Voltage (V_{IH})	2.0			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±30	±100	µA	At Vin=0V and Vin=DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CLKMODESEL (Pin 32) LOGIC INPUT					Pin 32 only.
Input High Voltage (V_{IH})	1.4			V	
Input Low Voltage (V_{IL})			0.4	V	
Input Current (I_{INH}, I_{INL})		±30	±100	µA	At Vin=0V and Vin=DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
LOGIC OUTPUTS					Pin 62, & bi-dir. pins 9, 10, 54, 55, 63
Output High Voltage (V_{OH})	2.7			V	I_{OH} = 1 mA w/ V_{OH} =DVDD_I/O-0.4V
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1mA w/ V_{OL} =0.4V
REFERENCE INPUTS					Pins 12, 13, 15, 16
Input Capacitance		3		pF	
Input Resistance		16		KΩ	Differential at Vbias=AVDD3-800mV
Common Mode Input Voltage[1]				V	differential operation
Differential Input Voltage Swing[1]				mV	differential operation
Input Voltage High (V_{IH})				V	single-ended operation
Input Voltage Low (V_{IL})				V	single-ended operation
Input Current				mA	single-ended operation
Internal Bias Voltage	AVDD3-1600	AVDD3-800	AVDD3-400	mV	programmable (see text)
FDBK INPUT					Pins 40, 41
Input Capacitance		3		pF	
Input Resistance		30		KΩ	Differential
Common Mode Input Voltage[2]				V	differential operation
Differential Input Voltage Swing[2]				mV	differential operation

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK INPUT					
SysClk PLL Bypassed					
Input Capacitance (DC)		1.5		pF	single-ended, each pin
Input Impedance (DC)		1		KΩ	differential
Common Mode Input Voltage[3]					differential operation
Differential Input Voltage Swing[3]					differential operation
Input Voltage High (V_{IH})					single-ended operation
Input Voltage Low (V_{IL})					single-ended operation
Input Current					single-ended operation
SysClk PLL Enabled					
Input Capacitance (DC)		3		pF	single-ended, each pin
Input Impedance (DC)		2		KΩ	differential
Common Mode Input Voltage[3]					differential operation
Differential Input Voltage Swing[3]					differential operation
Input Voltage High (V_{IH})					single-ended operation
Input Voltage Low (V_{IL})					single-ended operation
Input Current					single-ended operation
Crystal Resonator with SysClk PLL Enabled					
Motional Resistance				kΩ	
CLOCK OUTPUT DRIVERS					
HSTL Output Driver					
Differential Output Voltage Swing[4]	TBD	700		mV	Both pins AC-coupled using 0.01uF, then 50Ω to GND,
Common Mode Output Voltage[4]	TBD	0.9		V	
Continuous Output Current		7.2		mA	
CMOS Output Driver					
Output Voltage High (V_{OH})				V	
Output Voltage Low (V_{OL})			0.4	V	
Output High Current (I_{OH})				µA	
Output Low Current (I_{OL})				µA	
TOTAL POWER DISSIPATION					
All Blocks Running		TBD	TBD	mW	TBD
Power-Down Mode		TBD	TBD	mW	Using either the Power Down Register or PWRDOWN pin.
Default with SysClk PLL Enabled		TBD	TBD	mW	After reset or power up with f_S=1GHz, S4=0, S1-S3=1, f_{SYSCLK}=25MHz
Default with SysClk PLL Disabled		TBD	TBD	mW	After reset or power up with f_S=1GHz, S4-S4=1, & Sysclk PLL powered down.
- with Digital Power Down			TBD	mW	
- with REFA or REFB Power Down			TBD	mW	One reference still powered up.
- with HSTL Clock Driver Power Down			TBD	mW	
- with CMOS Clock Driver Power Down			TBD	mW	
- with HSTL 2x Freq. Multiplier Power Down			TBD	mW	

[1] Must be ≤ 0V relative to AVDD3 (pin 14) and ≥ 0V relative to AVSS (pins 33, 43).
[2] Must be ≤ 0V relative to AVDD (pin 42) and ≥ 0V relative to AVSS (pins 33, 43).
[3] Relative to AVSS (pins 33, 43).
[4] Must be ≤ 0V relative to AVDD (pin 36) and ≥ 0V relative to AVSS (pins 33, 43).
[5] See "Power Management" Section for details about power profiles.

AC SPECIFICATIONS

Unless otherwise noted: f_S=1GHz. DAC R_{SET}=10KΩ. Power supply pins within the range specified in "DC SPECIFICATIONS."

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS					Pins 12, 13, 15, 16
Frequency Range	.008		750	MHz	
Minimum Slew Rate				V/ns	
Minimum Pulse Width High				ps	
Minimum Pulse Width Low				ps	
FDBK INPUT					Pins 40, 41
Input Frequency Range	.008		750	MHz	sinusoidal (without degrading phase noise performance)
Minimum Slew Rate				V/ns	
Minimum Differential Input Level				V	peak-to-peak (xxxdBm into 50Ω)
SYSTEM CLOCK INPUT					Pins 27, 28
SysClk PLL Bypassed					
Input Frequency Range	TBD		1000	MHz	
Minimum Pulse Width High				ps	
Minimum Pulse Width Low				ps	
Minimum Differential Input Level				V	peak-to-peak (xxxdBm into 50Ω)
SysClk PLL Enabled					
VCO Frequency Range – Low Band	700		850	MHz	
VCO Frequency Range – High Band	800		1000	MHz	
Maximum Input Rate of PFD			100	MHz	
Without Bipolar Edge Detector					
Input Frequency Range	TBD		TBD	MHz	
Multiplication Range	8		66		integer multiples of 2
Minimum Pulse Width High				ps	
Minimum Pulse Width Low				ps	
Minimum Differential Input Level				V	peak-to-peak (xxxdBm into 50Ω)
With Bipolar Edge Detector					
Input Frequency Range	TBD		TBD	MHz	
Multiplication Range	16		132		integer multiples of 4
Input Duty Cycle				%	
Minimum Differential Input Level				V	peak-to-peak (xxxdBm into 50Ω)
Crystal Resonator with SysClk PLL Enabled					
Crystal Resonator Frequency Range	10		40+	MHz	fundamental mode resonator
Maximum Crystal Motional Resistance		TBD			see text for recommendations
CLOCK DRIVERS					
HSTL Output Driver					
Toggle Rate	20		725	MHz	see plot for maximum toggle rate
Output Duty Cycle	48		52	%	
Output Rise/Fall Time		TBD		ps	100Ω terminated, 5pF load
JITTER (12 kHz-20 MHz)		1.0		ps	Fin=19.44 MHz, Fout=155.52 MHz. 50 MHz System Clock Input. (See Phase Noise Plots for test conditions.)
HSTL Output Driver with 2x Multiplier					
Output Frequency Range	TBD		TBD	MHz	
Duty Cycle	45		55	%	

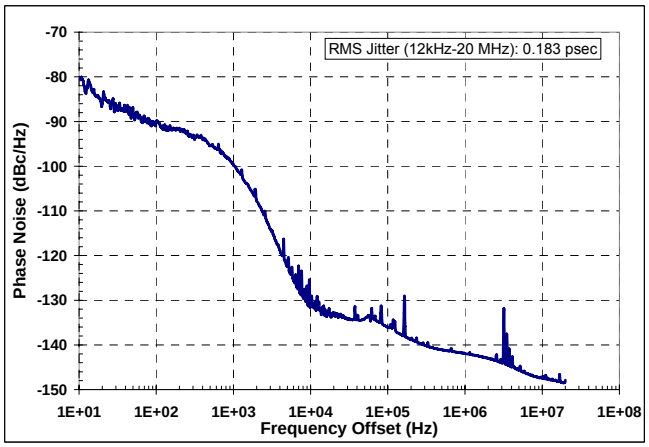
Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Sub-harmonic Spur Level		-35		dBc	without correction
JITTER (12 kHz-20 MHz)		1.1		Ps	Fin=19.44 MHz, Fout=622.08 MHz. 50 MHz System Clock Input. (See Phase Noise Plots for test conditions.)
CMOS OUTPUT DRIVER (AVDD3/PIN 37) @3.3V					
Toggle Rate			150	MHz	see plot for maximum toggle rate
Duty Cycle		**55**	**60**	%	With 20pF load and up to 250 MHz
Output Rise/Fall Time				ns	With 20pF load
JITTER (12 kHz-20 MHz)					Fin=25 MHz, Fout=50 MHz
CMOS OUTPUT DRIVER AT (AVDD3/PIN 37) @1.8V					
Toggle Rate			50	MHz	see plot for maximum toggle rate
Duty Cycle		**55**	**60**	%	With 20pF load and up to 40 MHz
Output Rise/Fall Time				ns	
JITTER (12 kHz-20 MHz)					Fin=25 MHz, Fout=50 MHz
HOLDOVER					
Frequency Accuracy (XTAL)					xxxMHz, xxxppm crystal resonator at SYSCLK pins
Variation Over Temperature range				Ppm/°C	
Variation Over Supply range				ppm/V	
Frequency Accuracy (TCXO)					TCXO at SYSCLK pins
Variation Over Temperature range			0	Ppm/°C	
Variation Over Supply range			0	ppm/V	
OUTPUT FREQUENCY SLEW LIMITER					
Slew Rate Resolution	0.54		111	Hz/sec	$P=2^{16}$ for minimum; $P=2^{5}$ for maximum
Slew Rate Range	0		$3x10^{16}$	Hz/sec	$P=2^{16}$ for minimum; $P=2^{5}$ for maximum
REFERENCE MONITORS					
LOSS OF REFERENCE MONITOR					
Operating Frequency Range	$7.63x10^{3}$		$167x10^{6}$	Hz	
Minimum Frequency Error for Continuous "REF" Present" Indication			-16	ppm	f_{REF}= 8 kHz
Minimum Frequency Error for Continuous "REF" Present" Indication			-19	%	f_{REF}= 155 MHz
Maximum Frequency Error for Continuous "REF Lost" Indication	-32			ppm	f_{REF}= 8 kHz
Maximum Frequency Error for Continuous "REF Lost" Indication	-35			%	f_{REF}= 155 MHz
REFERENCE QUALITY MONITOR					
Operating Frequency Range					
Frequency Resolution (normalized)	0.001		16	ppm	f_{REF}= 8 kHz; M=15 for minimum; M=1 for maximum (see text)
Frequency Resolution (normalized)	0.002		44.9	%	f_{REF}= 155 MHz; M=15 for minimum; M=1 for maximum (see text)
VALIDATION TIMER					
Timing range	$32x10^{-9}$		137	s	P_{IO}= 5 (see text)
Timing range	$65x10^{-6}$		$2.8x10^{5}$	s	P_{IO}= 16 (see text)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC OUTPUT CHARACTERISTICS					
DCO Frequency range (1st Nyquist zone)	10		450	MHz	DPLL loop bandwidth sets lower limit
Output Resistance		50		Ω	single-ended (each pin internally terminated to AVSS)
Output Capacitance		5		pF	
Full-Scale Output Current		10	31.7	mA	range depends on DAC RSET resistor
Gain Error	TBD		TBD	%FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVSS −0.50	+0.5V	AVSS +0.50		Outputs not DC shorted to Vss
Wideband SFDR (DC to Nyquist):					SFDR may be improved by activating *Harmonic Spur Suppression* (see text)
10MHz Analog Out		TBD		dBc	
40MHz Analog Out		TBD		dBc	
80MHz Analog Out		TBD		dBc	
120MHz Analog Out		TBD		dBc	
160MHz Analog Out		TBD		dBc	
Narrowband SFDR					
10 MHz Analog Out (±1 MHz)		TBD		dBc	
40 MHz Analog Out (±1 MHz)		TBD		dBc	
80 MHz Analog Out (±1 MHz)		TBD		dBc	
120 MHz Analog Out (±1 MHz)		TBD		dBc	
160 MHz Analog Out (±1 MHz)		TBD		dBc	
DIGITAL PLL					
Minimum open-loop bandwidth		0.0001		kHz	dependent on the frequency of REFA/B, the DAC sample rate, and the P, R, and S divider values
Maximum open-loop bandwidth		100		kHz	dependent on the frequency of REFA/B, the DAC sample rate, and the P, R, and S divider values
Minimum phase margin		10		degrees	dependent on the frequency of REFA/B, the DAC sample rate, and the P, R, and S divider values (not a hard limit but bounded by 0°)
Maximum phase margin		85		degrees	dependent on the frequency of REFA/B, the DAC sample rate, and the P, R, and S divider values (not a hard limit but bounded by 90°)
PFD input frequency range	~0.008		~24.5	MHz	
Feedforward divider ratio	1		131,070		1,2,..,65,535 or 2,4,..,131,070
Feedback divider ratio	1		131,070		1,2,..,65,535 or 2,4,..,131,070
LOCK DETECTION					
PHASE LOCK DETECTOR					
Time Threshold Programming Range	0		2097	µs	FPFD_Gain=200
Time Threshold Resolution		0.488		ps	FPFD_Gain=200
Lock Time Programming Range	$32x10^{-9}$		68.7	s	in power-of-2 steps
Unlock Time Programming Range	$64x10^{-6}$		16.8	ms	in power-of-2 steps
FREQUENCY LOCK DETECTOR					
Normalized Frequency Threshold Programming Range	0		0.0021		FPFD_Gain=200; normalized to $(f_{REF}/R)^2$; see text for details
Normalized Frequency Threshold		$5x10^{-13}$			FPFD_Gain=200; normalized to $(f_{REF}/R)^2$;

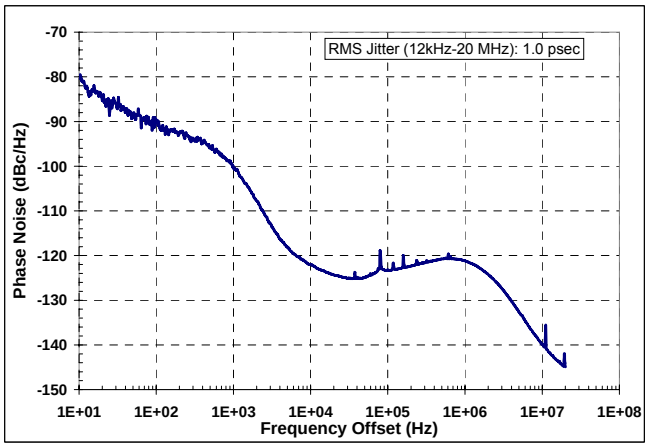
Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Programming Resolution					see text for details
Lock Time Programming Range	$32x10^{-9}$		68.7	s	in power-of-2 steps
Unlock Time Programming Range	$64x10^{-6}$		16.8	ms	in power-of-2 steps
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power Down				ns	
Time Req'd to Recover from Power Down				ns	
S0-4 Config Setup Time During Reset				ns	Time S0-4 must be present before falling edge of signal on RESET pin.
S0-4 Config Hold Time During Reset				ns	Time S0-4 must be held after falling edge of signal on RESET pin.
Reset assert to S0-4 High-Z Time				ns	Time from rising edge of RESET to High Z on S0-4 configuration pins.
Reset deassert to S0-4 Low-Z time				ns	Time from falling edge of RESET to Low-Z on S0-4 configuration pins.
CS to SCLK Setup Time	TBD			ns	
Period of SCLK	10			ns	
TDSU (Serial Data Setup Time)	TBD			ns	
TDHD (Serial Data Hold Time)	TBD			ns	
TDV (Data Valid Time)	TBD			ns	
PROPAGATION DELAY					
FDBK to HSTL Output Driver					
FDBK to HSTL Output Driver with 2x Frequency Multiplier Enabled					
FDBK to HSTL Output Driver with 2x Frequency Multiplier Enabled					
FDBK to CMOS Output Driver					
FDBK through S-Divider to CMOS Output Driver					

TYPICAL PERFORMANCE CHARACTERISTICS

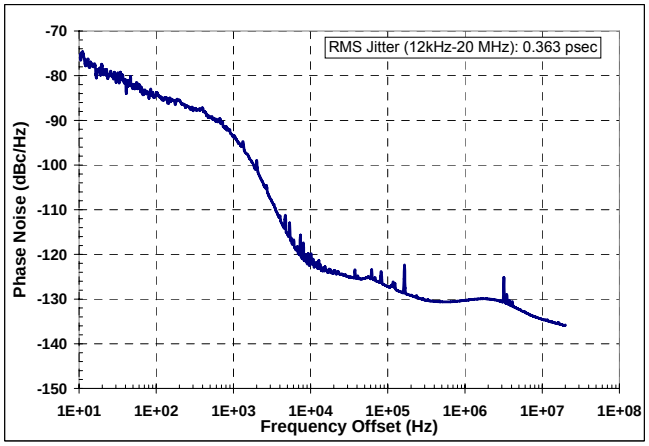
Unless otherwise noted: AVDD, AVDD3, and DVDD at nominal supply voltage; f_S= 1 GHz, DAC R_{SET}= 10kΩ.



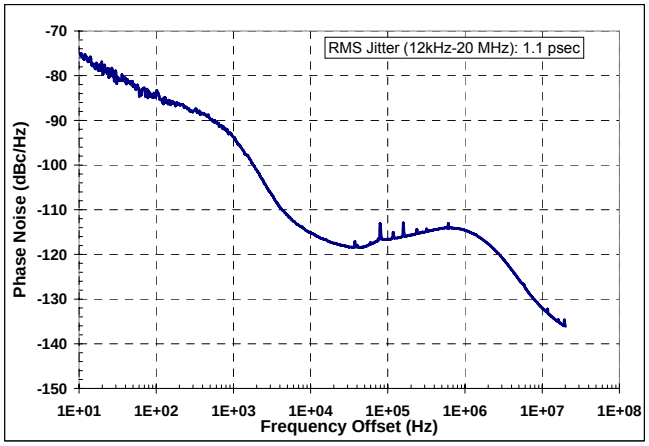
Plot 1: Additive Phase Noise at HSTL Output Driver. Sysclk=1 GHz (SysClk PLL Bypassed). Ref=19.44 MHz., Fout=311.04 MHz. DPLL loop BW= 1 kHz.



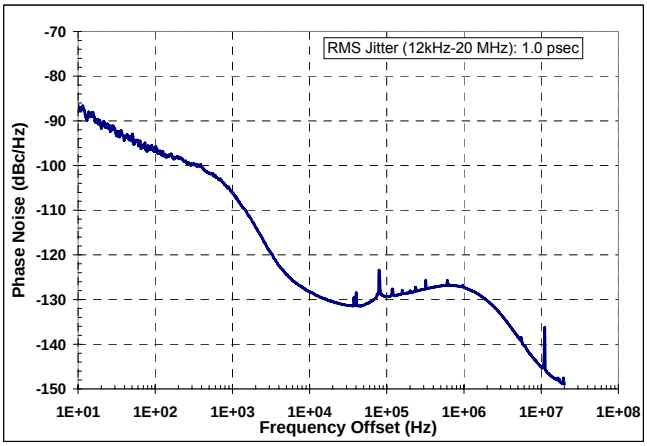
Plot 3: Additive Phase Noise at HSTL Output Driver. Sysclk = 1 GHz (SysClk PLL Enabled driven by R&S SMA100 Signal Generator at 50 MHz .Ref=19.44 MHz., Fout=311.04 MHz, DPLL loop BW= 1 kHz.



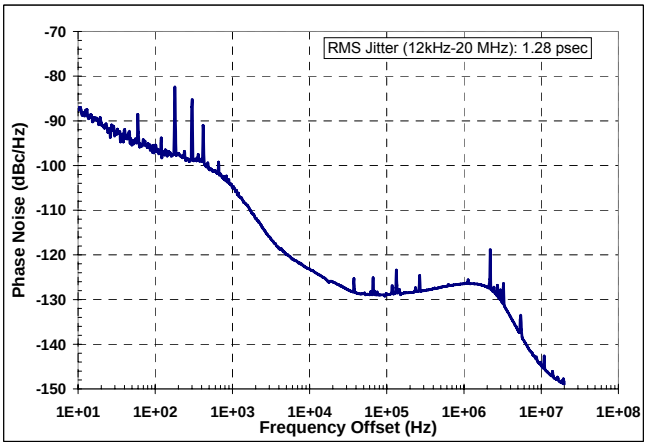
Plot 2: Additive Phase Noise at HSTL Output Driver. Sysclk=1 GHz (SysClk PLL Bypassed). Ref=19.44 MHz., Fout=622.08 MHz, DPLL loop BW= 1 kHz. HSTL Output Doubler Enabled



Plot 4: Additive Phase Noise at HSTL Output Driver. Sysclk= 1 GHz (SysClk PLL Enabled and driven by R&S SMA100 Signal Generator at 50 MHz. Fin=19.44 MHz., Fout=622.08 MHz, DPLL loop BW= 1 kHz. System Clock Doubler Enabled. HSTL Doubler Enabled.



Plot 5: Additive Phase Noise at HSTL Output Driver. Sysclk = 1 GHz. (Sysclk PLL enabled and driven by R&S SMA100 Signal Generator at 50 MHz.) Fin=19.44 MHz, Fout=155.52 MHz. System Clock Doubler Enabled. DPLL loop BW=1 kHz.



Plot 7: Additive Phase Noise at HSTL Output Driver. Sysclk = 1 GHz. (Sysclk PLL enabled and driven by a 25 MHz Fox Crystal Oscillator.) Fin=19.44 MHz, Fout=155.52 MHz. DPLL loop BW=1 kHz.

PLACE HOLDER

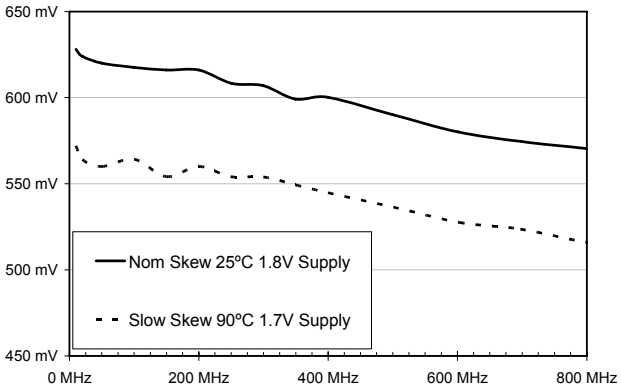
Plot 6: Additive Phase Noise at HSTL Output Driver. Sysclk = 500 MHz. Sysclk PLL disabled. Fin=8 kHz, Fout= 155.52 MHz. DPLL loop BW= 400 Hz.

PLACE HOLDER

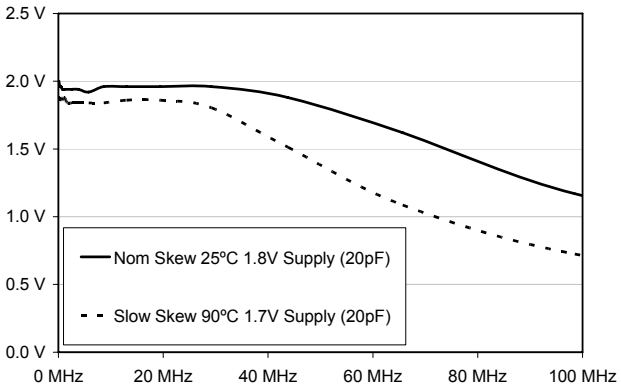
Plot 8: Additive Phase Noise at CMOS Output Driver. Sysclk= 500 MHz. Sysclk PLL disabled. Fin=10.24 MHz, Fout=10.24 MHz. DPLL loop BW=1 kHz

PLACE HOLDER

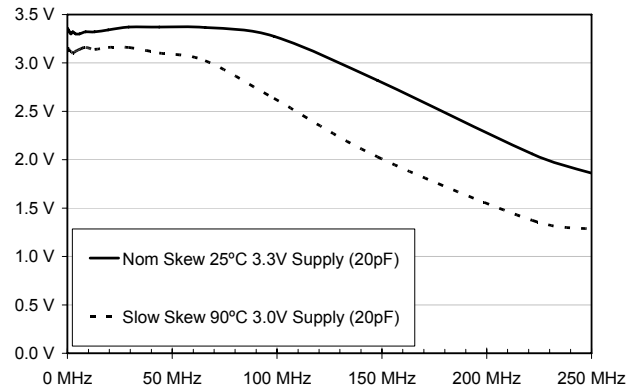
*Plot 9: SFDR vs Fout at Sysclk = 1GHz with and w/o recon filter. Fcut = Fout * 1.2*



Plot 10: HSTL Output Driver Peak-Peak Amplitude vs. Toggle Rate (100 ohms across differential pair,)



Plot 11: CMOS Output Driver Peak-Peak Amplitude vs. Toggle Rate (AVDD3 = 1.8 V) with 20 pF Load



Plot 12: CMOS Output Driver Amplitude vs. Toggle Rate (AVDD3 = 3.3 V) with 20 pF Load.

PLACE HOLDER

Plot 13: 12kHz-20mHz RMS Jitter vs System Clock PLL Frequency. Fin=19.44 MHz. Fout=155.52 MHz.

PLACE HOLDER

Plot 14: System Clock Sub-harmonic Spur Level for Typical System Clock PLL Conditions.

ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/0)	3.6 V
DAC Supply Voltage (DAC_VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to D_{VDD}_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C
Thermal Resistance[1] (Θ_{JA})	26°C/W typ.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulates on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

[1] The exposed pad on bottom of package must be soldered to ground in order to achieve the specified thermal performance.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

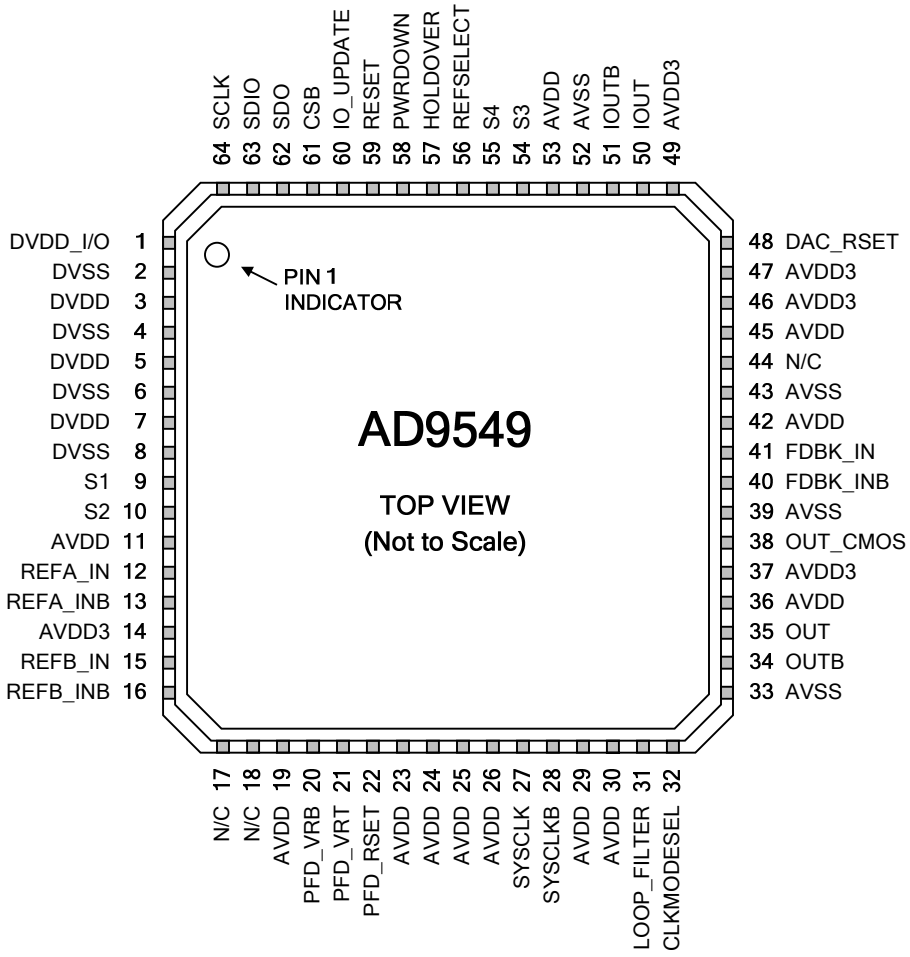


Figure 3: 64-Lead LFCSP Pin Configuration

Table 2: Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	I/O Digital Supply
2, 4, 6, 8	I	Power	DVSS	Digital Ground: Connect to Ground
3, 5, 7	I	Power	DVDD	Digital Supply
9, 10, 54, 55	I/O	3.3V CMOS	S1, S2, S3, S4	Configurable I/O pins: These pins are configured under program control (see "Status and Warnings" on Page 42., and do not have internal pull-up/pull-down resistors.
11, 19, 23-26, 29, 30, 36, 42, 45, 53	I	Power	AVDD	Analog Supply: Connect to a nominal 1.8V Supply

12	I	Diff Input	REFA_IN	Frequency/Phase Reference A Input. This internally biased input is typically AC-coupled, and when configured as such, can accept any differential signal, whose single-ended swing is between 0.4 and 3.3V. If DC-coupled, LVPECL or CMOS input is preferred.
13	I	Diff Input	REFA_INB	Complementary Frequency/Phase Reference A Input: Complementary signal to the input provided on pin 12. If using a single-ended, DC-coupled CMOS signal into REFA_IN, bypass this pin to ground with a 0.01uF capacitor.
14, 37, 46, 47, 49	I	Power	AVDD3	Analog Supply: Connect to a nominal 3.3V supply
15	I	Diff Input	REFB_IN	Frequency/Phase Reference B Input. This internally biased input is typically AC-coupled, and when configured as such, can accept any differential signal whose single-ended swing is between 0.4 and 3.3V. If DC-coupled, LVPECL or CMOS input is preferred.
16	I	Diff Input	REFB_INB	Complementary Frequency/Phase Reference B Input: Complementary signal to the input provided on pin 15. If using a single-ended, DC-coupled CMOS signal into REFA_IN, bypass this pin to ground with a 0.01uF capacitor.
17, 18			N/C	No Connects: These are excess, unused pins that may be left floating
20, 21	O		PFD_VRB, PFD_VRT	These pins must be capacitively decoupled. See the *Phase Detector Pin Connections* section for details.
22	O	I set Res	PFD_RSET	Connect a 5kΩ resistor from this pin to Ground (see the *Phase Detector Pin Connections* section).
27	I	Diff Input	SYSCLK	System Clock Input. Can be LVPECL or Crystal input, depending on CLKMODESEL pin. Single-ended 1.8V CMOS is also ok, but can introduce a spur caused by an input duty cycle that is not 50%.
28	I	Diff Input	SYSCLKB	Complementary System Clock: Complementary signal to the input provided on pin 27.
31	O		LOOP_FILTER	System Clock Multiplier Loop Filter: When using the frequency multiplier to drive the System Clock, an external loop filter must be constructed and attached to this pin. This pin is pulled high when the system clock PLL is bypassed, and can be left floating in this mode. Put a hyperlink here.
32	I	1.8V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pins 27 and 28). Pull up to 1.8V when using either an oscillator or external clock source. (See the *SysClk Inputs* section for details on the use of this pin).
33, 39, 43, 52	I	GND	AVSS	Analog Ground: Connect to Ground.
34	O	1.8V HSTL	OUTB	Complementary HSTL Output: See spec table and the OUTPUT DRIVERS AND MULTIPLIER section, under sub heading Primary (Differential) Driver, for details.
35	O	1.8V HSTL	OUT	HSTL Output: See spec table and the OUTPUT DRIVERS AND MULTIPLIER section, under sub heading Primary (Differential) Driver, for details.
38	O	3.3V CMOS	OUT_CMOS	CMOS Output: See specification table and the CLOCK DRIVERS section
40	I	Diff Input	FDBK_INB	Complementary Feedback input: In standard operating mode, this pin is connected to the filtered IOUTB output . This internally biased input is typically AC-coupled, and when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
41	I	Diff Input	FDBK_IN	Feedback Input: In standard operating mode, this pin is connected to the filtered IOUT output
48	O		DAC_RSET	DAC output current setting resistor. Connect a resistor from this pin to GND . See the "*DAC Output*" section.
50	O		IOUT	DAC output: This signal should be filtered and sent back on chip through FDBK_IN input
51	O		IOUTB	Complimentary DAC output: This signal should be filtered and sent back on chip through FDBK_INB input
56	I/O	3.3V CMOS	REFSELECT	Reference Select input: In manual mode, the REFSELECT pin operates as a high impedance input pin, while in automatic mode, it operates as a low impedance output pin. Logic 0 (low) indicates/selects RefA. Logic 1 (high) indicates/selects RefB. There is no internal pull-up/pull-down resistor on this pin.

57	I/O	3.3V CMOS	HOLDOVER	Holdover: (Active high) In manual holdover mode, this pin is used to force the AD9549 into holdover mode. In automatic holdover mode, it indicates holdover status. There is no internal pull-up/pull-down resistor on this pin.
58	I	3.3V CMOS	PWRDOWN	Power Down: When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50kohm pull-down resistor.
59	I	3.3V CMOS	RESET	Chip Reset: When this active high pin is asserted, the chip goes into reset. Note: upon power up, a 10 us reset pulse is internally generated when the power supplies reach a threshold and stabilize. This pin has an internal 50kohm pull-down resistor.
60	I	3.3V CMOS	IO_UPDATE	I/O Update: A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the *Write* subsection of the *General Operation of Serial Control Port* section). This pin has an internal 50kohm pull-down resistor.
61	I	3.3V CMOS	CSB	Chip Select: Active low. When programming a device, this pin must be held low. In systems where more than one AD9549 is present, this pin enables individual programming of each AD9549. This pin has an internal 100kohm pull-up resistor.
62	O	3.3V CMOS	SDO	Serial Data Output: When the device is in three wire mode, data is read on this pin. There is no internal pull-up/pull-down resistor on this pin.
63	I/O	3.3V CMOS	SDIO	Serial Data Input/Output: When the device is in three-wire mode, data is written via this pin. In 2 wire mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
64	O	3.3V CMOS	SCLK	Serial Programming Clock: data clock for serial programming. This pin has an internal 50kohm pull-down resistor.

INPUT / OUTPUT TERMINATION RECOMMENDATIONS

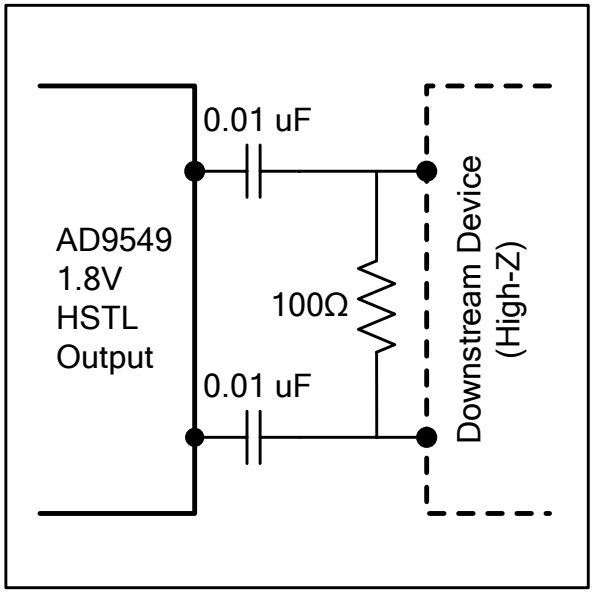


Figure 4: AC-Coupled HSTL Output Driver (Recommended)

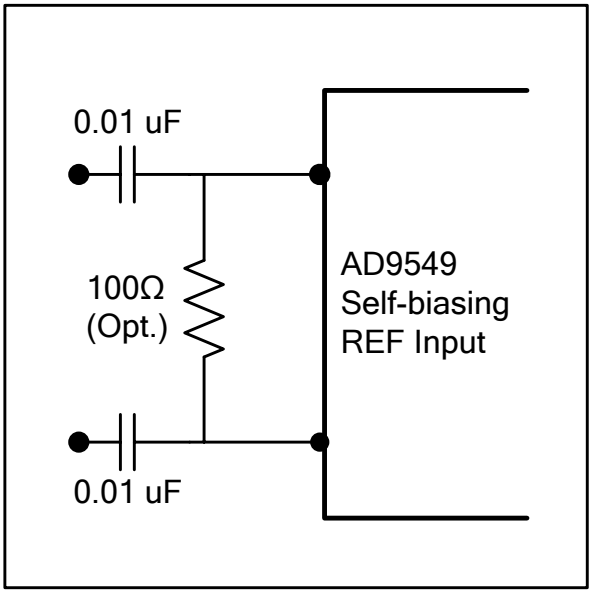


Figure 6: Reference Input.

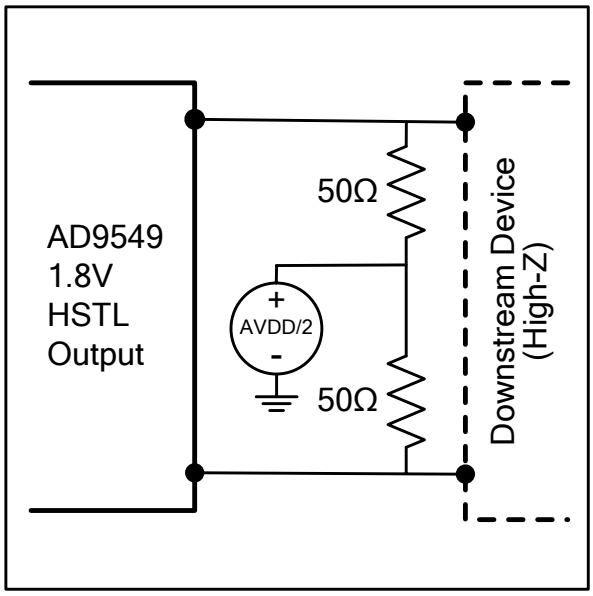


Figure 5: DC-Coupled HSTL Output Driver

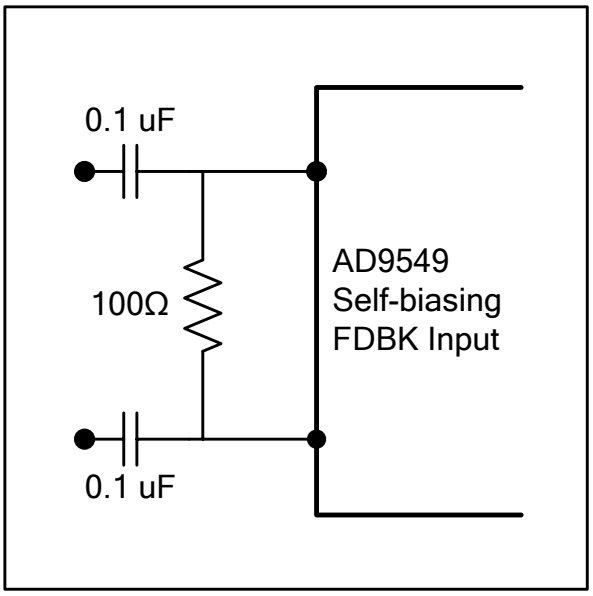


Figure 7: FDBK Input.

THEORY OF OPERATION

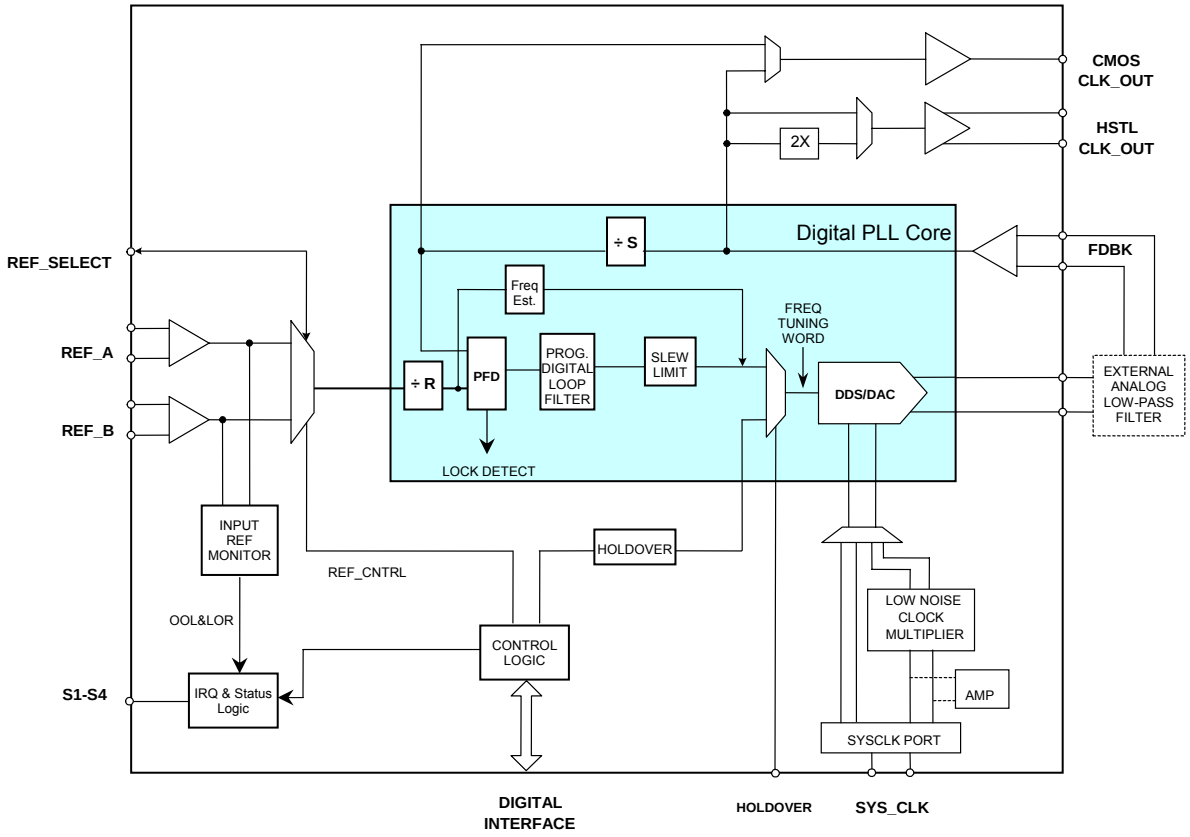


Figure 8: Detailed Block Diagram

OVERVIEW

The AD9549 provides a clocking output which is directly related in phase and frequency to the selected (active) reference (REF_A or REF_B), but having a phase noise spectrum primarily governed by the system clock. A wide band of reference frequencies is supported. Jitter existent on the active reference is greatly reduced by a programmable digital filter in the Digital Phase Locked Loop (PLL), which is the core of this product. The AD9549 supports both manual and automatic holdover. While in holdover, the AD9549 will continue to provide an output as long as the system clock is maintained. The frequency of the output during holdover is an average of the steady state output frequency prior to holdover. Also offered are manual and automatic switchover modes for changing between the two references should one become suspect or lost. A digitally controlled oscillator (DCO) is implemented using a Direct Digital Synthesizer (DDS) with an integrated output DAC, clocked by the system clock. A bypassable PLL based frequency multiplier is present enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed, and a low-noise high-frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter. The output signal from the reconstruction filter is fed back to the AD9549, both to complete the PLL, and to be processed through the output circuitry. The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler, for designs that need to provide frequencies above the Nyquist level of the DDS.

The individual functional blocks are described in the following sections.

PLL CORE (DPLLC)

The Digital Phase Locked Loop Core (DPLLC) includes the frequency estimation block and the digital phase lock control block driving the DDS.

The start of the DPLLC signal chain is the reference signal, f_R, which appears on REF A or REF B inputs. The frequency of this signal can be divided by an integer factor of R via the feedforward divider. The output of the feedforward divider is routed to the phase/frequency detector (PFD). Therefore, the frequency at the input to the PFD is given by $f_{PFD} = \frac{f_R}{R}$.

The PFD outputs a time series of digital words that are routed to the digital loop filter. The digital filter implementation offers many advantages: The filter response is determined by numeric coefficients rather than discrete component values. There is no aging of components and therefore, no drift of component value over time. There is no thermal noise in the loop filter, and there is no control node leakage current (which causes reference feed through in a traditional analog PLL).

The output of the loop filter is a time series of digital words. These words are applied to the frequency tuning input of a DDS to steer the DCO frequency. The DDS provides an analog output signal via an integrated DAC, effectively mimicking the operation of an analog VCO.

The DPLLC can be programmed to operate in conjunction with an internal frequency estimator to help decrease the time required to achieve lock. When the frequency estimator is employed, frequency acquisition is accomplished in a two-step process:

Step 1: An estimate is made of the frequency of f_{PFD}. The phase-lock control loop is essentially inoperative during the frequency estimation process. Once a frequency estimate is made, it is delivered to the DDS so that its output frequency is approximately equal to f_{PFD} multiplied by S (the modulus of the feedback divider).

Step 2: The phase-lock control loop becomes active and acts as a servo to acquire and hold phase lock with the reference signal.

As mentioned in step 1) above, the DPLLC includes a feedback divider that allows the DCO to operate at an integer multiple (S) of f_{PFD}. This establishes a nominal DCO frequency (f_{DDS}) given by: $f_{DDS} = \left(\frac{S}{R}\right) f_R$.

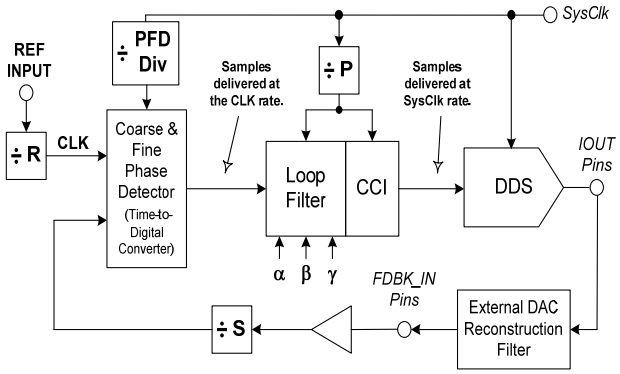


Figure 9: AD9549 Digital PLL Block Diagram

Feedforward Divider (Divide-by-R)

The feedforward divider is an integer divider allowing frequency prescaling of the REF Source input signal while maintaining the desired low jitter performance of the AD9549.

The feedforward divider is a programmable modulus divider with very low jitter injection. The divider is capable of handling input frequencies as high as 750 MHz. The divider depth is 16-bits cascaded with an additional divide-by-two. The divider therefore is capable of integer division from 1 to 65,535 (index of 1) or 2 to 131,070 (index of 2). The divider is programmed via the I/O Register Map to trigger on either the rising (default) or falling edge of the REF Source input signal.

There is a lower bound on the value of R imposed by the phase-frequency detector within the DPLLC which has a maximum operating frequency of $f_{PFD[max]}$ as explained in the *Fine Phase Detector* section. The "R Divider /2" bit must be set when REF_A or REF_B is greater than 400 MHz. The user must also ensure that R is chosen so that it satisfies the inequality:

$R \geq ceil(f_R / f_{PFD[max]})$

The upper bound is:

$R \leq floor(f_R / 8\ kHz)$

Where the *ceil*(x) function yields the nearest integer ≥ x. For example, if f_R=155 MHz and $f_{PFD[max]}$ =24.5 MHz, then *ceil* (155/24.5) = 7, so R must be ≥ 7.

Feedback Divider (Divide-by-S)

The feedback divider is an integer divider allowing frequency multiplication of the REF signal that appears at the input of the phase detector. It is capable of handling frequencies well above the Nyquist limit of the DDS. The divider depth is 16-bits cascaded with an additional divide-by-two. The divider is therefore capable of integer division from 1 to 65,535 (index of 1) or 2 to 131,070 (index of 2). The divider is programmed via

the I/O Register Map to trigger on either the rising (default) or falling edge of the feedback signal.

The feedback divider must be programmed within certain boundaries. The "S Divider /2" bit must be set when FDBK_IN is greater than 400 MHz. The upper boundary on the feedback divider is the lesser of the maximum programmable value of S and the maximum practical output frequency of the DDS (~ 40%f_S). Two formulae are given: S_{max1} for a feedback divider index of 1 and S_{max2} for an index of 2:

$$S_{\max 1} = \min\left(\frac{40\% f_S R}{f_R}, 65535\right) \quad \text{or}$$

$$S_{\max 2} = \min\left[\frac{40\% f_S R}{f_R}, 131070\right]$$

Where R is the modulus of the feedforward divider, f_S is the DAC sample rate, and f_R is the input reference frequency.

The DCO has a minimum frequency, f_{DCOmin} (see DAC output Characteristics section of AC specification table). This imposes a lower bound, S_{min}, on the feedback divider value, as well.

$$S_{\min} = \max\left(R\left(\frac{f_{DCO\min}}{f_R}\right), 1\right)$$

NOTE: Reduced DCO frequencies result in worse jitter performance (a consequence of the reduced slew rate of the sinusoid generated by the DDS).

Forward and Reverse FEC Clock Scaling

The Feedforward (Divide-by-R) and Feedback Divider (Divide-by-S) enable FEC clock scaling. For instance, to multiply the incoming signal by 255/237, set the S- divider to 255, and the R-divider to 237. One should be careful to abide by the limitations on the R- and S-Dividers, and make sure the Phase Detector input frequency is within specified limits.

Phase Detector

The phase detector is composed of two detectors: a coarse phase detector and a fine phase detector. The two detectors operate in parallel. Both detectors measure the duration (Δt) of the pulses generated by a conventional 3-state phase/frequency detector.

Together, the fine and coarse phase detectors produce a digital word that is a time-to-digital conversion of the separation between the edge transitions of the pre-scaled reference signal and the feedback signal.

If the fine phase detector is able to produce a valid result, then this result alone serves as the phase error measurement. If the fine phase detector is either in an overflow or underflow condition, the phase error measurement uses the coarse phase detector instead.

Digital Loop Filter

The digital loop filter integrates and low-pass filters the digital phase error values delivered by the phase detector. The loop filter response mimics that of a 2nd order, R-C network used to filter the output of a typical phase detector and charge pump combination as shown in the diagram below.

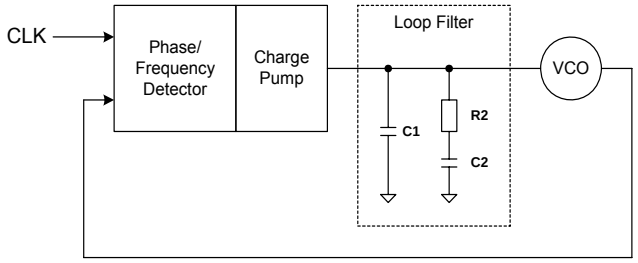


Figure 10: Typical Analog PLL Block Diagram

The building blocks implemented on the AD9549, however, are digital. A time-to-digital converter that produces digital values proportional to the edge timing error between the CLK and feedback signals replaces the phase-frequency detector and charge pump. A digital filter that processes the edge timing error samples from the time-to-digital converter replaces the loop filter. A DDS replaces the VCO, which produces a frequency that is linearly related to the digital value provided by the loop filter. This is shown in Figure 11 on Page 22 with some additional detail.

The samples provided by the time-to-digital converter are delivered to the loop filter at a sample rate equal to the CLK frequency (i.e., f_R/R). The loop filter is intended to oversample the time-to-digital converter output at a rate determined by the "P"-divider. The value of P is programmable via the I/O Register Map. It is stored as a 5-bit number, P_{IO}. The value of P_{IO} is related to P by the equation:

$P = 2^{P_{IO}}$ (where $5 \le P_{IO} \le 16$)

Hence, the "P"-divider can provide divide ratios between 32 and 65536 in power-of-2 steps. With a DAC sample rate of 1GHz the loop filter sample rate can range from as low as 15.26kHz to a maximum of 31.25MHz. Coupled to the loop filter is a cascaded comb-integrator (CCI) filter that provides a sample rate translation between the loop filter sample rate (f_S/P) and the DDS sample rate, f_S.

The choice of P is important because it controls both the response of the CCI filter and the sample rate of the loop filter. In order to understand the method for determining a useful

value for P, it is first necessary to examine the transfer function of the CCI filter:

$$H(\omega)_{CCI} = \left[\frac{1-e^{-j\omega P}}{P(1-e^{-j\omega})}\right]^2$$

or

$$\left|H_{CCI}(\omega)\right| = \begin{cases} 1, & \omega = 0 \\ \frac{1}{P^2}\left(\frac{1-\cos(\omega P)}{1-\cos(\omega)}\right), & \omega > 0 \end{cases}$$

To evaluate the response in terms of absolute frequency, make the substitution:

$$\omega = \frac{2\pi f}{f_S}$$

(where f_S is the DAC sample rate and *f* is the frequency at which H_{CCI} is to be evaluated)

Analysis of this function reveals that the CCI magnitude response follows a low pass characteristic that consists of a series of P lobes. The lobes are bounded by null points occurring at frequency multiples of f_S/P. The peak of each successive lobe is lower that its predecessor over the frequency range between DC and $\frac{1}{2}f_S$. For frequencies greater than $\frac{1}{2}f_S$, the response is a reflection about the vertical at $\frac{1}{2}f_S$. Furthermore, the first lobe (which appears between DC and f_S/P) exhibits a monotonically decreasing response. That is, the magnitude is unity at DC and it steadily decreases with frequency until it vanishes at the first null point (f_S/P).

The null points imply the existence of transmission zeros placed at finite frequencies. While transmission zeros placed at infinity yield minimal phase delay, zeros placed closer to DC result in increased phase delay. Hence, the position of the first null point has a significant impact on the phase delay introduced by the CCI filter. This is an important consideration, because excessive phase delay negatively impacts the overall closed loop response. As a rule of thumb, choose a value for P so that the frequency of the first null point (f_S/P) is the greater of:

80 times the desired loop bandwidth, or

1.5 times the frequency of CLK (f_R/R)

The value of P thus calculated (P_{MAX}) is the largest usable value in practice. Since P is programmed as P_{IO}, it is necessary to define P_{MAX} in terms of P_{IO}, so that P_{IOMAX} may be determined. The condition, $P_{IO} \le P_{IOMAX}$, ensures that the impact of the phase delay of the CCI filter on the phase margin of the loop will not exceed 5°. P_{IOMAX} may be expressed as:

$$P_{IOMAX} = \max\left\langle 5, \quad \min\left\{16, \ floor\left[\log_2\left(\frac{f_S}{80 f_{LOOP}}\right)\right], floor\left[\log_2\left(\frac{2 f_S}{3 f_{REF}}\right)\right]\right\}\right\rangle$$

With a properly chosen value for P, the closed-loop response of the digital PLL is primarily determined by the response of the digital loop filter. Flexibility in controlling the loop filter response translates directly into flexibility in the range of applications satisfied by the architecture of the AD9549.

The AD9549 Evaluation Software automatically sets the value of the P divider based on the user's input criteria. Therefore, the formulas are provided here mainly to assist in understanding how the part works.

Direct Digital Synthesizer

One of the primary building blocks of the digital PLL is a direct digital synthesizer (DDS). The DDS behaves like a sinusoidal signal generator. The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (i.e., numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the DDS's fundamental timing source. The accumulator behaves as a modulo-2^{48} counter with a programmable step size (FTW). A block diagram of the DDS is shown below.

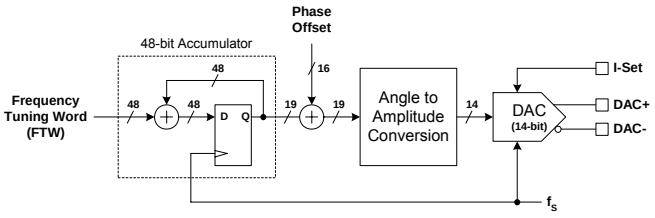


Figure 11: DDS Block Diagram

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output. For example, given an FTW=5, the accumulator would count by 5's, incrementing on each f_S cycle. Over time, the accumulator will reach the upper end of its capacity (2^{48} in this case). At which point it rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The average rollover rate of the accumulator is given by the formula below, and establishes the output frequency (f_{DDS}) of the DDS.

$$f_{DDS} = \left(\frac{FTW}{2^{48}}\right) f_S$$

Solving this equation for FTW yields:

$$FTW = round\left[2^{48}\left(\frac{f_{DDS}}{f_S}\right)\right]$$

For example, given that f_S=1GHz and f_{DDS}=19.44MHz, then FTW=5,471,873,547,255 (04FA05143BF7h).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the *phase offset* input to the DDS (a programmable 16-bit value (Δ*phase*); see the I/O Register Map). The resulting phase offset, Δϕ (radians), is given by:

$$\Delta\phi = 2\pi\left(\frac{\Delta phase}{2^{16}}\right)$$

The DDS can be operated in either *open loop* or *closed loop* mode, via the Close Loop bit in the DPLL Register.

There are two open loop modes: Single Tone and Holdover. In Single Tone Mode, the DDS behaves like a frequency synthesizer, and uses the value stored in the FTW0 register to determine its output frequency. Alternatively, the FTW and Δ*phase* values can be determined by the device itself using the frequency estimator. Because Single Tone mode ignores the reference inputs, it is very useful for generating test signals to aid in debugging. Single Tone mode must be activated manually via register programming.

In Holdover mode, the AD9549 uses past tuning words when the loop was closed to determine its output frequency. Therefore, the loop must have been successfully closed in order for Holdover Mode to work. Switching in and out of Holdover Mode can be either automatic or manual, depending on register settings.

Typically, the AD9549 operates in *closed loop* mode. In closed loop mode, the FTW values come from the output of the digital loop filter and vary with time. The DDS frequency is steered in a manner similar to a conventional VCO-based PLL.

NOTE: In "closed loop" mode, the DDS phase offset capability is inoperative.

DAC Output

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see DAC output diagram below). The peak output current derives from the combination of two factors. The first is a reference current (I_{DAC_REF}) established at the DAC_RSET pin and the second is a scale factor programmed into the I/O Register map.

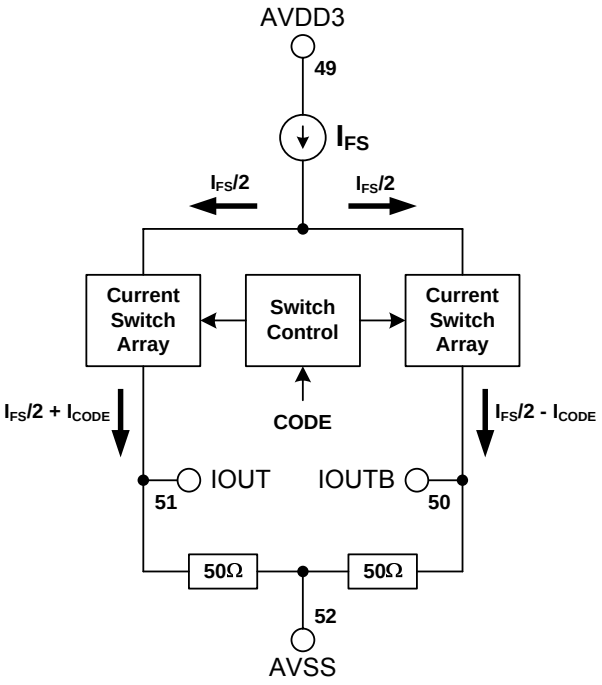


Figure 12: DAC Output Pins

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2v nominal, so the reference current can be calculated by:

$$I_{DAC\_REF} = \frac{1.2}{R_{DAC\_REF}}$$

NOTE: The recommended value of I_{DAC_REF} is 120µA, which leads to a recommended value of R_{DAC_REF} of 10kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the *DAC FS Current* register in the I/O Register Map. The full-scale DAC output current (I_{DAC_FS}) is then given by:

$$I_{DAC\_FS} = I_{DAC\_REF}\left(72 + \frac{192 \cdot FSC}{1024}\right)$$

Using the recommended value of R_{DAC_REF} the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6mA to 31.7mA. 20 mA is the default value.

PHASE DETECTOR

Coarse Phase Detector

The coarse phase detector uses the DAC sample rate (f_S) to determine the edge timing deviation between the REF signal and the feedback signal generated by the DDS. Hence, f_S sets the timing resolution of the coarse phase detector. At the recommended rate of f_S=1GHz, the coarse phase detector spans a range of over 131µs (sufficient to accommodate REF signal frequencies as low as 8 kHz).

The phase gain of the coarse phase detector is controlled via the I/O Registers by means of two numeric entries. The first is a 3-bit power-of-2 scale factor, PDS. The second is a 6-bit linear scale factor, PDG.

$$Phase\,Gain_{CPD} = R\left(\frac{f_S}{f_R}\right)\left(2^{PDS+6}\,PDG\right)$$

Fine Phase Detector

The fine phase detector operates on a divided down version of f_S as its sampling time base. The sample rate of the fine phase detector is set using a 4-bit word (PFD_Div) in the I/O Register Map and is given by:

$$Fine\ Phase\ Detector\ Sample\ Rate = \frac{f_S}{4(PFD\_Div)}$$

The default value of PFD_Div is 5, so for f_S=1GHz, the default sample rate of the fine phase detector is 50MHz. The upper bound on the maximum allowable input frequency to the phase detector ($f_{PFD[max]}$) is 49% of the sample rate, or:

$$f_{PFD[\max]} = \frac{f_S}{8(PFD\_Div)}$$

Therefore, $f_{PFD[max]}$ is 25MHz in the example above.

The fine phase detector uses a proprietary technique to determine the phase deviation between the REF signal and feedback signal.

The phase gain of the fine phase detector is controlled by an 8-bit scale factor (FPFD_Gain) in the I/O Register Map. The nominal (default) value of FPFD_Gain is 200, and establishes the phase gain as: $PhaseGain_{FPD} = \frac{R\left(2^{10}10^7\right)(FPFD\_Gain)}{f_R}$

Phase Detector Gain Matching

Although the fine and coarse phase detectors use different means to make a timing measurement, it is essential that both have equivalent phase gain. Without proper gain matching the closed-loop dynamics of the system cannot be properly controlled. Hence, the goal is to make $PhaseGain_{CPD}$= $PhaseGain_{FPD}$. This leads to:

$$\left(f_S\,2^{PDS+6}\right)PDG = \left(2^{10}10^7\right)FPFD\_Gain$$

Which simplifies to:

$$2^{PDS}\,PDG = \frac{\left(16 \cdot 10^7\right)FPFD\_Gain}{f_S}$$

Typically, FPFD_Gain is established first and then PDG and PDS are calculated. The proper choice for PDS is given by:

$$PDS = round\left\lfloor \log_2\left(\frac{10^7\,FPFD\_Gain}{2\,f_S}\right)\right\rfloor$$

The final value of PDS must satisfy 0 ≤ PDS ≤ 7. The proper choice for PDG is calculated using this equation:

$$PDG = round\left(\frac{10^7\,FPFD\_Gain}{2^{PDS-4}\,f_S}\right)$$

The final value of PDG must satisfy 0 ≤ PDG ≤ 63. For example, let f_S=700MHz and FPFD_Gain=200, then PDS=1 and PDG=23.

Note that the AD9549 Evaluation Software will calculate register values that have the phase detector gains already matched.

Phase Detector Pin Connections

There are three pins associated with the phase detector that must be connected to external components. The diagram below shows the recommended component values and their connections.

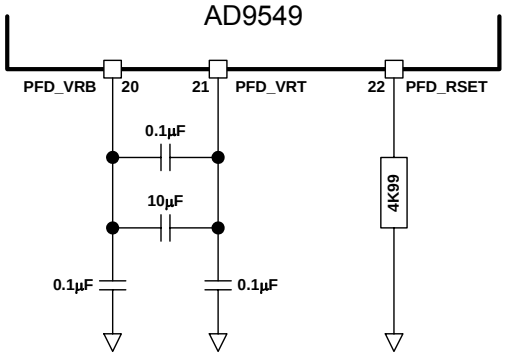


Figure 13: Phase Detector Pin Connections

DIGITAL LOOP FILTER COEFFICIENTS

In order to provide the desired flexibility, the loop filter has been designed with three programmable coefficients (α, β and γ). The coefficients along with P (where $P=2^{Pio}$) completely defines the response of the filter, which is given by:

$$H(\omega)_{LoopFilter} = \alpha\left(\frac{e^{j\omega}+(\beta-\gamma-1)}{e^{j2\omega}+(-\gamma-2)e^{j\omega}+(\gamma+1)}\right)$$

To evaluate the response in terms of absolute frequency substitute:

$$\omega = \frac{2\pi Pf}{f_S}$$

Where P is the divide ratio of the "P"-divider, f_S is the DAC sample rate, and *f* is the frequency at which the function is to be evaluated.

The loop filter coefficients are determined by the AD9549 evaluation software according to three parameters:

ϕ: desired closed-loop phase margin ($0 < \phi < \pi/2$ rad)

f_{LOOP}: desired open-loop bandwidth (Hz)

f_{DDS}: desired output frequency of the DDS (Hz)

Note that f_{DDS} can also be expressed as $f_{DDS} = f_R(S/R)$.

The three coefficients are calculated according to parameters via the equations below:

$$\beta = -4\pi P f_C \tan(\phi)$$

$$\gamma = \tfrac{1}{2} F(\phi)\beta$$

$$\alpha = -\left(\frac{2^{38}\pi}{10^7\, FPFD\_Gain}\right) f_{DDS}\, f_C F(\phi)\beta$$

Where $F(\phi) = 1 + \frac{1}{\sin(\phi)}$, $f_C = \frac{f_{LOOP}}{f_S}$, and FPFD_Gain is the value of the gain scale factor for the Fine Phase Detector as programmed into the I/O Register Map.

NOTE: The range of loop filter coefficients is limited as follows:

$0 < \alpha < 2^{23}$ (~$8.39 \cdot 10^6$)

$-0.125 < \beta < 0$

$-0.125 < \gamma < 0$

The above constraints on β and γ constrain the closed-loop phase margin such that both β and γ will assume negative values. Even though β and γ are limited to negative quantities, the values as programmed are positive. The negative sign is assumed internally.

NOTE: The closed-loop phase margin is limited to the range of $0° < \phi < 90°$ because β and γ are negative.

The three coefficients are implemented as digital elements, necessitating quantized values. Determination of the programmed coefficient values in this context follows.

The quantized α coefficient is composed of three factors, where α_0, α_1 and α_2 are the programmed values for the α coefficient:

$$\alpha_{quantized} = \left(\frac{\alpha_0}{2048}\right)\left(2^{\alpha_1}\right)\left(2^{-\alpha_2}\right)$$

The boundary values for each are $0 \le \alpha_0 \le 4095$, $0 \le \alpha_1 \le 22$, and $0 \le \alpha_2 \le 7$. The optimal values of α_0, α_1 and α_2 are:

$$\alpha_1 = \max\left[0,\ \min\left\{22,\ ceil\left(\log_2 \tfrac{2048\alpha}{4095}\right)\right\}\right]$$

$$\alpha_2 = \max\left[0,\ \min\left\{7,\ floor\left(\log_2\left(\tfrac{4095}{\alpha}\right) + \alpha_1 - 11\right)\right\}\right]$$

$$\alpha_0 = \max\left[0,\ \min\left\{4095,\ round\left(\alpha \cdot 2^{\alpha_2 - \alpha_1 + 11}\right)\right\}\right]$$

The magnitude of the quantized β coefficient is composed of two factors, where β_0 and β_1 are the programmed values for the β coefficient:

$$\beta_{quantized} = (\beta_0)\left(2^{-(\beta_1+15)}\right)$$

The boundary values for each are $0 \le \beta_0 \le 4095$ and $0 \le \beta_1 \le 7$. The optimal values of β_0 and β_1 are:

$$\beta_1 = \max\left[0, \min\left\{7, \ floor\left(\log_2\left(\frac{4095}{|\beta|}\right)-15\right)\right\}\right]$$

$$\beta_0 = \max\left[0, \min\left\{4095, round\left(|\beta| \cdot 2^{\beta_1+15}\right)\right\}\right]$$

The magnitude of the quantized γ coefficient is composed of two factors: $\gamma_{quantized} = (\gamma_0)\left(2^{-(\gamma_1+15)}\right)$

Where γ_0 and γ_1 are the programmed values for the γ coefficient, the boundary values for each are $0 \le \gamma_0 \le 4095$ and $0 \le \gamma_1 \le 7$. The optimal values of γ_0 and γ_1 are:

$$\gamma_1 = \max\left[0, \min\left\{7, \ floor\left(\log_2\left(\frac{4095}{|\gamma|}\right)-15\right)\right\}\right]$$

$$\gamma_0 = \max\left[0, \min\left\{4095, round\left(|\gamma| \cdot 2^{\gamma_1+15}\right)\right\}\right]$$

The *min*(), *max*(), *floor*(), *ceil*() and *round*() functions are defined as follows. The function, *min*(x_1, x_2, … x_n), chooses the smallest value in the list of arguments. The function, *max*(x_1, x_2, … x_n), chooses the largest value in the list of arguments. The function, *ceil*(x), increases x to the next higher integer if x is NOT an integer, otherwise x is unchanged. The function, floor(x), reduces x to the next lower integer if x is NOT an integer, otherwise x is unchanged. The function, *round*(x), rounds x to the nearest integer.

To demonstrate the wide programmable range of the loop filter bandwidth, consider the following design example. The system clock frequency (f_S) is 1GHz, the input reference frequency (f_R) is 19.44MHz, the DDS output frequency (f_{DDS}) is 155.52MHz, and the required phase margin (ϕ) is 45°. f_R is within the nominal bandwidth of the phase detector (25MHz), and f_{DDS}/f_R, is an integer (8), so the prescalar is not required. We can therefore use R=1 and S=8 for the feedforward and feedback dividers, respectively.

NOTE: If f_{DDS}/f_R is a non- integer, then R and S must be chosen such that $S/R = f_{DDS}/f_R$ with S and R both constrained to integer values. For example, if f_R=10MHz and f_{DDS}=155.52MHz, then the optimal choice for S and R is 1944 and 125, respectively.

The open loop bandwidth range under the defined conditions spans **9.5Hz** to **257.5kHz**. The wide dynamic range of the loop filter coefficients allows for programming of any open loop bandwidth within this range under these conditions. The resulting closed loop bandwidth range under the same conditions is approximately **12Hz** to **359kHz**.

The resulting loop filter coefficients for the upper loop bandwidth along with the necessary programming values are shown below.

α = 4322509.4784981	β_0 = 3393 (D41h)
α_0 = 2111 (83Fh)	β_1 = 0 (0h)
α_1 = 22 (16h)	γ = -0.12499215775201
α_2 = 0 (0h)	γ_0 = 4095 (FFFh)
β = -0.10354689386232	γ_1 = 0 (0h)

The resulting loop filter coefficients for the lower loop bandwidth along with the necessary programming values are shown below.

α = 0.005883404361345	β_0 = 16 (10h)
α_0 = 1542 (606h)	β_1 = 7 (7h)
α_1 = 0 (00h)	γ = -0.00000461136116
α_2 = 7 (7h)	γ_0 = 19 (13h)
β = -0.000003820176667	γ_1 = 7 (7h)

The AD9549 Evaluation Software generates these coefficients automatically based on the user's desired loop characteristics.

CLOSED LOOP PHASE OFFSET

The AD9549 provides for limited control over the phase offset between the reference input signal and the output signal by adding a constant phase offset value to the output of the phase detector. An adder is included at the output of the phase detector as shown in the figure below to support this. The value of the constant (PLL_{OFFSET}) is set via the *PLL Offset* register.

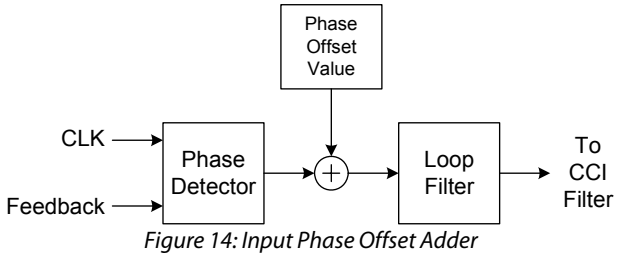


Figure 14: Input Phase Offset Adder

PLL$_{OFFSET}$ is a function of the phase detector gain and the desired amount of timing offset (Δt_{OFFSET}). It is given by:

$$PLL_{OFFSET} = \Delta t_{OFFSET}\left(2^{10}10^{7}\, FPFD\_Gain\right)$$

NOTE: FPFD_Gain is described in the Fine Phase Detector section.

For example, suppose that FPFD_Gain=200, f_{CLK}=3MHz, and 1° of phase offset is desired. First, we must find the value of Δt_{OFFSET}, which is:

$$\Delta t_{OFFSET} = \frac{\deg}{360} T_{CLK} = \frac{1}{360}\left(\frac{1}{3MHz}\right) = 925.9\, ps$$

Having determined Δt_{OFFSET}, we have:

$$PLL_{OFFSET} = 925.9\, ps\left(2^{10}\cdot 10^{7}\cdot 200\right) = 1896$$

The result has been rounded because PLL$_{OFFSET}$ is restricted to integer values.

NOTE: The PLL$_{OFFSET}$ value is programmed as a 14-bit, twos-complement number. However, the user must ensure that the magnitude is constrained to 12 bits, such that:

$-2^{11} \le PLL_{OFFSET} < +2^{11}$

The above constraint yields a timing adjustment range of ±1ns. This ensures that the phase offset remains within the bounds of the fine phase detector.

LOCK DETECTION

Phase Lock Detection

During the phase locking process, the output of the phase detector tends toward a value of zero, which indicates perfect alignment of the phase detector input signals. As the control loop works to maintain the alignment of the phase detector input signals, the output of the phase detector wanders around zero.

The phase lock detector tracks the *absolute value* of the digital samples generated by the phase detector. These samples are compared to the *Phase Lock Detect Threshold* value programmed in the I/O Register Map. A *false* state at the output of the comparator indicates the absolute value of a sample exceeds the value in the threshold register. A *true* state at the output of the comparator indicates alignment of the phase detector input signals to the degree specified by the lock detection threshold.

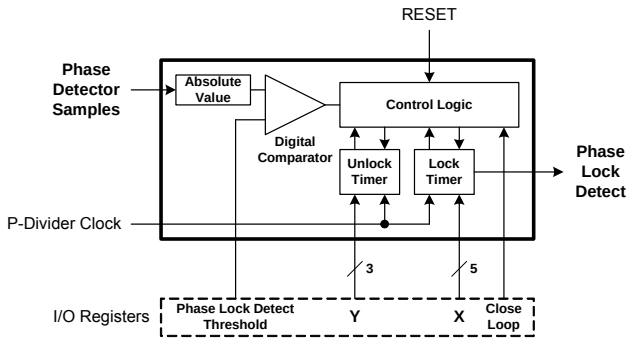


Figure 15: Phase Lock Detector Block Diagram

The Phase Lock Detect Threshold value (PLDT) is a 32-bit number stored in the I/O Register Map:

$$PLDT = round\left(\Delta t\cdot 2^{10}\cdot 10^{7}\cdot FPFD\_Gain\right)$$

Where Δt is the maximum allowable timing error between the signals at the input to the phase detector and the value of FPFD_Gain is as described in the *Fine Phase Detector* section. For example, suppose that f_R/R=3MHz, FPFD_Gain=200, and the maximum timing deviation is given as 1°. This yields a Δt value of:

$$\Delta t = \frac{1^{\circ}}{360^{\circ}}\left(R\cdot T_R\right) = \frac{R}{360\, f_R} = \frac{1}{360\cdot\left(3\cdot 10^{6}\right)}$$

The resulting phase lock detect threshold is:

$$PLDT = round\left(\frac{2^{10}\cdot 10^{7}\cdot 200}{360\left(3\cdot 10^{6}\right)}\right) = 1896$$

Hence, 1896 (00000768h) is the value that must be stored in the Phase Lock Detect Threshold register.

The "phase lock detect" signal is generated once the control logic observes that the output of the comparator has been in the *true* state for 2^X periods of the P-Divider clock (see the *Digital Loop Filter* section for a description of the P-Divider). Once the phase lock detect signal is asserted, it remains asserted until cleared by an "unlock" event or by a device RESET.

The duration of the lock detection process is programmable via the *Phase Lock Watchdog Timer* register. The interval is controlled by a 5-bit number, X ($0 \le X \le 20$). The absolute duration of the phase lock detect interval is:

$$T_{LOCK} = \frac{2^{X} P}{f_S}$$

Hysteresis in the phase lock detection process is controlled by specifying the minimum duration that qualifies as an unlock event. An unlock event is declared when the control logic observes that the output of the comparator has been in the *false* state for 2^{Y+1} periods of the P-Divider clock (provided that the phase lock detect signal has been asserted). Detection of an unlock event clears the phase lock detect signal, and the phase lock *detection* process is automatically restarted.

The time required to declare an unlock event is programmable via the *Phase Unlock Watchdog Timer* register. The interval is controlled by a 3-bit number, Y ($0 \le Y \le 7$). The absolute duration of the unlock detection interval is:

$$T_{UNLOCK} = \frac{2^{Y+1} P}{f_S}$$

Figure 16 below shows the basic timing relationship between the reference signal at the input to the phase detector, the phase error magnitude, the output of the comparator, and the output of the phase lock detector. The example shown here assumes that X=3 and Y=1.

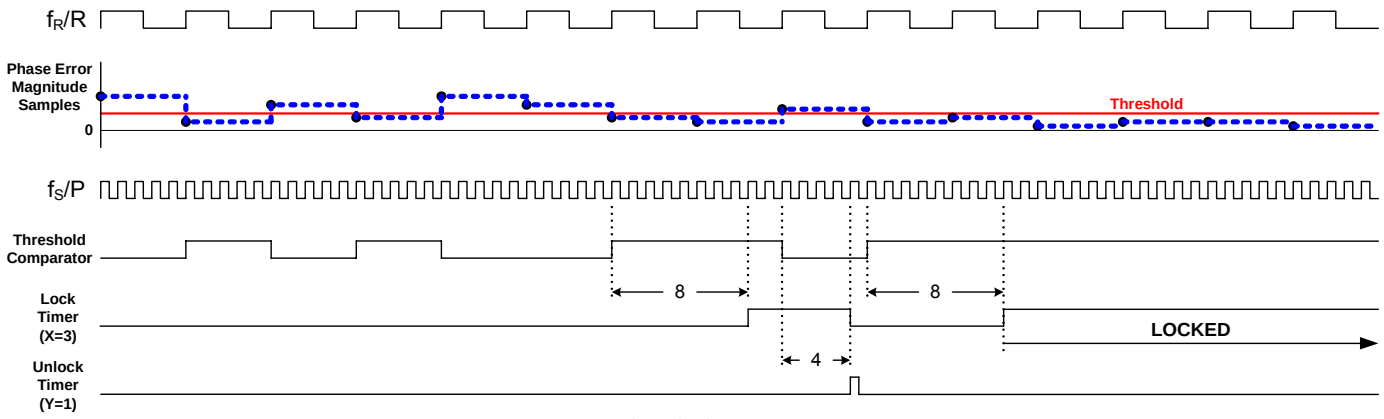


Figure 16: Lock/Unlock Detection Timing

Frequency Lock Detection

Frequency lock detection is similar to phase lock detection, with the exception that the *difference* between successive phase samples is the source of information. A running difference of the phase samples serves as a digital approximation to the time-derivative of the phase samples, which is analogous to frequency.

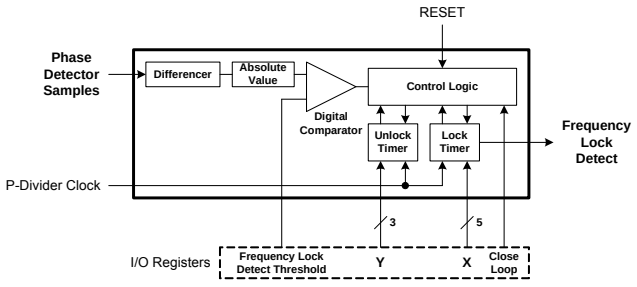


Figure 17: Frequency Lock Detection

The formula for the Frequency Lock Detect Threshold value (FLDT) is:

$$FLDT = round\left[\Delta f \cdot 2^{10}10^{7} FPFD\_Gain \cdot \left(\frac{R}{f_R}\right)^2\right]$$

Where f_R is the frequency of the active reference, R is the value of the reference prescaler, and Δf is the maximum frequency deviation of f_R that is considered to indicate a frequency locked condition ($\Delta f \ge 0$). For example, suppose that f_R=3MHz, R=5, FPFD_Gain=200, and a frequency lock threshold of 1% is specified. Then the frequency lock detect threshold value is:

$$FLDT = round\left[\left(1\% \cdot 3 \cdot 10^{6}\right) \cdot 2^{10}10^{7} \cdot 200 \cdot \left(\frac{5}{3 \cdot 10^{6}}\right)^2\right] = 170{,}667$$

Hence, 170667 (00029AABh) is the value that should be stored in the *Frequency Lock Detect Threshold* register.

The duration of the frequency lock/unlock detection process is controlled in exactly the same way as the phase lock/unlock

detection process in the previous section. However, different control registers are used: the *Frequency Lock/ Unlock Watchdog Timer* registers.

REFERENCE MONITORS

Loss of Reference

The AD9549 can set an alert when one or both of the reference signals are not present. Each of the two reference inputs (REFA, REFB) has a dedicated LOR (Loss of Reference) circuit enabled via the I/O Register Map. Detection of an LOR condition sets the appropriate LOR bit in both a status register and an IRQ register in the I/O Register Map. The LOR state is also internally available to the multi-purpose "status" pins (S1:4) of the AD9549. By setting the appropriate bit in the I/O Register Map, the user can assign a status pin to each of the LOR flags. This provides a means to control external hardware based on the state of the LOR flags directly.

The LOR circuits are internal 'watchdog' timers with a programmable period. The period of the timer is set via the I/O register Map so that its period is longer than that of the monitored reference signal. The rising edge of the reference signal continuously resets the watchdog timer. If the timer reaches a full count, this indicates that the reference was either lost or its period was longer than the timer period. LOR does not differentiate between these.

The period for each of the LOR timers is controlled by a 16-bit word in the I/O Register Map. The period of the timer clock (T_{CLK}) is $2/f_S$. Therefore, the period of the watchdog timer (T_{WD}) is:

$T_{WD} = (2/f_S)N$

Where N is the value of the 16-bit word stored in the I/O Register Map for the appropriate LOR circuit. Choose the value of N so that the watchdog period is greater than the input reference period, expressed mathematically as:

$$N > floor\left(\frac{f_S}{2 f_R}\right)$$

where f_R is the frequency of the input reference. The value of N results in establishing two frequencies. One for which the LOR signal will never be triggered ($f_{PRESENT}$), and one for which the LOR signal will always be active (f_{LOST}). Between these frequencies the LOR signal will intermittently toggle between states.

The values of the two frequency bounds are:

$$f_{PRESENT} = \frac{f_S}{2N} \qquad f_{LOST} = \frac{f_S}{2(N+1)}$$

Note that when N is chosen to be $floor\left(\frac{f_S}{2 f_R}\right)+1$, the LOR circuit is capable of indicating an LOR condition in little more than a single input reference period. For example, if f_S=1GHz and f_R=2.048MHz, then the smallest useable N value is:

$$N_{MIN} = floor\left(\frac{10^9}{2\left(2.048\times10^6\right)}\right)+1 = 245$$

Which yields values for $f_{PRESENT}$ and f_{LOST} as:

$$f_{PRESENT} = 2{,}048{,}816 \; and \; f_{LOST} = 2{,}032{,}520$$

NOTE: N should be chosen sufficiently large to account for any acceptable deviation in the period of the input reference signal.

Notice that the value of N is inversely proportional to the reference frequency, meaning that as the reference frequency goes up, the precision for adjusting the threshold goes down. Proper operation of the LOR circuit requires that N be no less than 3. Therefore, the highest reference frequency for which the LOR circuit will function properly is given by: $f_{LOR\_MAX} = f_S/6$.

Reference Frequency Monitor

The AD9549 can set an alert whenever one or both of the reference inputs drift in frequency beyond user-specified limits. Each of the two references has a dedicated Out of Limits (OOL) circuit enabled/disabled via the I/O Register Map. Detection of an OOL condition sets the appropriate OOL bit in both a status register and an IRQ register in the I/O Register Map. The user can also assign a status pin (S1-S4) to each of the OOL flags by setting the appropriate bit in the I/O Register Map. This provides a means to control external hardware based on the state of the OOL flags directly.

Each reference monitor contains three main building blocks: a programmable reference divider, a 32-bit counter, and a 32-bit digital comparator.

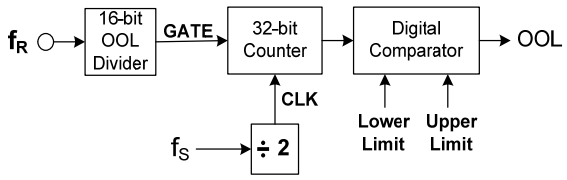


Figure 18: Reference Monitor

Four values are needed to calculate the correct values of the reference monitor: The system clock frequency, f_S (usually 1 GHz), the reference input frequency, f_R (in Hz), the error bound, E (1%=0.01), and the monitor window size (W). The monitor window size is the difference between the maximum and minimum number of counts accumulated between adjacent edges of the reference input. If this window is too small, random variations will cause the OOL detector to indicate incorrectly that a reference is out of limits. However, the time required to determine if the reference frequency is valid increases with window size. A window size of at least 20 is a good starting point.

The four input values mentioned above are used to calculate the OOL Divider (D) and OOL nominal value (N), which in turn are used to calculate the OOL Upper Limit (U), and OOL Lower Limit (L) according to the following formulas:

$$D = \max(1, \min(65535, ceil\left(4 * \frac{f_R}{f_S} * \frac{W}{E}\right)))$$

$$N = \frac{f_R}{f_S} * \frac{D}{4}$$

$$L = floor(N) - floor(W)$$

$$U = ceil(N) + floor(W)$$

The timing accuracy is dependent on two factors. The first is the inherent accuracy of f_S, since it serves as the time base for the Reference Monitor. As such, the accuracy of the Reference Monitor can be no better than the accuracy of f_S. Second, the value of W, which must be sufficiently large so that the timer resolves the deviation between a nominal value of f_R and a value that is out of limits.

As an example, let f_R=10MHz, E=1.0%, f_S=1GHz, and W=20. The limits are then:

Lower Limit = 1980 Upper Limit = 2020

Now let E=0.01%, Then the limits are:

Lower Limit = 199980 Upper Limit = 200020

Notice that the number of counts (and time) required to make this measurement has increased 100x.

REFERENCE SWITCHOVER

The AD9549 supports dual input reference clocks. Reference switchover may be accomplished either automatically or manually by appropriately programming the "AutoRefSel" bit in the I/O Register Map. Transition to a newly selected reference depends on a number of factors:

State of the REFSELECT pin

State of the "Ref_AB" control register bit

State of the "Enable Ref Input Override" register bit

Holdover status

A functional diagram of the reference switchover and holdover logic is shown in Figure 19.

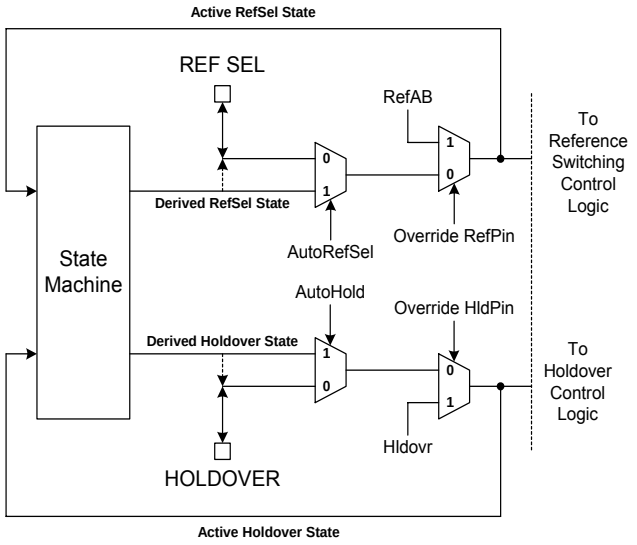


Figure 19: Reference Switchover and Holdover Logic

In manual mode, the active reference is determined by an externally applied logic level to the REFSELECT pin. In automatic mode, an internal state machine determines which reference is active, and the REFSELECT pin becomes an output indicating which reference the state machine is using.

The user may override the active reference chosen by the internal state machine via the "Enable Ref Input Override " bit in the I/O Register Map. The "Ref_AB" bit in the I/O Register Map is then used to select the desired reference. When in override, it is important to note that the REFSELECT pin does not indicate the physical reference selected by the "Ref_AB" bit. Instead, it indicates the reference that the internal state machine would select if the device were not in the override mode. This

allows the user to force a reference switchover by means of the programming registers while monitoring the response of the state machine via the REFSELECT pin.

The same type of operation (manual/automatic and override) also applies to the holdover function, as shown in the Reference Switchover Logic diagram. The dashed arrows in the diagram indicate that the state machine output is available to the REFSELECT and HOLDOVER pins when in override mode.

Use of Line Card Mode to Eliminate Runt Pulses

When two references are not in exact phase alignment and a transition is made from one to the other, it is possible that an extra pulse can be generated. This depends on the relative edge placement of the two references and the point in time that a switch over is initiated. To eliminate the "extra pulse" problem, an "Enable Line Card Mode" bit is provided in the I/O Register map. The Line Card Mode logic is shown in Figure 20 below. When Enable Line Card bit is 0, reference switch over occurs on command without consideration to the relative edge placement of the references. This means that there is the possibility of an extra pulse. However, when this bit is set to 1, the timing of the reference switch over is executed conditionally as shown in Figure 21 on Page 31.

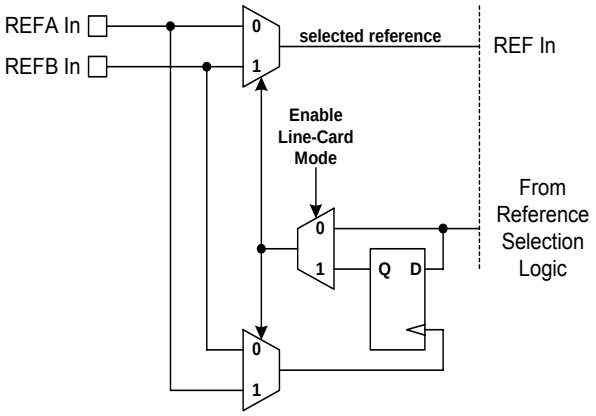


Figure 20: Reference Switchover Control Logic

Note that when the line card mode is enabled, the rising edges of the alternate reference are used to clock a latch. The latch holds off the actual transition until the next rising edge of the alternate reference.

Shown in Figure 21 is a timing diagram that demonstrates the difference between reference switchover with the line card mode enabled and disabled. If enabled, when the reference switchover logic is given the command to switch to the alternate reference, an actual transition does not occur until the next rising edge of the alternate reference. This action eliminates the spurious pulse that can occur when the line card mode is disabled.

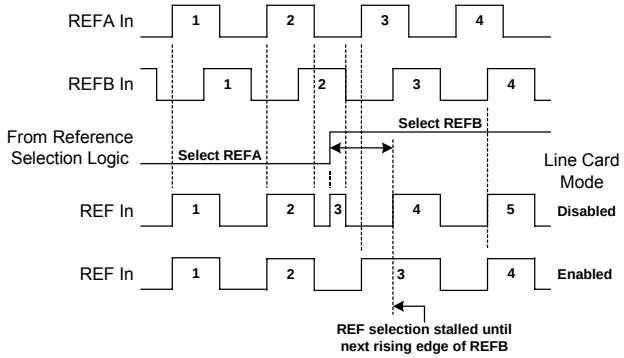


Figure 21: Reference Switchover Timing

HOLDOVER

Holdover Control

Holdover functionality provides the user with a means of maintaining the output clock signal even in the absence of a reference signal at the REF A or B input. In holdover mode, the output clock is generated from the SysClk input (via the DDS) by directly applying a frequency tuning word to the DDS.

Transfer from normal operation to holdover mode may be accomplished either manually or automatically by appropriately programming the "Automatic Holdover" bit (0=Manual, 1=Auto). The actual transfer to holdover operation, however, depends on the state of the HOLDOVER pin and the state of control register bits "Enable Holdover Override" and "Holdover On/Off".

Manual holdover is established when the “Automatic Holdover” bit is a logic 0 (default). In manual mode, holdover is determined by the state of the HOLDOVER pin (0=Normal, 1=Holdover). The HOLDOVER pin is configured as a high impedance (>100kΩ) *input* pin in order to accommodate manual holdover operation.

Automatic holdover is invoked when the “AutoHold" bit is a logic 1. In automatic mode, the HOLDOVER pin is configured as a low impedance *output* with its logic state indicating the holdover state as determined by the internal state machine (0=Normal, 1=Holdover).

In automatic holdover operation the user may override the internal state machine by programming the "Override HldPin" bit to a logic 1 and the "Hldovr" bit to the desired state (0=Normal, 1=Holdover). However, the HOLDOVER pin does

not indicate the "forced" holdover state in the override condition, but continues to indicate the holdover state as chosen by the internal state machine (even though the state machine choice is overridden). This allows the user to force a holdover state by means of the programming registers while monitoring the response of the state machine via the HOLDOVER pin. A diagram of the reference switchover and holdover logic is shown in Figure 19 on Page 30.

NOTE: The default state for the reference switchover bits is AutoHold=0, Override HldPin=0, and Hldovr=0.

Holdover & Reference Switchover State Machine

The interplay between the input reference signals and holdover is in Figure 22. The various control signals and the four states are shown.

States 1 or 2 are in effect when the device is not in the holdover condition, while states 3 & 4 are in effect when the holdover condition is active. When REF A is selected as the "active" reference, then states 1 or 3 are in effect. When REF B is selected as the "active" reference, then states 2 or 4 are in effect. A transition between states depends on the reference switchover and holdover control register settings, the logic state of the REFSELECT and HOLDOVER pins, and the occurrence of certain events (e.g., a reference failure).

The state machine and its relationship to control register and external pin stimuli are shown below. The state machine generates a "derived" reference selection and holdover state. The actual control signal sent to the reference switchover logic and the holdover logic, however, depends on the control signals applied to the MUXes. The "dashed" path leading to the REFSELECT and HOLDOVER pins is active when the "auto" mode is selected for reference selection and/or holdover assertion.

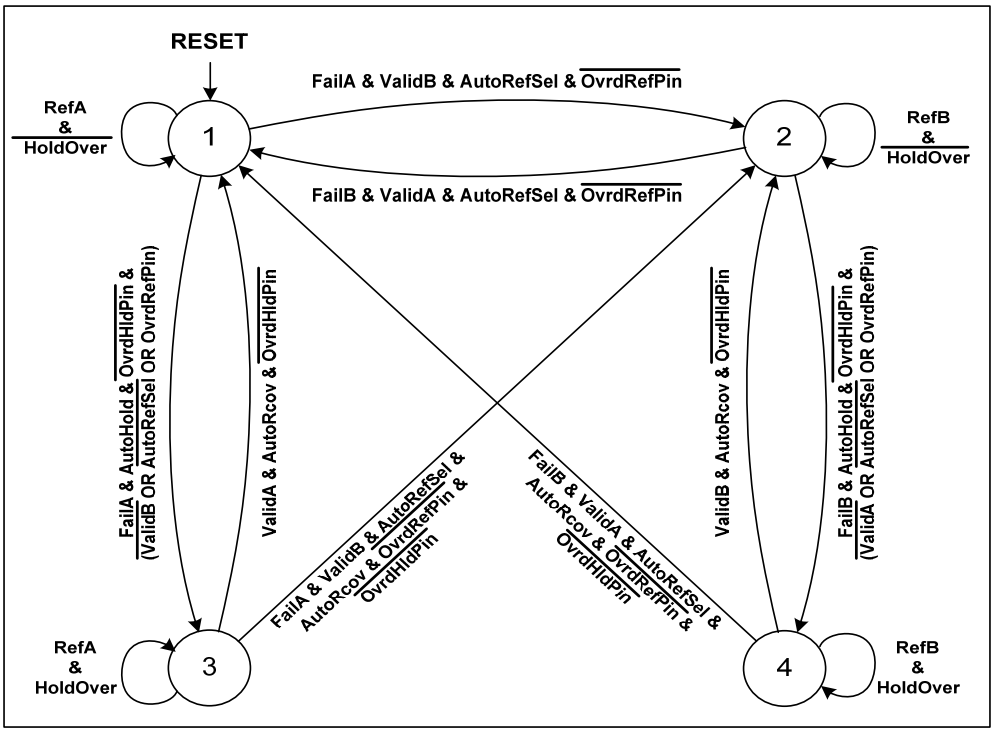


Figure 22: Holdover state diagram

Abbreviation Key			
RefA:	**Reference A selected**	**OvrdRefPin:**	**Override REF SEL pin**
RefB:	**Reference B selected**	**OvrdHldPin:**	**Override HOLDOVER pin**
HoldOver:	**Holdover state**	**AutoRefSel:**	**Automatic reference select**
FailA:	**Reference A failed**	**AutoRcov:**	**Automatic holdover recovery**
FailB:	**Reference B failed**	**AutoHold:**	**Automatic holdover entry**
ValidA:	**Reference A validated**	**||**	**Logical OR**
ValidB:	**Reference B validated**	**&**	**Logical AND**
		%	**Logical NOT**

Figure 23: Holdover State Diagram Abbreviation Key

Reference Validation Timers

Each of the two reference inputs has a dedicated validation timer. The status of these timers is used by the holdover state machine as part of the decision making process for reverting to a previously faulty reference. For example, suppose that a reference fails (i.e., an LOR or OOL condition is in effect) and that the device is programmed to revert automatically to a valid reference when it recovers. When a reference returns to normal operation, the LOR and OOL conditions will no longer be true. However, the state machine is not immediately notified of the clearing of the LOR and OOL condition. Instead, once both the LOR and OOL conditions are cleared, the validation timer for that particular reference is started. Expiration of the validation timer is an indication to the state machine that the reference is now available for selection. However, even though the reference is now flagged as "valid", actual transition to the recovered reference depends on the programmed settings of the various holdover control bits.

The validation timers are controlled via the I/O Register Map. The user should be careful to make sure the validation timer is at least two periods of the reference clock. Although there are two independent validation timers, the programmed information is shared among both. The desired time interval is controlled via a 5-bit word (T) such that $0 \le T \le 31$ (default is T=0). The duration of the validation timers is given by:

$$T_{RECOVER} = T_0\left(2^{T+1} - 1\right)$$

Where T_0 is the sample rate of the digital loop filter, whose period is:

$$T_0 = \frac{2^{P_{IO}}}{f_S}$$ (see the *Digital Loop Filter* section)

Holdover Operation

When the holdover condition is asserted, the DDS output frequency is no longer controlled by the phase lock feedback loop. Instead, a static frequency tuning word (FTW) is applied to the DDS to hold it at a specified frequency. The source of the static FTW depends on the status of the appropriate control register bits. During normal operation, the Averager & Sampler monitors and accumulates up to 65000 FTW values as they are generated, and upon entering holdover, the holdover state machine can use the averaged tuning word, or the last valid tuning word.

Holdover mode is exited in a similar manner that it is entered. If manual holdover control is used, then when the holdover pin is de-asserted, the phase detector starts comparing the holdover signal with the reference input signal, and will start to adjust the phase/frequency using the holdover signal as its starting point.

The behavior of the holdover state machine when it is in automatically exiting holdover mode is very similar. The primary difference is that reference monitor is continuously monitoring both reference inputs and as soon as one becomes valid, it automatically switches to that input.

The output frequency in Holdover mode depends on the frequency of the SysClk input source and the value of the frequency tuning word applied to the DDS. Therefore, the stability of the output signal is completely dependent on the stability of the SysClk source (and the SysClk PLL Multiplier, if enabled).

Note: It is very important to power down an unused reference input to avoid chattering on that input. Also, the reference validation timer must be set to at least one full cycle of the signal coming out of the reference divider.

Holdover Sampler and Averager

If activated via the I/O Register Map, the HSA continuously monitors the data generated by the digital loop filter in the background. It should be noted that the loop filter data is a time sequence of frequency adjustments (Δf) to the DDS. The output of the HSA is routed to a read-only register in the I/O Register Map and to the holdover control logic.

The first of these destinations (the read-only register) serves as a "trace buffer" that may be read by the user and the data processed externally. The second destination (the holdover control logic) uses the output of the HSA to "peg" the DDS at a specific frequency upon entry into the holdover state. Hence, the DDS will assume a frequency specified by the last value generated by the HSA just prior to entering the holdover state.

The state of the output MUX is established by programming the I/O Register Map. The default state is such that the Δf values pass through the HSA unaltered. In this mode, the output sample rate is f_S/P, the same as the sample rate of the digital loop filter.

NOTE: P is the divide ratio of the "P"-divider (see “Digital Loop Filter” on Page 21) and f_S is the DAC sample rate.

Alternatively, the MUX can be set to select the averaging path. In this mode, a "block average" is performed on a sequence of

samples. The length of the sequence is determined by programming the value of Y (a 4-bit number stored in the I/O Register Map), and has a value of 2^{Y+1}. In the "averaging" mode, the output sample rate is given by $f_S/(P \cdot 2^{Y+1})$.

When the number of Δf samples specified by Y has been collected, the averaged result is delivered to a 2-stage pipeline. The last stage of the pipeline contains the value that will be delivered to the holdover control logic when a transition into the holdover state occurs. The pipeline is a guarantee that the averaged Δf value delivered to the holdover control logic has not been interrupted by the transition into the holdover state.

The pipeline provides an inherent delay of $\Delta t = P \cdot 2^{Y+1}/f_S$. Hence, the DDS "hold" frequency is the average as it appeared Δt to 2Δt seconds prior to entering the holdover state. Note that the user has some control over the duration of Δt because it is dependent on the programmed value of Y.

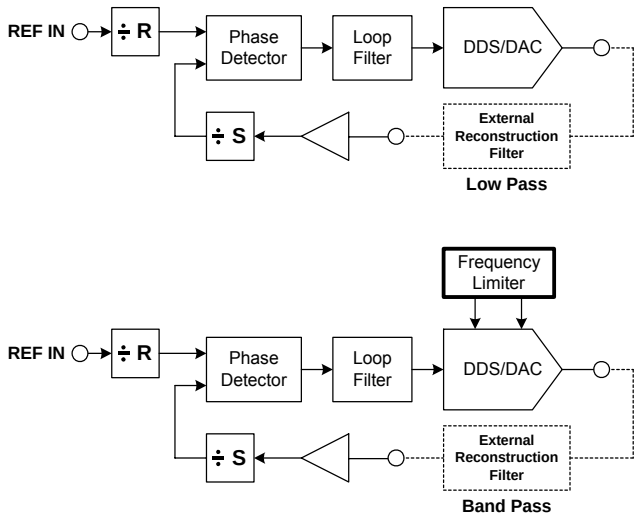


Figure 24: Application of the Frequency Limiter

OUTPUT FREQUENCY RANGE CONTROL

Under normal operating conditions, its output frequency is dynamically changing in response to the output of the digital loop filter. The loop filter can steer the DDS to any frequency between DC and $f_S/2$ (with 48-bit resolution). However, the user is given the option of placing limits on the tuning range of the DDS via two 48-bit registers in the I/O Register Map: *FTW Upper Limit* and *FTW Lower Limit*. If the tuning word input exceeds the upper or lower frequency limit boundaries, the tuning word is clipped to the appropriate value. The default setting for these registers is $f_S/2$ and DC, respectively.

It may be desirable to limit the output range of the DDS to a narrow band of frequencies (for example, to achieve better jitter performance in conjunction with a band pass filter). See "Use of Narrowband Filter for High Performance" on Page 35 for more information about this feature.

RECONSTRUCTION FILTER

The origin of the output clock signal produced by the AD9549 is the combined DDS and DAC. The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth. The signal is then brought back on-chip to be converted to a square wave that is routed internally to the output clock driver or the 2x DLL multiplier.

Since the DAC constitutes a sampled system, its output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the desired base band signal, which extends from DC to the Nyquist frequency ($f_S/2$). It also contains images of the base band signal that theoretically extend to infinity. Notice that the odd images (shown in Figure 25 below) are mirror images of the base band signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the "sample and hold" nature of the DAC output signal.

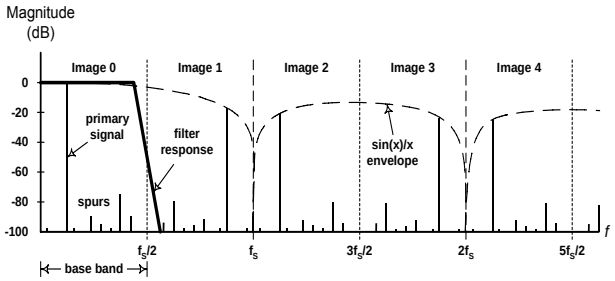


Figure 25: DAC Spectrum vs. Reconstruction Filter Response

The response of the reconstruction filter should preserve the base band signal (image 0), while completely rejecting all other images. However, a practical filter implementation will typically exhibit a relatively flat pass band that covers the desired output frequency plus 20%, roll off as steeply as possible, and then maintain significant (though not complete) rejection of the remaining images.

PLACE HOLDER

Plot 15: DAC Output without Reconstruction Filter. f_{OUT}=155.52 MHz. Sysclk=25 MHz. Sysclk PLL = x40. Spur reduction disabled. DPLL Loop Closed. Freq Span for Plot: 500 MHz.

PLACE HOLDER

Plot 16: Filtered DAC Output Using 7th order elliptical with Fc=186 MHz. Same Conditions as previous plot.

Since the DAC output signal serves as the feedback signal for the digital PLL, the design of the reconstruction filter can have a significant impact on the overall jitter performance. Hence, good filter design and implementation techniques are important for obtaining the best possible jitter results.

Use of Narrowband Filter for High Performance

A distinct advantage of the AD9549 architecture is its ability to constrain the frequency output range of the DDS. This allows the user to employ a narrow band reconstruction filter instead of the low pass response shown above resulting in less jitter on the output. For example, suppose that the nominal output frequency of the DDS is 150MHz. One might then choose a 5MHz narrow band filter centered at 150MHz. By using the AD9549's DDS frequency limiting feature, the user could constrain the output frequency to 150MHz ± 4.9MHz (which allows for a 100kHz margin at the pass band edges). This will ensure that a feedback signal is always present for the digital PLL. Such a design would be extremely difficult to implement with conventional PLL architectures.

FDBK INPUTS

The FDBK pins serve as the input to the feedback path of the digital PLL. Typically, these pins are used to receive the signal generated by the DDS after it has been band-limited by the external reconstruction filter.

A diagram of the FDBK input pins is provided here, which includes some of the internal components used to bias the input circuitry. Note that the FDBK input pins are internally biased to a DC level of ~1V. Care should be taken to ensure that any external connections do not disturb the DC bias, as this may significantly degrade performance.

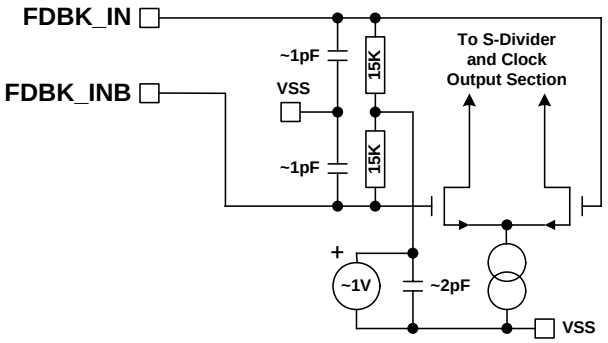


Figure 26: Differential FDBK Inputs

REFERENCE INPUTS

Reference Clock Receiver

The Reference Clock receiver is the point at which the user supplies the input clock signal that the Synchronizer will synthesize into an output clock. The clock receiver circuit is able to handle a relatively broad range of input levels as well as frequencies from 8 kHz up to 750 MHz.

The following is a diagram of the REFA/B input pins, which includes some of the internal components used to bias the input circuitry. Note that the REF input pins are internally biased by a DC source, V_b. Care should be taken to ensure that any external connections do not disturb the DC bias, as this may significantly degrade performance.

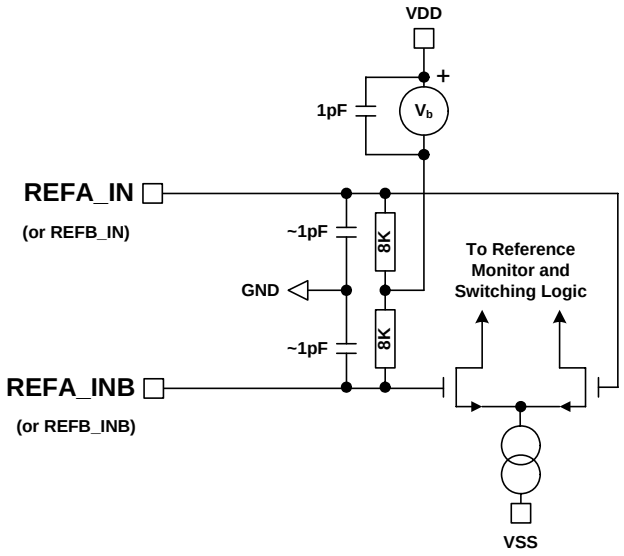


Figure 27: Reference Inputs

NOTE: Support for redundant reference clocks is achieved by using the two Reference Clock receivers (REFA & REFB).

In order to accommodate a variety of input signal conditions the value of V_b is programmable via a pair of bits in the I/O Register Map. Table 3 below gives the value of V_b for the bit pattern in Register 040F.

Reference Bias Level R040F[1:0]	V_b
00 (default)	AVDD3-800mV
01	AVDD3-400mV
10	AVDD3-1600mV
11	AVDD3-1200mV

Table 3: Setting of Input Bias Voltage (V_b)

SYSCLK INPUTS

Functional Description

The SysClk pins are where an external timebase is connected to the AD9549 for generating the internal high frequency system clock (f_S).

The SysClk inputs can be operated in one of three modes: 1) SysClk PLL Bypassed, 2) SysClk PLL Enabled with input signal generated externally, or 3) Crystal Resonator with SysClk PLL Enabled. A functional diagram of the system clock generator is shown in Figure 28 on Page 37.

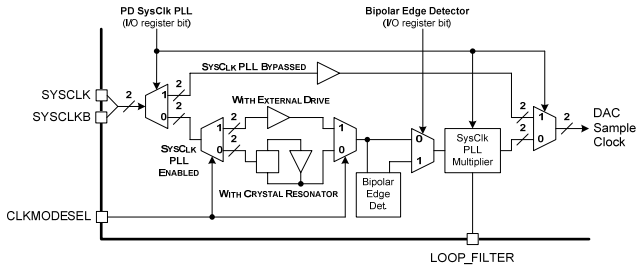


Figure 28: System Clock Generator Block Diagram

The SysClk PLL multiplier path is enabled by a logic 0 (default) in the *PD SysClk PLL* location of the I/O Register Map. The SysClk PLL multiplier can be driven from the SysClk input pins by one of two means depending on the logic level applied to the 1.8V CMOS CLKMODESEL pin. When CLKMODESEL=0, a crystal can be connected directly across the SysClk pins. When CLKMODESEL=1, the maintaining amp is disabled, and an external frequency source (oscillator, signal generator, etc.) can be connected directly to the SysClk input pins. Note that CLKMODESEL=1 does not disable the system clock PLL.

When the SysClk PLL multiplier path is disabled, the AD9549 must be driven by a high frequency signal source (up to 1GHz). The signal thus applied to the SysClk input pins becomes the internal DAC sampling clock (f_S) after passing through an internal buffer.

Bipolar Edge Detector

The SysClk PLL Multiplier path offers an optional Bipolar Edge Detector (BED). This block acts as a frequency doubler by generating a pulse on each edge of the SysClk input signal. The SysClk PLL Multiplier locks to the falling edges of this regenerated signal.

The impetus for doubling the frequency at the input of the SysClk PLL Multiplier is that an improvement in overall phase noise performance can sometimes be realized. The main drawback is that the BED output not a rectangular pulse with a constant duty cycle even for a perfectly symmetric SysClk input signal. This results in a sub-harmonic appearing at the same frequency as the SysClk input signal, and the magnitude of the sub-harmonic can be quite large. When employing the BED care must be taken to ensure that the loop bandwidth of the SysClk PLL Multiplier will adequately suppress the sub-harmonic.

The benefit offered by the BED depends on the magnitude of the sub-harmonic, the loop bandwidth of the SysClk PLL Multiplier, and the overall phase noise requirements of the specific application. In many applications, the AD9549 clock output is applied to the input of another PLL, and the sub-harmonic is often suppressed by the relatively narrow bandwidth of the downstream PLL.

NOTE: Generally, the benefits of the Bipolar Edge Detector are realized for SysClk input frequencies of 25MHz and above.

SysClk PLL Multiplier

When the SysClk PLL Multiplier path is employed, the frequency applied to the SysClk input pins must be limited so as not to exceed the maximum input frequency of the SysClk PLL phase detector. A block diagram of the SysClk generator appears in Figure 29 below.

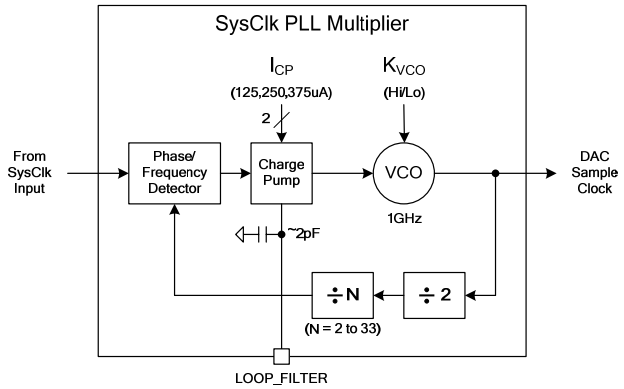


Figure 29: Block Diagram of the SysClk PLL

The SysClk PLL Multiplier has a 1GHz VCO at its core. A phase/frequency detector (PFD) and charge pump provide the steering signal to the VCO in typical PLL fashion. The PFD operates on the falling edge transitions of the input signal, which means that the loop locks on the negative edges of the reference signal. The charge pump gain is controlled via the I/O Register Map by selecting one of three possible constant current sources ranging from 125-375µA in 125µA steps. The center frequency of the VCO is also adjustable via the I/O Register Map and provides high/low gain selection. The feedback path from VCO to PFD consists of a fixed divide-by-2 prescaler followed by a programmable divide-by-N block, where $2 \le N \le 33$. This limits the overall divider range to any *even* integer from 4 to 66, inclusive. The value of N is programmed via the I/O Register Map via a 5-bit word that spans a range of 0 to 31, but the internal logic automatically adds a bias of 2 to the value entered, extending the range to 33. Care should be taken when choosing these values so as to not exceed the maximum input frequency of the Sysclk PLL phase detector or bipolar edge detector. These values can be found in the AC Electrical Characteristics section of this datasheet.

External Loop Filter (SysClk PLL)

The loop bandwidth of the SysClk Multiplier PLL can be adjusted by means of three external components as shown in the diagram below. The nominal gain of the VCO is 800MHz/V. The recommended component values are shown in Table 4 below. They establish a loop bandwidth of approximately 1.6MHz with the charge pump current set to 250µa. The default case is N=40, and assumes a 25MHz SysClk input frequency and generates an internal DAC sampling frequency (f_S) of 1GHz.

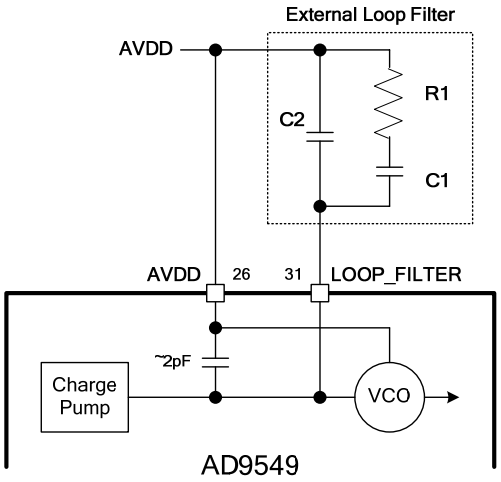


Figure 30: External Loop Filter for SysClk PLL

Sysclk Multiplier	R1	Series C1	Shunt C2
< 8	390Ω	1 nF	82 pF
10	470Ω	820pF	56 pF
20	1kΩ	390pF	27 pF
40 (default)	2.2kΩ	180 pF	10 pF
60	2.7kΩ	120 pF	5 pF

Table 4: Recommended Loop Filter Values for a nominal 1.5MHz Sysclk PLL loop Bandwidth

Detail of SysClk Differential Inputs

A diagram of the SysClk input pins is provided here. Included are details of the internal components used to bias the input circuitry. These components have a direct effect on the static levels at the SysClk input pins. This information is intended to aid in determining how best to interface to the device for a given application.

Note that the SysClk PLL Bypassed and SysClk PLL Enabled input paths are internally biased to a DC level of ~1V. Care should be taken to ensure that any external connections do not disturb the DC bias, as this may significantly degrade performance. Generally, it is recommended that the SysClk inputs be AC coupled to the signal source (except when using a crystal resonator).

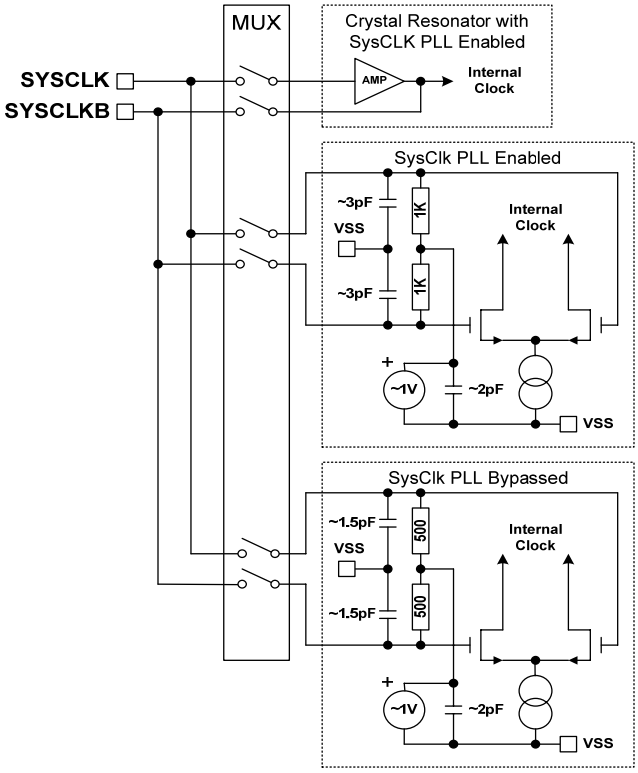


Figure 31: Differential SysClk Inputs

HARMONIC SPUR REDUCTION

The most significant spurious signals produced by the DDS are harmonically related to the desired output frequency of the DDS. The source of these harmonic spurs can usually be traced to the DAC, and the spur level is in the -60dBc range. This ratio represents a level that is about 10 bits below the full-scale output of the DAC (10 bits down is 2^{-10}, or 1/1024).

To reduce such a spur would require combining the original signal with a replica of the spur but offset in phase by 180°. This idea is the foundation of the technique used to reduce harmonic spurs in the AD9549. Since the DAC has 14-bit resolution, a -60dBc spur can be synthesized using only the lower 4 bits of the DAC full scale range. That is, the 4 LSBs can create an output level approximately 60dB below the full scale level of the DAC (commensurate with a -60dBc spur). This fact gives rise to a means of digitally reducing harmonic spurs or their aliased images in the DAC output spectrum by digitally adding a sinusoid at the input of the DAC with similar magnitude as the offending spur but shifted in phase to produce destructive interference.

Although the worst spurs tend to be harmonic in origin, the fact that the DAC is part of a sampled system results in the possibility of some harmonic spurs to appear in non-harmonic locations in the output spectrum. For example, if the DAC is sampled at 1 GHz and generates an output sinusoid of 170 MHz, the 5th harmonic would normally be at 850 MHz. However, because of the sampling process, this spur appears at 150 MHz, only 20 MHz away from the fundamental. Hence, when attempting to reduce DAC spurs it is important to know the actual location of the harmonic spur in the DAC output spectrum based on the DAC sample rate so that its harmonic number can be reduced.

The mechanics of performing harmonic spur reduction is shown in figure below. It essentially consists of two additional DDS cores operating in parallel with the original DDS. This enables the user to reduce two different harmonic spurs from the 2nd to the 15th with 9 bits of phase offset control (±π) and 8 bits of amplitude control.

The dynamic range of the cancellation signal is further augmented by a *gain* bit associated with each channel. When this bit is set, the magnitude of the cancellation signal is doubled by employing a 1-bit left-shift of the data. However, the shift operation reduces the granularity of the cancellation signal magnitude.

NOTE: Full-scale amplitude of a cancellation spur is approximately -60dBc when the gain bit is a logic 0 and approximately -54dBc when the gain bit is a logic 1.

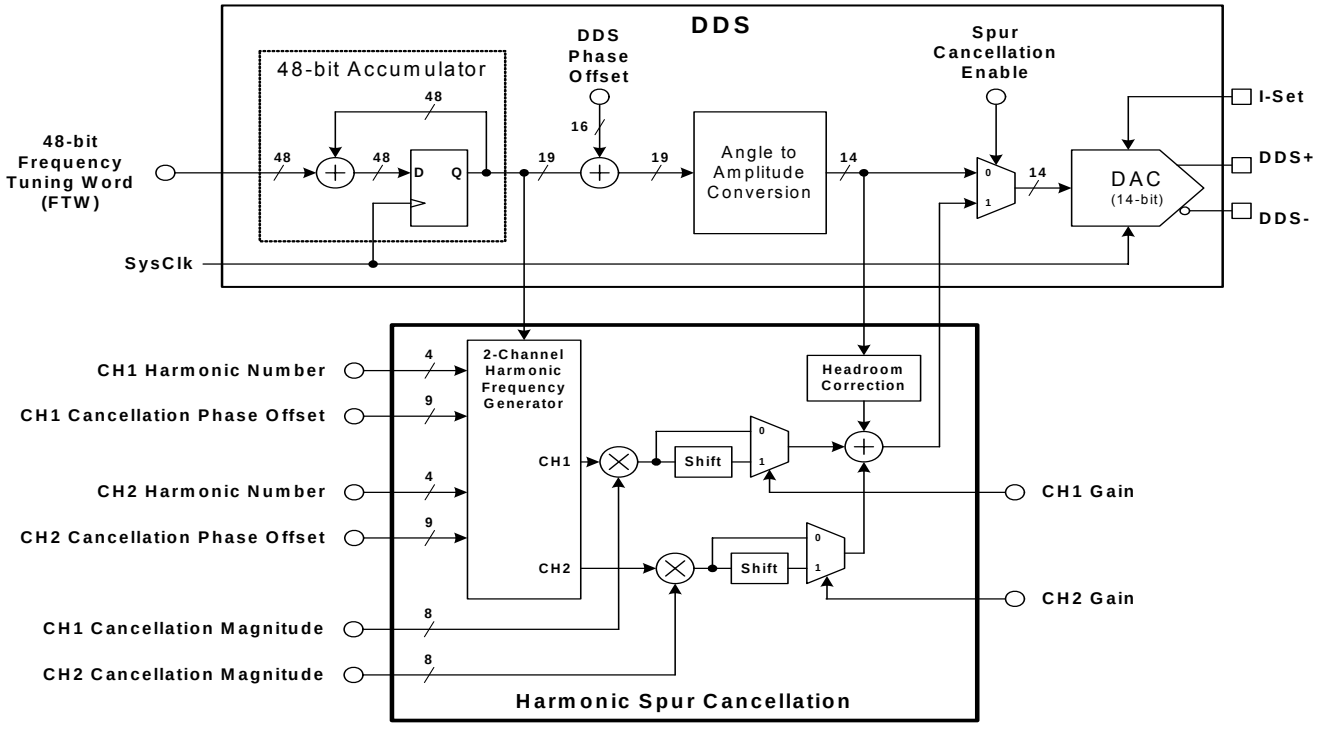


Figure 32: Spur Reduction Technique

OUTPUT CLOCK DRIVERS & 2X FREQUENCY MULTIPLIER

There are two output drivers provided by the AD9912. The primary supports differential 1.8V HSTL output levels while the secondary supports either 1.8V or 3.3V CMOS levels, depending on whether Pin 37 is driven at 1.8 or 3.3V.

The primary differential driver nominally provides an output voltage with 100Ω load applied differentially (V_{DD}-V_{SS}=1.8V). The source impedance of the driver is approximately 100Ω for most of the output clock period; during transition between levels, the source impedance reaches a maximum of about 500 ohms. The driver is designed to support output frequencies of up to and beyond the OC-12 network rate of 622.08MHz.

The output clock may also be powered down by a control bit in the I/O Register Map.

Primary 1.8V Differential HSTL Driver

The DDS produces a sinusoidal clock signal that is sampled at the system clock rate. This DDS output signal is routed off-chip where it is passed through an analog filter and brought back on-chip for buffering and, if necessary, frequency doubling. Where possible, for the best jitter performance, it is recommended that the upconverter be bypassed.

The 1.8V HSTL output driver should be AC-coupled, with 100Ω termination at the destination. The driver design has low jitter injection for frequencies in the range of 50 to 750 MHz. Please refer to the AC Electrical Specifications for the exact frequency limits.

2x Frequency Multiplier

The AD9549 may be configured (via the I/O Register Map) with an internal 2x Delay Locked Loop (DLL) multiplier at the input of the primary clock driver. The extra octave of frequency gain allows the AD9549 to provide output clock frequencies that exceed the range available from the DDS alone. These settings are found in Registers 0010 and 0200.

The input to the DLL consists of the filtered DDS output signal after it has been "squared up" by an integrated clock receiver circuit. The DLL can accept input frequencies in the range of 200MHz to 400MHz.

Single-Ended CMOS Output

In addition to the high speed differential output clock driver, the AD9549 provides an independent, single-ended output, CMOS clock driver. It serves as a relatively low speed (<50MHz) clock source. The origin of the signal generated by the CMOS clock driver is determined by the appropriate control bits in the I/O Register Map. The user may select one of two sources under program control.

One source is the signal generated by the DDS after it has been externally filtered and brought back on-chip. In this configuration, the CMOS clock driver generates the same frequency as appears at the output of the DDS.

NOTE: In this configuration, the DDS output frequency must not exceed 50MHz.

The other source is the output of the feedback divider (S-divider). In this configuration, the CMOS clock driver generates the same frequency as the input reference after optional prescaling by the R-divider (i.e., $f_{CMOS}=f_R/R$) which is inherently limited to a maximum of 25 MHz.

FREQUENCY SLEW LIMITER

The AD9549 offers frequency slew limiting capability enabling users to specify the maximum rate of frequency change that appears at the output. The function is programmable via the I/O Register Map. Program control a bit to enable/disable the function (default condition is *disable*) and a register that sets the desired slew rate.

The frequency slew limiter is located between the digital loop filter and the CCI filter as shown in the diagram below.

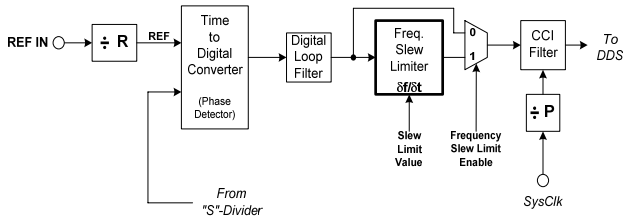


Figure 33: Frequency Slew Limiter

The frequency slew limiter sets a boundary on the rate of change of the output frequency of the DDS. The frequency slew limiting constant, K_{SLEW}, is a 48-bit value stored in the I/O Register Map. The value of the constant is determined by:

$$K_{SLEW} = round\left[\left(\frac{2^{48+P_{IO}}}{{f_S}^2}\right)\frac{\delta f}{\delta t}\right]$$

Where P_{IO} is the value stored in the I/O Register Map for the "P"-Divider, f_S is the DAC sample rate, and $\delta f/\delta t$ is the desired frequency slew rate limitation. For example, suppose that f_S=1GHz, P_{IO}=9 and $\delta f/\delta t$=5kHz/second, then:

$$K_{SLEW} = round\left[\left(\frac{2^{48+9}}{(10^9)^2}\right)\left(5\cdot 10^3\right)\right] = 721$$

The resulting slew rate can be calculated as:

$$\frac{\delta f}{\delta t} = K_{SLEW}\left(\frac{{f_S}^2}{2^{48+P_{IO}}}\right)$$

The above example yields: $\delta f/\delta t$=5.003kHz/s

FREQUENCY ESTIMATOR

The AD9549 has a frequency estimation function that will automatically set the DDS output frequency so that the feedback frequency (f_{DDS}/S) and the prescaled reference frequency (f_{REF_IN}/R) are matched within an error tolerance (ε_0). It's primary purpose is to allow the PLL to quickly lock when the reference frequency is not known. The error tolerance is defined as a fractional error and is controlled by a 16-bit programmable value (K) via the I/O Register Map.

The precision of any frequency measurement is dependent on two factors:

the timing resolution of the measurement device (δt)

the duration of the measurement (T_{meas})

The frequency estimator uses f_S as its measurement reference, so $\delta t=1/f_S$ (i.e., δt=1ns for a 1GHz DAC sample rate). The duration of the measurement is controlled by K, which establishes a measurement interval that is K cycles of the measured signal such that $T_{meas}=KR/f_{REF\_IN}$.

The frequency estimator uses a 17-bit counter to accumulate the number δt periods within the measurement interval. The finite capacity of the counter puts an upper limit on the duration of the measurement, which is constrained to $T_{max}=2^{17}/f_S$. If f_S=1GHz, then this equates to ~131µs. The fact that the measurement time is bounded by T_{max} means there is a limit to the largest value of K (K_{MAX}) that can be used without causing the counter to overflow. The value of K_{MAX} is given by:

$$K_{MAX} = floor\left(\frac{65535}{\rho}\right) \text{ where } \rho = \frac{f_S R}{f_R}$$

R is the modulus of the feedforward divider and f_R is the input reference frequency.

The measurement error (ε) associated with the frequency estimator depends on the choice of the measurement interval parameter (K). These are related by:

$$\varepsilon = \frac{\rho K}{floor(\rho K)-1} - 1$$

With a specified fractional error (ε_0), only those values of K for which $\varepsilon \le \varepsilon_0$ result in a frequency estimate that meets the requirements. A plot of ε versus K (for a given ρ) takes on the general form shown below.

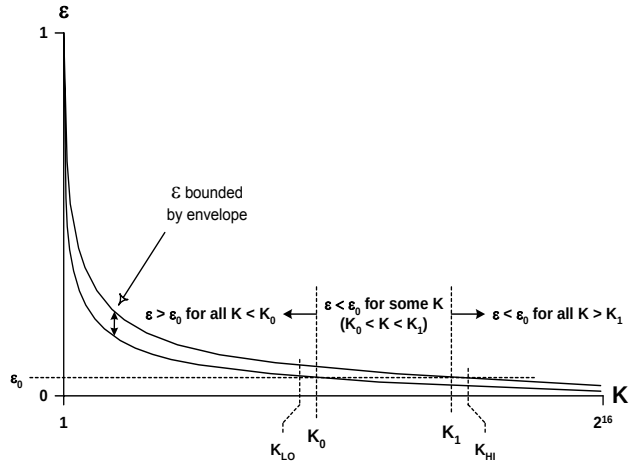


Figure 34: Frequency Estimator ε vs. K

An iterative technique is necessary to determine the exact values of K_0 and K_1. However, a closed form exists for a conservative estimate of K_0 (K_{LO}) and K_1 (K_{HI}):

$$K_{LO} = ceil\left[\frac{1}{\rho}\left(1+\frac{1}{\varepsilon_0}\right)\right]$$

$$K_{HI} = ceil\left[\frac{2}{\rho}\left(1+\frac{1}{\varepsilon_0}\right)\right]$$

As an example, consider the system conditions specified below:

f_S = 400MHz f_{REF_IN} = 155.52MHz

R = 8 ε_0=0.00005 (i.e., 50ppm)

These conditions yield K_{MAX}=3185, which is the largest K value that can be programmed without causing the frequency estimator counter to overflow. With K=K_{MAX} we find that T_{meas}=163.84µs and ε=30.2ppm. K_{MAX} will generally (but not always) yield the smallest value of ε, but this comes at the cost of the largest measurement time (T_{meas}).

If the measurement time must be reduced, then K_{HI} can be used instead of K_{MAX}. This yields: K_{HI}=1945, T_{meas}=100.05µs, and ε=39.4ppm.

The measurement time can be further reduced (though marginally) by using K_1 instead of K_{HI}. K_1 is found by solving the $\varepsilon \le \varepsilon_0$ inequality iteratively. To do so, start with K=K_{HI} and *decrement* K successively while evaluating the inequality for each value of K. Stop the process the first time that the inequality is no longer satisfied and add 1 to the value of K thus obtained. The result is the value of K_1. For the above example, K_1=1912, T_{meas}=98.35µs, and ε=39.8ppm.

If a further reduction of the measurement time is necessary, then K_0 can be used. K_0 is found in a manner similar to K_1. Start with K=K_{LO} and *increment* K successively while evaluating the inequality for each value of K. Stop the process the first time that the inequality is satisfied. The result is the value of K_0. For the above example, K_0=1005, T_{meas}=51.70µs and ε=49.0ppm.

STATUS AND WARNINGS

Status Pins

Four pins (S1 – S4) are reserved for providing device status information to the external environment. These four pins are individually programmable (via the serial I/O port) as an OR'd combination of six possible status indications. Each pin has a dedicated group of control register bits that determine which internal status flags are used to provide an indication on a particular pin (as shown in the diagram below).

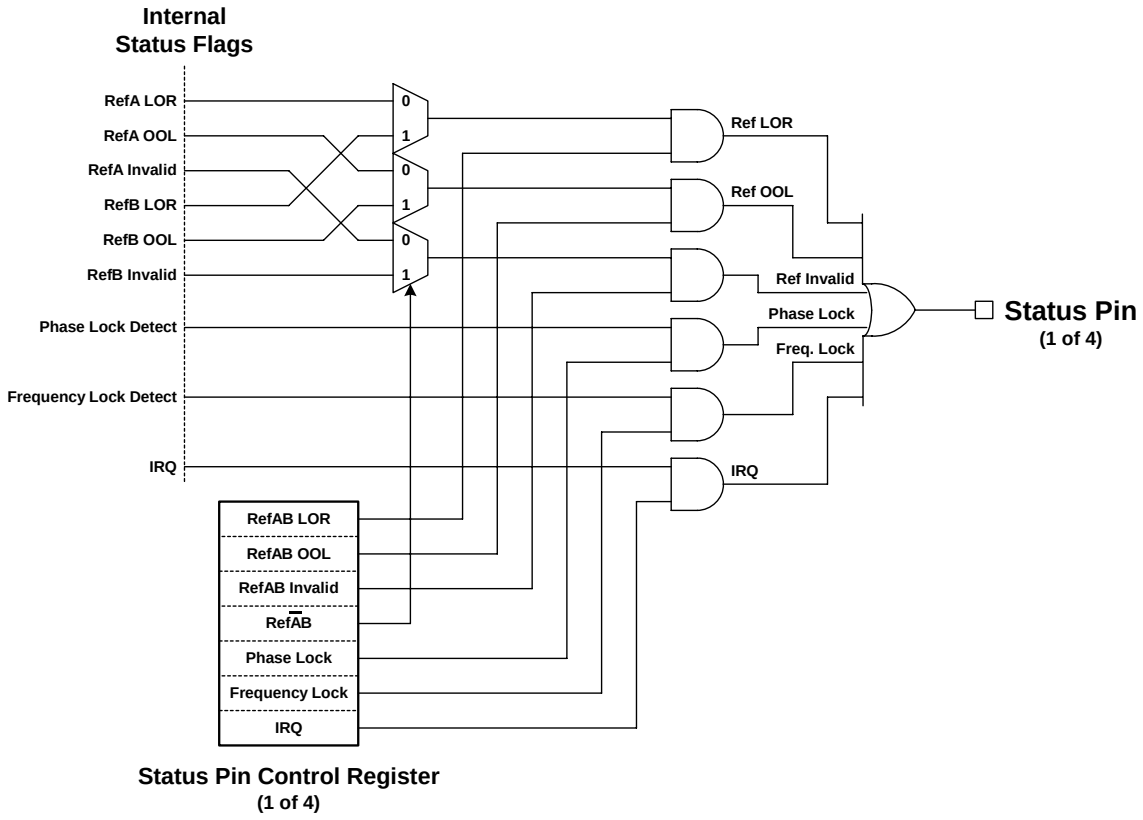


Figure 35: Status Pin Control

Reference Monitor Status

In the case of reference monitoring status information, a pin can be programmed for either RefA or RefB, but not both. In addition, the OR'd output configuration allows the user to combine multiple status flags into a single status indication. For example, if both the LOR and OOL control register bits are true, then the status pin associated with that particular control register will give an indication if either the LOR *or* OOL status flag is asserted for the selected reference (A or B).

Default DDS Output Frequency on Power-Up

The four Status Pins (S1-S4) provide a completely separate function at power-up. They can be used to define the output frequency of the DDS at power-up even though the I/O Registers have not yet been programmed. This is made possible because the status pins are designed with bi-directional drivers. At power-up, internal logic initiates a reset pulse of about 10 ns. During this time, S1-S4 briefly function as input pins, and can be driven externally. Any logic levels thus applied are transferred to a 4-bit register on the falling edge of the internally initiated pulse. The falling edge of the pulse also returns S1-S4 to their normal function as output pins. The same behavior occurs when the RESET pin is asserted manually.

Setting up S1-S4 for default DDS start-up is accomplished by connecting a resistor to each pin (either pull-up or pull-down) to produce the desired bit pattern, yielding 16 possible states that are used both to address an internal 8x16 ROM and to select the SysClk Mode (see Table 5). The ROM contains eight 16-bit DDS frequency tuning words (FTWs), one of which is selected by the state of the S1-S3 pins. The selected FTW is transferred to the FTW0 register in the I/O Register Map without the need for an "I/O_Update". This ensures that the DDS generates the selected frequency even if the I/O registers have not been programmed. The state of the S4 pin selects whether the internal System Clock is generated by means of the internal SysClk PLL multiplier or not (see the *SysClk Input* section for details).

The DDS output frequency listed in Table 5 assumes that the internal DAC sampling frequency (f_S) is 1GHz. These frequencies scale 1:1 with f_S, meaning that other startup frequencies are available by varying the Sysclk frequency.

At startup, the internal frequency multiplier defaults to 40x when the Xtal/PLL Mode is selected via the Status Pins.

Note: when using this mode, the digital PLL loop is still open, and the AD9549 is acting as a frequency synthesizer. The frequency dividers and DPLL loop filter must still be programmed prior to closing the loop.

Status Pin				SysClk Input Mode	Output Frequency in MHz
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal /PLL	38.87939
0	0	1	0	Xtal /PLL	51.83411
0	0	1	1	Xtal /PLL	61.43188
0	1	0	0	Xtal /PLL	77.75879
0	1	0	1	Xtal /PLL	92.14783
0	1	1	0	Xtal /PLL	122.87903
0	1	1	1	Xtal /PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Table 5: Default Power-up Frequency Options for 1 GHz System Clock

Interrupt Request (IRQ)

Any one of the four status pins (S1-S4) may be programmed as an IRQ pin. If a status pin is programmed as an IRQ pin, then the state of the internal IRQ flag appears on that pin. An IRQ flag is internally generated based on the *change of state* of any one of the internal status flags. The individual status flags are routed to a read-only I/O register (Status Register) so that the user may interrogate the status of any of these flags at any time. Furthermore, each status flag is monitored for a change in state. In some cases, only a change of state in one direction is necessary (e.g., the Frequency Estimate Done flag), but in most

cases, the status flags are monitored for a change of state in either direction (see the diagram below).

Whether or not a particular state change is allowed to generate an IRQ is dependent on the state of the bits in the IRQ Mask Register. The user programs the mask to enable those events, which are to constitute cause for an IRQ. If an unmasked event occurs, it will trigger the IRQ latch and the IRQ Flag will be asserted (active high). The state of the IRQ Flag is made available externally via one of the programmable status pins (see the *Status Pins* section of this document).

The automatic assertion of the IRQ Flag causes the contents of the Status Register to be transferred to the IRQ Register. The user can then read the IRQ Register any time after the indication of an IRQ event (i.e., assertion of the IRQ Flag). By noting the bits in the IRQ Register that is set, the cause of the IRQ event can be determined.

Once the IRQ Register has been read, the user must set the IRQ Reset bit in the appropriate control register via the serial I/O port. This restores the IRQ Flag to its default state, clears the IRQ status register, and resets the edge detection logic that monitors the status flags in preparation for the next state change.

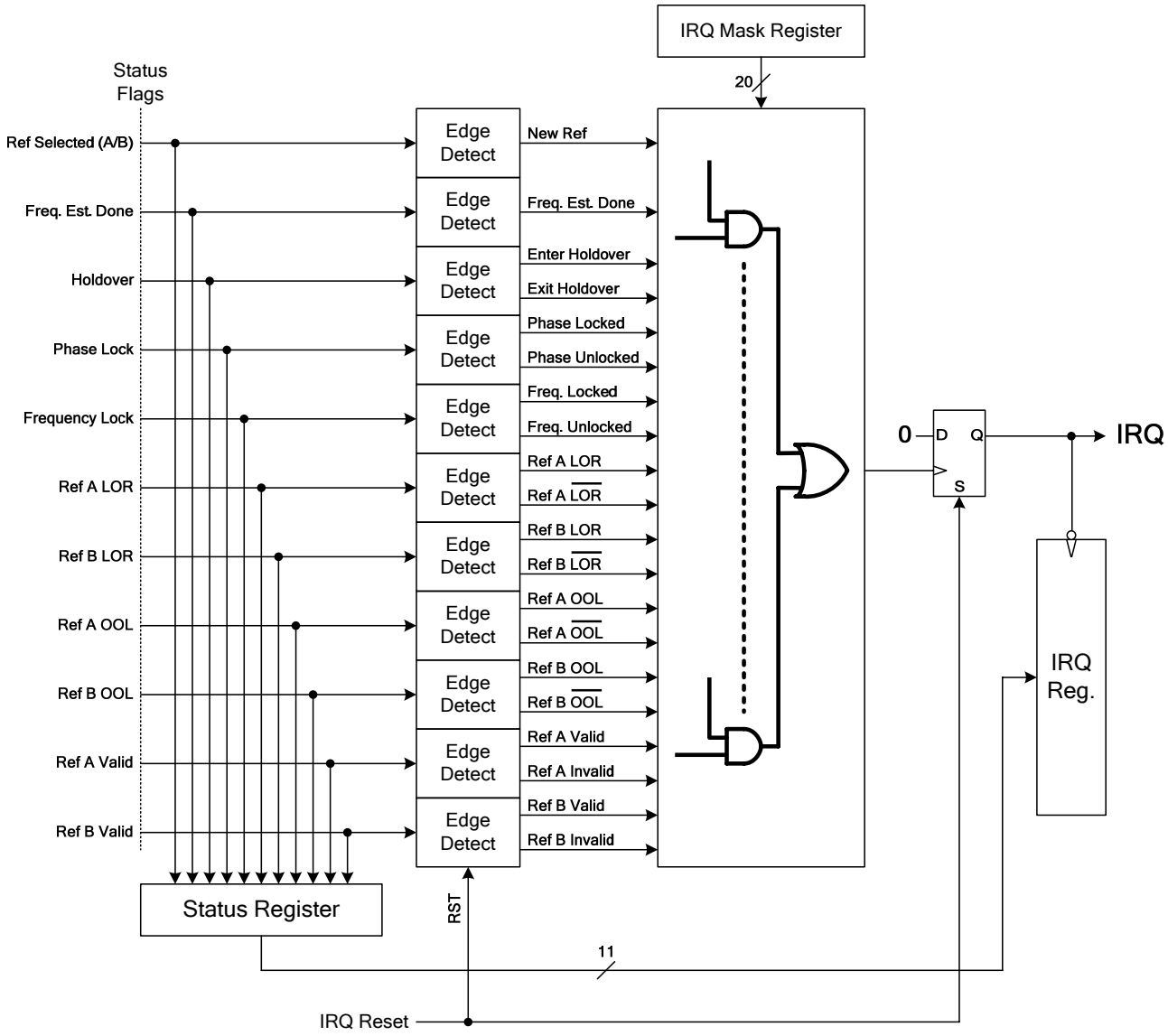


Figure 36: Interrupt Request Logic

POWER-ON RESET

On initial power-up, the AD9549 internally generates a 75ns RESET pulse. The pulse is initiated when both of the following two conditions are met:

The 3.3v supply is greater than 2.35± 0.1V

The 1.8v supply is greater than 1.4± 0.05V

Less than 1 ns after RESET goes high, the S1-S4 configuration pins go high impedance, and remain high impedance until RESET is deactivated. This allows strapping and configuration during RESET.

Because of this reset sequence, power supply sequencing isn't critical.

AD9549 POWER UP AND PROGRAMMING SEQUENCE

The following sequence should be followed when initializing the AD9549:

1. Apply Power. The AD9549 will perform an internal reset.
2. IMPORTANT: Make sure the desired configuration registers have Single Tone mode(R0100[5]) set, and Lock Loop (R0100[0]) cleared. If the Lock Loop bit is set on initial loading, the AD9549 will attempt to lock the loop before it has been configured.
3. Once the registered are loaded, the OOL (Out of limits) and LOR (loss of reference) can be monitored to insure that a valid reference signal is present on RefA or RefB.
4. If a valid reference is present, Register 0100 can be reprogrammed to clear Single Tone Mode and lock the loop.
5. Automatic Holdover mode can now be used to make the AD9549 immune to any disturbance on the reference inputs.

The following sequence should be followed when changing frequencies the AD9549:

1. Open the loop and enter single tone mode via Register 0100.
2. Enter the new register settings.
3. Write 1E to Register 0012.
4. Once the registered are loaded, the OOL (Out of limits) and LOR (loss of reference) can be monitored to insure that a valid reference signal is present on RefA or RefB.
5. If a valid reference is present, Register 0100 can be reprogrammed to clear Single Tone Mode and lock the loop.
6. Automatic Holdover mode can now be used to make the AD9549 immune to any disturbance on the reference inputs.

Notes:

Attempting to lock the loop without a valid reference can put the AD9549 into a state that requires a reset.

Automatic Holdover mode is not available unless the loop has been successfully closed.

If the user desires to open and close the loop manually, we recommend writing 1E to Register 0012 prior to reclosing the loop.

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POWER MANAGEMENT

The AD9549 features multiple power supplies, and their power consumption varies with its configuration. This section covers which power supplies can be grouped together, and how each block's power consumption varies with frequency.

The numbers quoted here are for comparison only. Please refer to the spec table for exact numbers. With each group, bypass caps of 1 uF in parallel with a 10 uF should be used.

The recommendations here are for typical applications, and an application demanding the highest performance may require additional power supply isolation.

3.3V SUPPLIES

Digital I/O (Pin 1) and VDDX_REF (Pin 14): These two 3.3V supplies can be grouped together. The power consumption on Pin 1 varies dynamically with serial port activity. Noise from the serial port that couples into the reference input should be filtered by the digital PLL.

AVDD3 (Pin 37): This is the CMOS driver supply. If the CMOS driver will be used, this supply should be isolated from other 3.3V supplies to avoid a spur at the output frequency. The power consumption is a function of the output frequency and loading of this pin. If this supply will not be used, this supply can be tied to other 3.3V supplies, and its consumption will be less than 5 mA.

AVDD3 (Pins 46,47,49): These are 3.3V DAC power supplies that typically consume about 25mA. At a minimum, a ferrite bead should be used to isolate these from other 3.3V supplies, with a separate regulator being ideal.

1.8V SUPPLIES

Digital Core (Pins 3,5,7): These Pins can be grouped together. Their current consumption increases from about 160mA at a system clock of 700 MHz to about 220mA a system clock of 1 GHz. There is also a slight (~5%) increase as Fout increases from 50 MHz to 400 MHz.

VDD DAC Decoder (Pin 53): This 1.8V supply consumes about 20 to 40 mA. It is critical that this supply be well isolated from other 1.8V supplies. At a minimum, a ferrite bead should be used for isolation, with a separate regulator being ideal.

AVDD (Pins 11, 19, 23, 24, 36, 42, 45): These pins may be grouped together and should be isolated from other 1.8V supplies. At a minimum, a ferrite bead should be used for isolation, with a separate regulator being ideal.

AVDD (Pin 25, 26, 29, 30): These pins may be grouped together and should be isolated from other 1.8V supplies. At a minimum, a ferrite bead should be used for isolation, with a separate regulator being ideal.

SERIAL CONTROL PORT

The AD9549 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9549 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts as input only or input/output. The AD9549 defaults to bidirectional pins for I/O. Alternatively, SDIO can be used as a unidirectional I/O pin by writing to the SDO active register at 00h<7> = 1b. In this case, SDIO is the input, and SDO is the output.

SDO (serial data out) is used only in the unidirectional I/O mode (00h<7> = 1) as a separate output pin for reading back data. Bidirectional I/O mode (using SDIO as both input and output) is active by default and (i.e. SDO enable register at 00h<7> = 0).

CSB (chip select bar) is an active low control that gates the read and write cycles. When CSB is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 100 kΩ resistor to 3.3V. It should not be left floating. See the Operation of Serial Control Port section on the use of the CSB in a communication cycle.

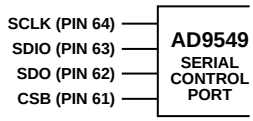


Figure 37: Serial Control Port

OPERATION OF SERIAL CONTROL PORT

Framing a Communication Cycle with CSB

A communications cycle (a write or a read operation) is gated by the CSB line. CSB must be brought low to initiate a communication cycle.

CSB stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (W1:W0 must be set to 00, 01, or 10, see Table 6 below). In these modes, CSB can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. CSB can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer. During this period, the serial control port state machine enters a wait state until all data has been sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfer or by returning the CSB low for at least one complete SCLK cycle (but less than eight SCLK cycles). Raising the CSB on a non-byte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (W1:W0 = 11b), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). CSB must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9549. The first writes a 16-bit instruction word into the AD9549, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9549 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation (I15 = 0b), the second part is the transfer of data into the serial control port buffer of the AD9549. The length of the transfer (1, 2, 3 bytes, or streaming mode) is indicated by 2 bits (W1:W0) in the instruction byte. The length of the transfer indicated by (W1:W0) does not include the two-byte instruction. CSB can be raised after each sequence of 8 bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when CSB is lowered. Stalling on non-byte boundaries resets the serial control port.

There are three types of registers on the AD9549: buffered, live, and read-only. Buffered (also referred to as mirrored) registers require an IO_UPDATE to transfer the new values from a temporary buffer on the chip to the actual register, and are marked with an "M" in the column labeled "Type" of the register map. Toggling the IO_UPDATE pin or writing a "1" to the Register Update bit (R05h<0>) will cause the update to occur. Since any number of bytes of data can be changed before issuing an update command, the update simultaneously enables all register changes since any previous update. Live registers do not require IO_UPDATE and update immediately after being written. Read-only registers ignore write commands, and are marked "RO" in the "Type" column of the register map. The "Type" column of the register map may also have an "AC," which indicates that the register is auto-clearing.

Read

If the instruction word is for a read operation (I15 = 1b), the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1,2,3,4 as determined by W1:W0. In this case, 4 is used for streaming mode where 4 or more words are transferred per read. The data read back is valid on the falling edge of SCLK.

The default mode of the AD9549 serial control port is bidirectional mode, and the data read back appears on the SDIO pin. It is possible to set the AD9549 to unidirectional mode by writing the SDO enable register at 00h<7> = 0b, and in that mode, the requested data appears on the SDO pin.

By default, a read request reads the register value that is currently in use by the AD9549. However, setting R04h<0>=1 will cause the "buffered" registers to be read instead. The buffered registers are the ones that will take effect during the next IO_UPDATE.

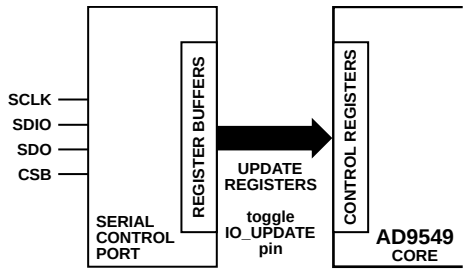


Figure 38: Relationship Between Serial Control Port Register Buffers and Control Registers of the AD9549

The AD9549 uses Addresses 00h to 509h. Although the AD9549 serial control port allows both 8-bit and 16-bit instructions, the 8-bit instruction mode provides access to five address bits (A4 to A0) only, which restricts its use to the address space 00h to 01F. The AD9549 defaults to 16-bit instruction mode on power-up, and the 8-bit instruction mode is not supported.

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1:W0, indicate the length of the transfer in bytes. The final 13 bits are the address (A12:A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits W1:W0, which is interpreted according to Table 6.

A12:A0: These 13 bits select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. The AD9549 uses all of the 13-bit address space. For multi-byte transfers, this address is the starting byte address.

W1	W0	Bytes to Transfer (excluding the two-byte instruction)
0	0	1
0	1	2
1	0	3
1	1	Streaming Mode

Table 6: Byte Transfer Count

MSB/LSB FIRST TRANSFERS

The AD9549 instruction word and byte data may be MSB first or LSB first. The default for the AD9549 is MSB first. The LSB first mode may be set by writing 1b to Register 00h<6>, and requires that an I/O Update be executed. Immediately after the LSB, first bit is set, all serial control port operations are changed to LSB first order.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multi-byte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from high address to low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multi-byte transfer cycle.

When LSB_First = 1b (LSB first), the instruction and data bytes must be written from LSB to MSB. Multi-byte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial control port internal byte address generator increments for each byte of the multi-byte transfer cycle.

The AD9549 serial control port register address decrements from the register address just written toward 0000h for multi-byte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the serial control port register address increments from the address just written toward 1FFFh for multi-byte I/O operations.

Unused addresses are not skipped during multi-byte I/O operations. The user should write the default value to a reserved register, and should only write zeros to unmapped registers. Note: It is more efficient to issue a new write command than writing the default value to more than two consecutive reserved (or unmapped) registers.

MSB															**LSB**
I15	**I14**	**I13**	**I12**	**I11**	**I10**	**I9**	**I8**	**I7**	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 7: Serial Control Port, 16-Bit Instruction Word, MSB First

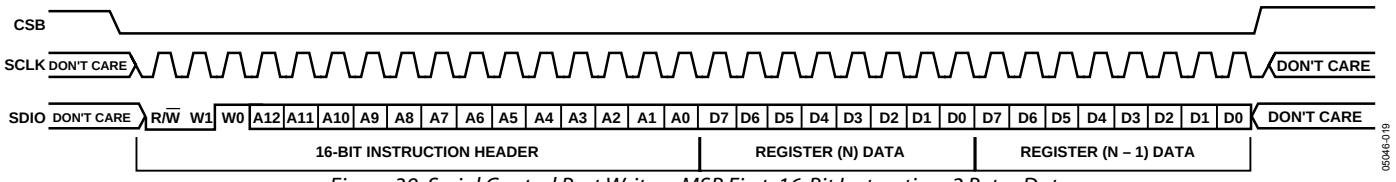


Figure 39: Serial Control Port Write—MSB First, 16-Bit Instruction, 2 Bytes Data

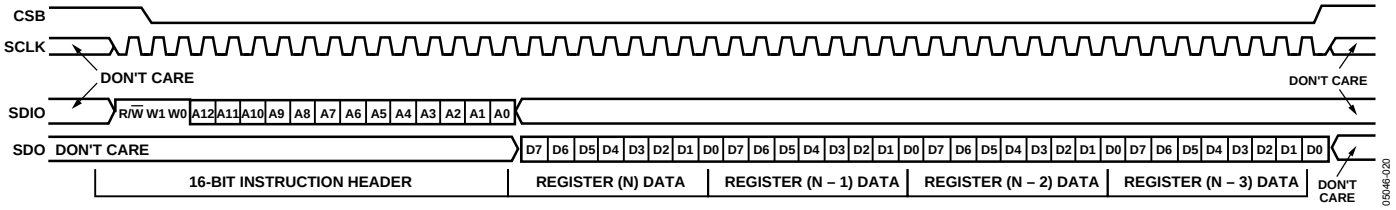


Figure 40: Serial Control Port Read—MSB First, 16-Bit Instruction, 4 Bytes Data

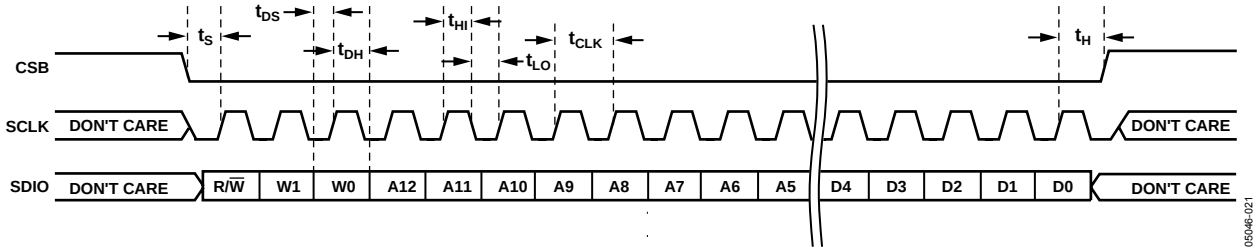


Figure 41: Serial Control Port Write: MSB First, 16-Bit Instruction, Timing Measurements

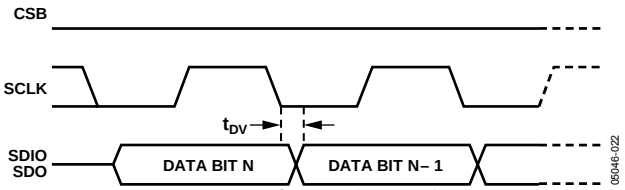


Figure 42: Timing Diagram for Serial Control Port Register Read

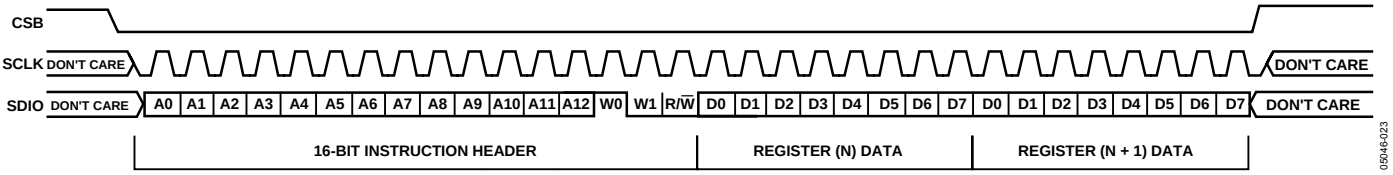


Figure 43: Serial Control Port Write—LSB First, 16-Bit Instruction, 2 Bytes Data

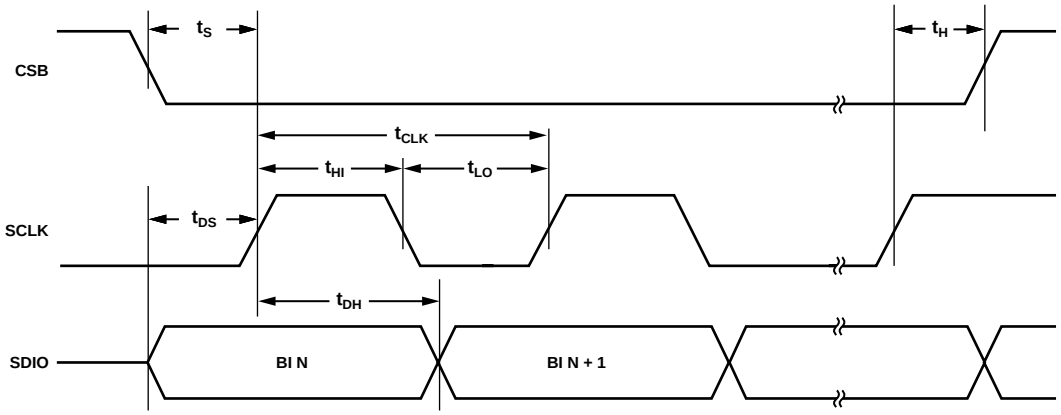


Figure 44: Serial Control Port Timing—Write

Parameter	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

Table 8: Definitions of Terms Used Serial Control Port Timing Diagrams

I/O REGISTER MAP

Table 9

Addr (hex)	Type	Name (short description)	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)
0000	Serial Port Configuration and Part Identification										
0000		Serial Config	SDO Active	LSB First (buffered)	Soft RST	Long Inst.					18
0001		Reserved									00
0002	RO	Part ID	Part ID								02
0003	RO										09
0004		Serial Options								Read Buffer Reg	00
0005	AC									Register Update	00
0010	Power Down and Reset										
0010		Power Down / Enable	PD HSTL Driver	Enable CMOS Driver	Enable Output Doubler	PD SysClk PLL	PD RefA	PD RefB	Full PD	Digital PD	00
0011		Reserved									00
0012	M, AC	Reset	History Reset		IRQ Reset	FPFD Reset	CPFD Reset	LF Reset	CCI Reset	DDS Reset	00
0013	M		PD Fund DDS				S Div2 Reset	R Div2 Reset	S Div Reset	R Div Reset	00
0020	System Clock										
0020		N-Divider				N Divider [4:0]					12
0021		Reserved									00
0022		PLL Parameters	VCO Auto Range				2x Refer-ence	VCO Range	Charge Pump Current [1:0]		04
0023		PFD Divider					PFD Divider [3:0] (relationship between SysClk and PFD clock)				05
0100	DPLL										
0100	M	PLL Control			Single Tone Mode	Disable Freq. Estimator	Enable Freq Slew Limiter		Loop Polarity	Close Loop	30
0101		R-Divider	R Divider [15:0]								00
0102											00
0103			Falling Edge Triggered							R Divider /2	00

0104		S-Divider	S Divider [15:0]												00
0105															00
0106			Falling Edge Triggered											S Divider /2	00
0107	M	P-Divider				P Divider[4:0]									05
0108	M	Loop Coefficients	Alpha-0 [7:0]												00
0109	M						Alpha-0 [11:8]								00
010A	M					Alpha-1 [4:0]									00
010B	M							Alpha-2 [2:0]							00
010C	M		Beta-0 [7:0]												00
010D	M						Beta-0 [11:8]								00
010E	M							Beta-1 [2:0]							00
010F	M		Gamma-0 [7:0]												00
0110	M						Gamma-0 [11:8]								00
0111	M							Gamma-1 [2:0]							00
0112															00
0113															00
0114															00
0115	RO	FTW Estimate	FTW Estimate [47:0] (read-only)												N/A
0116	RO														N/A
0117	RO														N/A
0118	RO														N/A
0119	RO														N/A
011A	RO														N/A

011B	M	FTW Limits	FTW Lower Limit [47:0]	00
011C	M			00
011D	M			00
011E	M			00
011F	M			00
0120	M			00
0121	M		FTW Upper Limit [47:0]	FF
0122	M			FF
0123	M			FF
0124	M			FF
0125	M			FF
0126	M			7F
0127	M	Slew Limit	Frequency Slew Limit [47:0]	00
0128	M			00
0129	M			00
012A	M			00
012B	M			00
012C	M			00
012D		Reserved		00
012E				00
012F				00
0130				00

01A0		Free-Run Mode								
01A0		Reserved								00
01A1										00
01A2										00
01A3										00
01A4										00
01A5										00
01A6	M	FTW0 (Open Loop Frequency Tuning Word)	FTW0 [47:0]							00
01A7	M									00
01A8	M									00
01A9	M									00
01AA	M									start-up cond.
01AB	M									start-up cond.
01AC-01AD	M	Phase (Open Loop Only)	DDS Phase Word [15:0]							00
01C0		Reference Selector / Holdover								
01C0	M	Automatic Control				Holdover Mode		Automatic Selector	Automatic Recover	Automatic Holdover	00
01C1	M	Override				Enable Line-Card Mode	Enable Ref Input Override	Ref_AB	Enable Holdover Override	Holdover On/Off	00
01C2		Averaging Window					FTW Windowed Average Size [3:0]				00
01C3		Reference Validation				Validation Timer [4:0]					00
0200		Doubler and Output Drivers								
0200		HSTL Driver				OPOL (polarity)			HSTL Output Doubler		05
0201		CMOS Driver								CMOS MUX	00

0300		Monitor									
0300	RO	Status		PFD Freq too High	PFD Freq too Low	Freq. Est. Done	Ref Selected	Free Run	Ph. Lock Detected	Freq. Lock Detected	N/A
0301	RO			RefA Valid	RefA LOR	RefA OOL		RefB Valid	RefB LOR	RefB OOL	N/A
0302	RO	IRQ Status		PFD Freq too High	PFD Freq too Low	Freq. Est. Done	Ref Selected	Free Run	Ph. Lock Detected	Freq. Lock Detected	00
0303	RO			RefA Valid	RefA LOR	RefA OOL		RefB Valid	RefB LOR	RefB OOL	00
0304		IRQ Mask						Ref. Changed	Leave Free Run	Enter Free Run	00
0305						Freq Est Done	Phase Unlock	Phase Lock	Freq. Unlock	Freq. Lock	00
0306					RefA Valid	!RefA Valid	RefA LOR	!RefA LOR	RefA OOL	!RefA OOL	00
0307					RefB Valid	!RefB Valid	RefB LOR	!RefB LOR	RefB OOL	!RefB OOL	00
0308		S1 Pin Config	Ref?	Ref? LOR	Ref? OOL	Ref? Not Valid	Phase Lock	Freq. Lock		IRQ	60
0309		S2 Pin Config	Ref?	Ref? LOR	Ref? OOL	Ref? Not Valid	Phase Lock	Freq. Lock		IRQ	E0
030A		S3 Pin Config	Ref?	Ref? LOR	Ref? OOL	Ref? Not Valid	Phase Lock	Freq. Lock		IRQ	08
030B		S4 Pin Config	Ref?	Ref? LOR	Ref? OOL	Ref? Not Valid	Phase Lock	Freq. Lock		IRQ	01
030C		Control	Enable RefA LOR	Enable RefA OOL	Enable RefB LOR	Enable RefB OOL			Enable Phase Lock Det.	Enable Freq. Lock Detector	A2
030E	RO	HFTW	Average or Instantaneous FTW [47:0] (read-only) (An IO_UPDATE is required to refresh these registers.)								N/A
030F	RO										N/A
0310	RO										N/A
0311	RO										N/A
0312	RO										N/A
0313	RO										N/A
0314	M	Phase Lock	Phase Lock Threshold [31:0]								FF
0315	M										00
0316	M										00
0317	M										00

0318	M		Phase Unlock Watchdog Timer [2:0]	Phase Lock Watchdog Timer [4:0]	FF
0319	M	Frequency Lock	Frequency Lock Threshold [31:0]		00
031A	M				00
031B	M				00
031C	M				00
031D	M		Frequency Unlock Watchdog Timer [2:0]	Frequency Lock Watchdog Timer [4:0]	FF
031E	M	Loss of Reference	RefA LOR Divider [15:0]		FF
031F	M				FF
0320	M		RefB LOR Divider [15:0]		FF
0321	M				FF
0322	M	Reference Out Of Limits	RefA OOL Divider [15:0]		00
0323	M				00
0324	M		RefA OOL Upper Limit [31:0]		FF
0325	M				FF
0326	M				FF
0327	M				FF
0328	M		RefA OOL Lower Limit [31:0]		00
0329	M				00
032A	M				00
032B	M				00
032C	M		RefB OOL Divider [15:0]		00
032D	M				00
032E	M		RefB OOL Upper Limit [31:0]		FF
032F	M				FF
0330	M				FF

0331	M			FF
0332	M		RefB OOL Lower Limit [31:0]	00
0333	M			00
0334	M			00
0335	M			00
0400		Calibration (User Accessible Trim)		
0400		K Divider	K Divider [15:0]	00
0401				00
0402	M	CPFD Gain	CPFD Gain Scale [2:0]	00
0403	M		CPFD Gain [5:0]	20
0404		FPFD Gain	FPFD Gain [7:0]	C8
0405		Reserved		00
0406				00
0407				00
0408				00
0409	M	PFD Offset	DPLL Phase Offset [7:0]	00
040A	M		DPLL Phase Offset [13:8]	00
040B		DAC FS Current	DAC Full-scale Current [7:0]	FF
040C			DAC Full-scale Current [9:8]	01
040D		Reserved		00
040E		Reserved		10
040F		Ref Bias Level	DC Input Level [1:0]	00
0410		Reserved		00

0500		Harmonic Spur Reduction									
0500	M	Spur A	HSR-A Enable	Gain			Spur A Harmonic [3:0]				00
0501	M		Spur A Magnitude [7:0]								00
0502	M										00
0503	M		Spur A Phase [7:0]								00
0504	M									Spur A Phase [8]	00
0505	M	Spur B	HSR-B Enable	Gain			Spur B Harmonic [3:0]				00
0506	M		Spur B Magnitude [7:0]								00
0507	M										00
0508	M		Spur B Phase [7:0]								00
0509	M									Spur B Phase [8]	00

Types of Registers:

M: Mirrored (also called Buffered). This type of register needs an IO_UPDATE for the new value to take effect.)

RO: Read-Only

AC: Auto-clear

I/O REGISTER DESCRIPTION

Serial Port Configuration (0000 – 0005)

0000; Serial Configuration; bits D4 – D7 are mirror image of D0 – D3

[0] SDO Active: Enables SDO pin 1=SDO pin enabled (four-wire serial port mode.) 0= three-wire mode.

[1] LSB First: Sets bit order for serial port. 1=LSB first. 0=MSB first. IO_UPDATE must occur in order to take effect.

[2] Soft Reset: Resets register map except for register 0000. Setting this bit forces a soft reset, meaning that S1-S4 are not tri-stated, nor is their state read when this bit is cleared. The 9549 will assume the values of S1-S4 that were present during the last hard reset. This bit is not self-clearing, and all other registers will be restored to their default values after a soft reset.

[3] Long Instruction: Read-only: this part only supports long instructions.

0001; Reserved

0002 - 0003; Part ID (read-only)

0004; Serial Options

[0] Read Buffer Register: For buffered registers, serial port read-back reads from actual (active) registers instead of the buffer.
1= Reads the buffered values that will take effect during the next IO_UPDATE.
0= Reads values that are currently in effect.

0005; Serial Options; Self Clearing

[0] Register Update: Software access to the "Register Update" pin function.
Writing a "1" to this bit is identical to performing an IO_UPDATE.

Power Down and Reset

0010; Power Down and Enables; Power up default is defined by start-up pins.

[0] Digital PD; Remove clock from most of digital section; leave serial port usable.
In contrast to Full PD, setting this bit does not de-bias inputs, allowing for quick wake-up.

[1] Full PD; Setting this bit is identical to activating the PD pin, and puts all blocks (except serial port) into power down mode. Sysclk is turned off.

[2] PD RefB; Power down reference clock B input (and related circuits)

[3] PD RefA; Power down reference clock A input (and related circuits)

[4] PD System Clock PLL: System clock multiplier is powered down. 1= System Clock Multiplier powered down.

[5] Enable Output Doubler; Power up output clock generator doubler. Output Doubler must still be enabled in Register 0200.

[6] Enable CMOS Driver: Power up CMOS output driver. 1= CMOS Driver on.

[7] PD HSTL Driver: Power down HSTL output driver. 1 = HSTL Driver powered down.

0011; Reserved

0012; Reset; Auto Clear;

To reset the entire chip, the user may also use the (non-self clearing) Soft Reset bit in Register 0000.
Except for IRQ reset, the user normally would not need to use these. However, if the user attempts to lock the loop for the first time when no signal is present, the user should write a 1 to bits 0-4 of this register prior to attempting to lock the loop again.

[0] DDS (Direct Digital Synthesis) Reset

[1] CCI (Cascaded Comb Integrator) Reset

[2] LF (Loop Filter) Reset

[3] CPFD (Coarse Phase Frequency Detector) Reset

[4] FPFD (Fine Phase Frequency Detector) Reset

[5] IRQ Reset: Clear IRQ signal and IRQ status monitor

[6] Unused

[7] History Reset: Setting this bit clears the FTW monitor and pipeline.

0013; Reset (continued); NOT Auto Clear.

[0] R Divider Reset: Synchronous (to R divider prescaler output) reset for integer divider

[1] S Divider Reset: Synchronous (to S divider prescaler output) reset for integer divider

[2] R Div2 Reset: Asynchronous reset for R prescaler

[3] S Div2 Reset: Asynchronous reset for S prescalar

[7] PD Fund DDS: Setting this bit powers down the DDS fundamental output, but not the spurs. It is used during tuning of the Spur Killer circuit.

System Clock

0020; N Divider

[4:0] N Divider: These bits set the Feedback divider for System Clock PLL. There is a fixed /2 preceding this block, as well as a an offset of 2 added to this value. Therefore, setting this register to 00000 translates to an overall feedback divider ratio of 4. See Figure 29: Block Diagram of the SysClk PLL on Page 37.

0021; Reserved

0022; PLL Parameters

[1:0] Charge Pump Current: 00: 250 uA , 01: 375 uA, 10: Off, 11: 125 uA

[2] VCO Range: Select low range or high range VCO. 0= low range (700 to 800 MHz). 1= high range (850 to 1000 MHz). For System clock settings in between 800-850 MHz, use the VCO Auto Range (Bit 7) to set the correct VCO range automatically.

[3] 2x Reference: Enables a frequency doubler prior to the Sysclk PLL and can be useful in reducing jitter induced by the Sysclk PLL. See Figure 28: System Clock Generator Block Diagram, Page 37.

[4:6] Reserved

[7] VCO Auto Range: Automatic VCO range selection. Enabling this bit allows Bit 2 of this register to be set automatically.

0023; PFD Divider

[3:0] Divide ratio for PFD clock from system clock. This is typically varied only in cases where the designer wishes to run the DPLL Phase detector fast while Sysclk is run relatively slowly. The ratio is equal to PFD Divider * 4. For a 1 GHz system clock, the ADC runs at 1 GHz / 20 = 50 MHz, and the DPLL phase detector runs at half this speed , which in this case is 25 MHz).

Digital PLL Control and Dividers

0100; PLL Control

[0] Close Loop: Setting this bit closes the loop. If Bit 4 of this register is cleared, then the frequency estimator will be used. If this bit is cleared and the loop is opened, the user should reset the CCI and LF bits of Register 0012 prior to closing the loop again.

[1] Loop Polarity: This bit reverses the polarity of the loop response.

[2] Unused

[3] Enable Frequency Slew Limiter: This bit enables the frequency slew limiter that controls how fast the tuning word can change, and is useful for avoiding runt and stretched pulses during clock switchover and holdover transitions. These values are set in Registers 0127-012C. See “Frequency Slew Limiter” on Page 40.

[4] Disable Frequency Estimator. The Frequency Estimator is normally not used, but is useful when the input frequency is unknown, or needs to be qualified. This estimate appears in Registers 115-11A. The Frequency Estimator is not needed when FTW0 (Register 01A6-01AB) is programmed. See “Frequency Estimator“ on Page 41.

[5] Single Tone Mode: Setting this bit allows the 9549 to output a tone open loop using FTW0 as DDS tuning word. This bit must be cleared when Bit 0 (Close Loop) is set. This is very useful in debugging when the signal coming into the AD9549 is questionable or nonexistent.

[7:6] Reserved

0101 – 0102; R Divider (DPLL Feedforward Divider)

[15:0] Feedforward Divider (also called the Reference divider) of the DPLL. Divide Ratio: 1 – 65536. See “Feedforward Divider (Divide-by-R)” on Page 20. If the desired feedfeedforward ratio is greater than 65536, or if the reference input signal on REF_A or REF_B is greater than 400 MHz, then Bit 0, R103 must be set.

0103; R Divider (continued)

[0] Divide by 2: Setting this bit enables an additional /2 pre-scalar, effectively doubling the range of the Feedforward Divider. If the desired feedfeedforward ratio is greater than 65536, or if the reference input signal on REF_A or REF_B is greater than 400 MHz, then this bit must be set.

[6:1] Unused

[7] Falling Edge Triggered: Setting this bit inverts the reference clock before R divider.

0104 – 0105; S Divider (DPLL Feedback Divider)

[15:0] Feedback Divider: Divide Ratio: 1 – 65536. If the desired feedback ratio is greater than 65536, or if the feedback signal on FDBK_IN is greater than 400 MHz, then Bit 0, R106 must be set.

0106; S Divider (continued)

[0] Divide by 2: Setting this bit enables an additional /2 pre-scalar. See "Feedback Divider (Divide-by-S)" on Page 20. If the desired feedback ratio is greater than 65536, or if the feedback signal on FDBK_IN is greater than 400 MHz, then this bit must be set. An example of this case is when the PLL is locking to an image of the DAC output that is above the Nyquist frequency.

[6:1] Unused

[7] Falling Edge Triggered: Setting this bit inverts the reference clock before the S divider.

Digital PLL Loop Filter

0107; P Divider

[4:0] Divide Ratio: Controls the ratio of DAC sample rate to loop filter sample rate. See "Digital Loop Filter" on Page 21. Loop filter sample rate = DAC Sample rate / 2^(Divide Ratio[4:0]). For the default case of 1 GHz DAC sample rate, and P Divider [4:0] of 5, the loop filter sample rate is 31.25 MHz. Note: The DAC sample rate is the same as System Clock.

0108 – 0109; Loop Coefficients (See "Digital Loop Filter Coefficients" on Page 25.)

(Note : The AD9549 evaluation software will derive these values.)

[11:0] Alpha-0: Linear coefficient for "alpha" coefficient

010A; Loop Coefficients (continued)

[4:0] Alpha-1: Power of 2 multiplier for "alpha" coefficient

010B; Loop Coefficients (continued)

[3:0] Alpha-2: Power of 2 divider for "alpha" coefficient

010C – 010D; Loop Coefficients (continued)

[11:0] Beta-0: Linear coefficient for "beta" coefficient

010E; Loop Coefficients (continued)

[2:0] Beta-1: Power of 2 divider for "beta" coefficient

010F – 0110; Loop Coefficients (continued)

[11:0] Gamma-0: Linear coefficient for "gamma" coefficient

0111; Loop Coefficients (continued)

[2:0] Gamma -1: Power of 2 divider for "gamma" coefficient

0112 – 0114; Reserved

0115 – 011A; FTW Estimate (Read-Only)

[47:0] FTW Estimate: This is frequency estimate from frequency estimator circuit, and is informational only. It's useful for verifying the input reference frequency. See "Frequency Estimator" on Page 41 for a description.

011B – 0120; FTW Lower Limit

[47:0] FTW Lower Limit: Lowest DDS tuning word in closed loop mode. This feature is recommended when a bandpass reconstruction filter is used. See "Output Frequency Range Control" on Page 34.

0121 – 0126; FTW Upper Limit

[47:0] FTW Upper Limit: Highest DDS tuning word in closed loop mode. This feature is recommended when a bandpass reconstruction filter is used. See "Output Frequency Range Control" on Page 34.

0127 – 012C; Frequency Slew Limit

[47:0] Frequency Slew Limit: See "Frequency Slew Limiter" on Page 40.

012D – 0130; Reserved

Free-Run (Single-Tone) Mode

01A0 – 01A5; Reserved

01A6 – 01AB; FTW0

[47:0] FTW0: FTW (Frequency Tuning Word) for DDS when loop is not "closed" (see register 0100 bit 0)
Also used as the initial frequency estimate when the estimator is disabled (see register 0100 bit 4)
Note: The power up default is defined by startup pins S1-S4. See "Default DDS Output Frequency on Power-Up" on Page 43.

01AC – 01AD; Phase

[15:0] DDS Phase Word: Allows user to vary the phase of the DDS output. Active only when loop is not "closed."

Reference Selector / Holdover

01C0; Automatic Control

[0] Automatic Holdover: Setting this bit permits state-machine to enter holdover (free-run) mode.

[1] Automatic Recover: Setting this bit permits state-machine to leave holdover mode.

[2] Automatic Selector: Setting this bit permits state-machine to switch the active reference clock input.

[3] Reserved

[4] Holdover Mode: This bit determines which Frequency Tuning Word (FTW) is used in Holdover Mode.
0: Use last FTW at time of holdover. 1: Use averaged FTW at time of holdover, which is the recommended setting. The number of averages used is set in Register 01C2.

01C1; Override

[0] Holdover On/Off: This bit controls the status of holdover when Bit 1 of this register is set.

[1] Enable Holdover Override: Setting this bit disables automatic holdover, and allows user to enter/exit holdover manually via Bit 0 (see above). Setting this bit overrides the HOLDOVER pin.

[2] Ref_AB: This bit selects the input when Bit 3 of this register is set. 0 equals REF_A.

[3] Enable Ref Input Override: Setting this bit disables automatic reference switchover, and allows user to switch references manually via Bit 2 of this register. Setting this bit overrides the REFSELECT pin.

[4] Enable Line-Card Mode: Enables line-card mode of reference switch MUX, which eliminates the possibility of a runt pulse during switchover. See "Use of Line Card Mode to Eliminate Runt Pulses" on Page 31.

01C2; Averaging Window

[3:0] FTW Windowed Average Size: This register sets the number of FTWs (frequency tuning words) that are used for calculating the average FTW. Bit 4 in Register 01C0 enables this feature. An average size of at least 32000 is recommended for most applications. The number of averages equals $2^{(\text{FTW Windowed Average Size [3:0]})}$. These samples are taken at the rate of (fs / 2^P_{IO}).

01C3; Reference Validation

[4:0] Validation Timer: The value in this register sets the time required to validate a reference after a LOR or OOL event before the reference can be used as the DPLL reference. This circuit uses the digital loop filter clock (see Register 0107). Validation time = Loop filter clock period * $2^{(\text{Validation Timer[4:0] +1})}$ -1. Assuming power-on defaults, the recovery time varies from 32 ns (00000) to 137 sec (11111). If longer validation times are required, the user can make the P divider larger. The user should be careful to set the validation timer to at least two periods of the OOL Evaluation Period. The OOL Evaluation Period is is the period of reference input clock times the OOL Divider (R0322-0323).

[6:5] Unused

Doubler and Output Drivers

0200; HSTL Driver

[2:0] HSTL Output Doubler: 01: Doubler disabled. 00: Doubler enabled.

[3:2] Unused

[4] OPOL: Output polarity: Setting this bit inverts the HSTL driver output polarity.

0201; CMOS Driver

[0] User MUX control: This bit allows the user to select whether the CMOS driver output is divided by the S Divider. 0: S divider input sent to CMOS driver. 1: S divider output sent to CMOS driver.
See Figure 8: Detailed Block Diagram on Page 19.

Monitor

0300; Status: This register contains the status of the chip. This register is read-only and live update.

[0] Frequency Lock Detect: This flag indicates that the "Frequency Lock Detect" circuit has detected frequency lock. This feature compares the absolute value of the difference of two consecutive phase detector edges against a programmable threshold. Because of this, frequency lock detect is more rigorous than phase lock detect, and it is possible to have phase lock detect without frequency lock detect.

[1] Phase Lock Detect: This flag indicates that the "Phase Lock Detect" circuit has detected phase lock. The amount of phase adjustment is compared against a programmable threshold. Note: this bit may be set in single tone and holdover modes, and should be ignored in these cases.

[2] Free Run: DPLL is in holdover mode (free-run)

[3] Reference Selected: 0: Reference A is active. 1: Reference B is active.

[4] Frequency Estimator Done: True when the "Frequency Estimator" circuit has successfully estimated the input frequency. See "Frequency Estimator" on Page 41.

[5] PFD Frequency too Low: This flag indicates that the Frequency Estimator failed and detected too low of a PFD frequency. This bit is only relevant if the user is relying on the Frequency Estimator to determine the input frequency.

[6] PFD Frequency too High: This flag indicates that the Frequency Estimator failed and detected too high of a PFD frequency. This bit is only relevant if the user is relying on the Frequency Estimator to determine the input frequency.

[7] Unused

0301; Status (continued): This register contains the status of the chip. This register is read-only and live update.

[0] RefB OOL: The "OOL" (Out of Limits) circuit has determined that Reference B is out of limits.

[1] RefB LOR: A "LOR" (Loss of Reference) has occurred on Reference B.

[2] RefB Valid: The Reference Validation circuit has successfully determined that Reference B is valid.

[3] Unused

[4] RefA OOL: The "OOL" (Out of Limits) circuit has determined that Reference A is out of limits.

[5] RefA LOR: A "LOR" (Loss of Reference) has occurred on Reference A.

[6] RefA Valid: The Reference Validation circuit has successfully determined that Reference A is valid.

[7] Unused

0302 – 0303; IRQ Status; These registers contain the chip status (Registers 0300 – 0301) at the time of IRQ.

These bits are cleared with an IRQ reset (see Register 0012, Bit 5).

0304; IRQ Mask

[0] Enter Free Run: Trigger IRQ when DPLL enters free-running (holdover) mode.

[1] Leave Free Run: Trigger IRQ when DPLL leaves free-running (holdover) mode

[2] Reference Changed: Trigger IRQ when active reference clock selection changes

[7:3] Unused

0305; IRQ Mask (continued)

[0] Frequency Lock: Trigger IRQ on rising edge of "Frequency Lock" signal

[1] Frequency Unlock: Trigger IRQ on falling edge of "Frequency Lock" signal

[2] Phase Lock: Trigger IRQ on rising edge of "Phase Lock" signal

[3] Phase Unlock: Trigger IRQ on falling edge of "Phase Lock" signal

[4] Frequency Estimator Done: Trigger IRQ when the "Frequency Estimator" is done

0306; IRQ Mask (continued)

[0] !RefA OOL: Trigger IRQ on falling edge of reference A's OOL

[1] RefA OOL: Trigger IRQ on rising edge of reference A's OOL

[2] !RefA LOR: Trigger IRQ on falling edge of reference A's LOR

[3] RefA LOR: Trigger IRQ on rising edge of reference A's LOR

[4] !RefA Valid: Trigger IRQ on falling edge of reference A's "Valid"

[5] RefA Valid: Trigger IRQ on rising edge of reference A's "Valid"

[7:6] Unused

0307; IRQ Mask (continued)

[0] !RefB OOL: Trigger IRQ on falling edge of reference B's OOL

[1] RefB OOL: Trigger IRQ on rising edge of reference B's OOL

[2] !RefB LOR: Trigger IRQ on falling edge of reference B's LOR

[3] RefB LOR: Trigger IRQ on rising edge of reference B's LOR

[4] !RefB Valid: Trigger IRQ on falling edge of reference B's "Valid"

[5] RefB Valid: Trigger IRQ on rising edge of reference B's "Valid"

[7:6] Unused

0308; S1 Pin Configuration (See “Status and Warnings” on Page 42.)

Note: The choice of input for a given pin must be all Ref A or all Ref B, and not a combination thereof.

[0] IRQ: Select “IRQ” signal for output on this pin

[1] Reserved

[2] Frequency Lock: Select “Frequency Lock” signal for output on this pin

[3] Phase Lock: Select “Phase Lock” signal for output on this pin

[4] Ref? Not Valid: Select either RefA (0) or RefB (1) “Not Valid” signal for output on this pin

[5] Ref? OOL: Select either RefA (0) or RefB (1) “OOL” signal for output on this pin

[6] Ref?: LOR: Select either RefA (0) or RefB (1) “LOR” signal for output on this pin

[7] Ref?: Choose either RefA (0) or RefB (1) for use with bits 4 – 6

0309; S2 Pin Configuration: Same as register 0308, except applies to pin S2

030A; S3 Pin Configuration: Same as register 0308, except applies to pin S3

030B; S4 Pin Configuration: Same as register 0308, except applies to pin S4

030C; Control

[0] Enable Frequency Lock Detector. Register 0319 must be set up to use this. See “Frequency Lock Detection” on Page 28.

[1] Enable Phase Lock Detector: Register 0314h-0318h must be set up to use this. See “Phase Lock Detection” on Page 27.

[3:2] Unused

[4] Enable RefB OOL: The RefB OOL limits are set up in Registers 032C to 0335.

[5] Enable RefB LOR: The RefA LOR limits are set up in Registers 0320 to 0321.

[6] Enable RefA OOL: The RefB OOL limits are set up in Registers 0322 to 032B.

[7] Enable RefA LOR: The RefB LOR limits are set up in Registers 031E to 031F.

030D; Unused

030E – 0313; HFTW; Read-Only

[47:0] Average or Instantaneous FTW: This read-only register is the output of FTW monitor. Average or Instantaneous is determined by “Holdover Mode” (see Bit 4, Register 01C0). These registers must be manually refreshed by issuing an IO_UPDATE.

0314 – 0317; Phase Lock

[31:0] Phase Lock Threshold: See “Phase Lock Detection” on Page 27.

0318; Phase Lock (continued)

[7:5] Phase Unlock Watchdog Timer : See “Phase Lock Detection” on Page 27.

[4:0] Phase Lock Watchdog Timer : See “Phase Lock Detection” on Page 27.

0319 – 031C; Frequency Lock

[31:0] Frequency Lock Threshold: See "Frequency Lock Detection" on Page 28.

031D; Frequency Lock (continued)

[7:5] Frequency Unlock Watchdog Timer: See "Frequency Lock Detection" on Page 28.

[4:0] Frequency Lock Watchdog Timer: See "Frequency Lock Detection" on Page 28.

031E – 031F; Loss of Reference

[15:0] RefA LOR Divider: See "Loss of Reference" on Page 29.

0320 – 0321; Loss of Reference (continued)

[15:0] RefB LOR Divider: See "Loss of Reference" on Page 29.

0322 – 0323; Reference Out Of Limits (OOL)

[15:0] RefA OOL Divider: See "Reference Frequency Monitor" on Page 29. R0322 is the LSB, and R0323 is the MSB.

0324 – 0327; Reference OOL (continued)

[31:0] RefA OOL Upper Limit: See "Reference Frequency Monitor" on Page 29.

0328 – 032B; Reference OOL (continued)

[31:0] RefA OOL Lower Limit: See "Reference Frequency Monitor" on Page 29.

032C – 032D; Reference OOL (continued)

[15:0] RefB OOL Divider: See "Reference Frequency Monitor" on Page 29. R032C is the LSB, and R032D is the MSB.

032E – 0331; Reference OOL (continued)

[31:0] RefB OOL Upper Limit: See "Reference Frequency Monitor" on Page 29.

0332 – 0335; Reference OOL (continued)

[31:0] RefB OOL Lower Limit: See "Reference Frequency Monitor" on Page 29.

Calibration (User Accessible Trim)

0400 – 0401; K Divider

[15:0] K Divider: The K divider alters precision of frequency estimator circuit. See "Frequency Estimator" on Page 41.

0402; CPFD Gain

[2:0] CPFD Gain Scale: This register is the coarse phase frequency power of 2 multiplier (PDS). See "Phase Detector" on Page 24. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

0403; CPFD Gain (continued)

[5:0] CPFD Gain: This register is the coarse phase frequency linear multiplier (PDG). See "Phase Detector" on Page 24. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

0404; FPFD Gain

[7:0] FPFD Gain: This register is the fine phase frequency detector linear multiplier (alters charge-pump current). See "Fine Phase Detector" on Page 24. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

0405 – 0408; Unused

0409 – 040A; PFD Offset

[13:0] DPLL Phase Offset: This register controls the static time offset of the PFD (Phase Frequency Detector) in closed-loop mode. It has no effect when the DPLL is open.

040B; DAC Full-scale Current:

[7:0] DAC Full-scale Current: DAC Full-scale Current [7:0]. See "DAC Output" on Page 23.

040C; DAC Full-scale Current

[1:0] DAC Full-scale Current: DAC Full-scale Current [9:8]. See Register 040B.

040D – 040E; Unused

040F; Reference Bias Level

[1:0] DC Input Level for VDDX @ 3.3 V: This register sets the DC bias level for the reference inputs. The value should be chosen such that VIH is as close as possible to (but not exceeding) 3.3V.
00: VDD3 – 800 mV
01: VDD3 – 400 mV
10: VDD3 – 1.6 V
11: VDD3 – 1.2 V

[7:2] Reserved

0410; Unused

Harmonic Spur Reduction

0500; Spur A: See "Harmonic Spur Reduction" on Page 70.

[3:0] Spur A Harmonic 1 – 15

[5:4] Unused

[6] Amplitude Gain x2

[7] Harmonic Spur Reduction A Enable (HSR-A Enable)

0501 – 0502; Spur A (continued)

[7:0] Spur A Magnitude: Linear multiplier for Spur A magnitude

0503 – 0504; Spur A (continued)

[8:0] Spur A Phase: Linear offset for Spur A phase

0505; Spur B

[3:0] Spur B Harmonic: 1 – 15

[5:4] Unused

[6] Amplitude Gain x2

[7] Harmonic Spur Reduction B Enable (HSR-B Enable)

0506 – 0507; Spur B (continued)

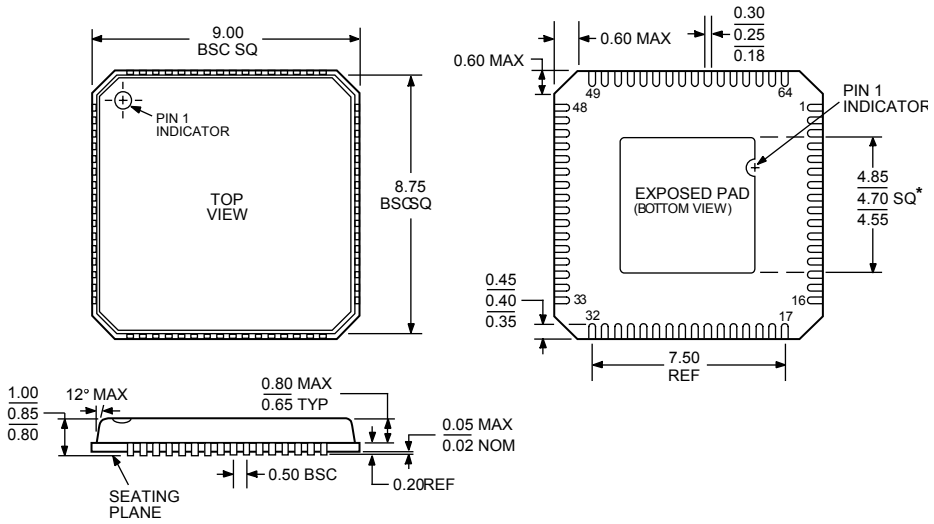
[7:0] Spur B Magnitude: Linear multiplier for Spur B magnitude

0508 – 0509; Spur B (continued)

[8:0] Spur B Phase: Linear offset for Spur B phase

OUTLINE DIMENSIONS

64-Lead Lead Frame Chip Scale Package [LFCSP]
9 x 9 mm Body
(CP-64-1)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 45: Outline Dimensions

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9549BCPZ[1](when released)	-40 to +85	64-lead LFCSP	
AD9549XCPZ[1] (prototypes)	-40 to +85	64-lead LFCSP	

[1] Z = Pb-free part.