Digital MEMS Vibration Sensor w/ Embedded RF Transceiver

ANALOG DEVICES

ADIS16000/ADIS16229

FEATURES

Wireless vibration system, 862MHz – 928MHz
    Clear Channel Assessment/Packet collision avoidance
    Error Detection and Correction in RF protocol
    Programmable RF Output power
Gateway node (ADIS16000)
    SPI to RF function
    Manage up to 6 sensor nodes
Sensor Node (ADIS16229)
    Dual-axis, ±18g MEMS accelerometer
    5.5kHz Resonant frequency
    Digital range settings: 0 g to 1 g/5 g/10 g/20 g
    Sample rate up to 20kSPS
    Programmable wake-up capture, update cycle times
    FFT, 512-point, real valued
    Rectangular, Hanning, flat top window options
    Programmable decimation filter, 11 rate settings
    Multi-record capture for selected filter settings
    Manual capture mode for time domain data collection
    Programmable FFT averaging: up to 255 averages
    Record Storage: 14 FFT records on all three axes (x, y)
    Programmable alarms, 6 spectral bands, 2 levels
    Adjustable response delay to reduce false alarms
    Internal self-test with status flags
    Digital temperature and power supply measurements
    Identification registers: serial number, device ID, user ID
47mm x 38mm PCB package with SMA antenna interface
Single-supply operation: 3.0 V to 3.6 V
Operating temperature range: –40°C to +85°C

APPLICATIONS

Vibration analysis
Condition monitoring
Machine health
Instrumentation, diagnostics
Safety shutoff sensing

GENERAL DESCRIPTION

The ADIS16000 and ADIS16229 enable creation of a simple wireless vibration-sensing network for a wide variety of industrial-equipment applications. . The ADIS16000 provides the gateway function, which manages the network, while the ADIS16229 provides the remote sensing function.

The ADIS16229 iSesnor is a complete wireless vibration sensor node that combines dual-axis acceleration sensing with advanced time domain and frequency domain signal processing. Time domain signal processing includes a programmable decimation filter and selectable windowing function. Frequency domain processing includes a 512-point, real-valued FFT, FFT magnitude averaging, and programmable spectral alarms. The FFT record storage system offers users the ability to track changes over time and capture FFTs with multiple decimation filter settings.

The ADIS16229's dynamic range, bandwidth, sample rate and noise performance are well suited for a wide variety of machine health and production equipment monitoring systems. This devices also provides a number of wireless configuration parameters enable a wide level of flexibility in managing the trade-off between battery life and communication frequency.

The ADIS16000 SPI interface provides simple connectivity with most embedded processor platforms and the SMA connector interface enables the use of many different antennas. This module supports up to six ADIS16229 devices at one time, using a proprietary wireless protocol.

Both ADIS16000 and ADIS16229 modules are in in 47.0x37.6x22.6mm PCB structures, have an SMA connector for simple antenna connection, have two mounting holes for simple installation and support operation over a temperature range of -40°C to +85°C. The ADIS16000 also includes a standard 1mm, 14-pin connector for connecting to an embedded processor system. The ADIS16229 provides a lead structure that enables simple connection with standard batteries.
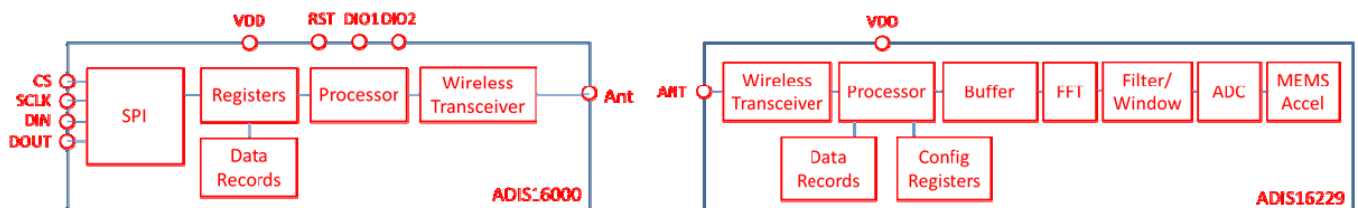
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

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SPECIFICATIONS

T_A = −40°C to +125°C, VDD = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS (ADIS16229)					
Measurement Range[1]	T_A = 25°C	±18			g
Sensitivity, FFT	T_A = 25°C, 0 g to 20 g range setting		0.3052		mg/LSB
Sensitivity, Time Domain	T_A = 25°C		0.6104		mg/LSB
Sensitivity Error	T_A = 25°C		±0.3	±6	%
Nonlinearity	With respect to full scale		±0.2	±1.25	%
Cross-Axis Sensitivity			4		%
Alignment Error	With respect to package mounting holes		2.3		Degrees
Offset Error	T_A = 25°C		±0.01	±1	g
Offset Temperature Coefficient			2		mg/°C
Output Noise	T_A = 25°C, 20.48 kHz sample rate, time domain		11		mg rms
Output Noise Density	T_A = 25°C, 10 Hz to 1 kHz		0.248		mg/√Hz
Bandwidth	±5% flatness,[2] see Figure 19		840		Hz
Sensor Resonant Frequency			5.5		kHz
LOGIC INPUTS[3] (ADIS16000)					
Input High Voltage, V_{INH}		0.7 x VDD			V
Input Low Voltage, V_{INL}				0.2xVDD	V
Input Leakage Current					
All Except $\overline{RST}$			TBD		μA
$\overline{RST}$			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1 mA	VDD-0.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1 mA			0.36	V
FLASH MEMORY					
Endurance[4]		20,000			Cycles
Data Retention[5]	T_J = 85°C, see Figure 23	20			Years
START-UP TIME[6]					
Initial Startup	ADIS16000		200		ms
	ADIS16229		100		ms
Reset Recovery[7]	ADIS16000		200		ms
	ADIS16229		50		ms
Sleep Mode Recovery	ADIS16229		2.3		ms
CONVERSION RATE	REC_CTRL1[11:8] = 0x1 (SR0 sample rate selection)		20		kSPS
Clock Accuracy			3		%
POWER SUPPLY	Operating voltage range, VDD	3.0	3.3	3.6	V
Power Supply Current, ADIS16229	Transmission mode, 10dBm, +25C		39	41	mA
	Transmission mode, 10dBm, -40C to +85C		TBD		
	Transmission mode, -1dBm, +25C		18	TBD	mA
	Transmission mode, -1dBm, -40C to +85C		TBD		
	Receive mode, +25C		20	TBD	mA
	Receive mode, +40C to +85C		TBD		
	Data capture mode, no transceiver activity, +25C		7.2		
	Sleep mode, T_A = 25°C		2.5		μA
Power Supply Current, ADIS16000	Transmission mode, 10dBm, +25C		37		mA
	Transmission mode, -1dBm, +25C		18		mA
	Receive mode, +25C		20		mA

[1] The maximum range depends on the frequency of vibration.
[2] Assumes that frequency flatness calibration is enabled.
[3] The digital I/O signals are 5 V tolerant.
[4] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[5] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime depends on junction temperature.
[6] The start-up times presented reflect the time it takes for data collection to begin.
[7] Applies to the reset line ($\overline{RST}$ = 0) and the software reset command (GLOB_CMD[7] = 1). The $\overline{RST}$ pin must be held low for at least 10 μs.

TIMING SPECIFICATIONS

$T_A = 25°C$, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max	Unit
f_{SCLK}	SCLK frequency	0.01		2.5	MHz
t_{STALL}	Stall period between data, between 16th and 17th SCLK	25			µs
t_{CS}	Chip select to SCLK edge	48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			ns
t_{SR}	SCLK rise time			12.5	ns
t_{SF}	SCLK fall time			12.5	ns
t_{DF}, t_{DR}	DOUT rise/fall times		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			ns

[1] Guaranteed by design, not tested.

Timing Diagrams
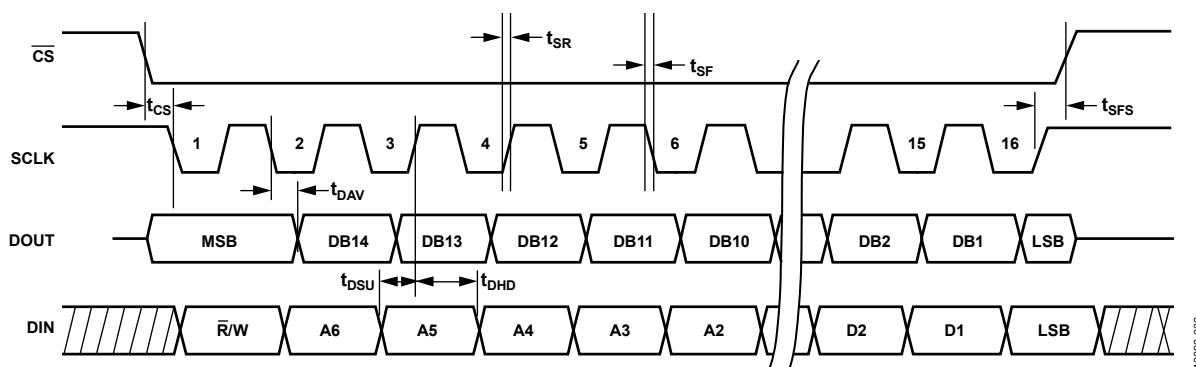
Figure 2. SPI Timing and Sequence
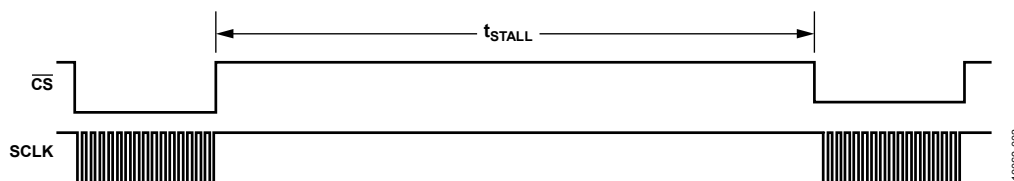
Figure 3. DIN Bit Sequence

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 g
Any Axis, Powered	2000 g
VDD to GND	−0.3 V to +3.96 V
Digital Input Voltage to GND	−0.3 V to +3.96 V
Digital Output Voltage to GND	−0.3 V to +3.96 V
Temperature	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
15-Lead Module	31°C/W	11°C/W	6.5 grams

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
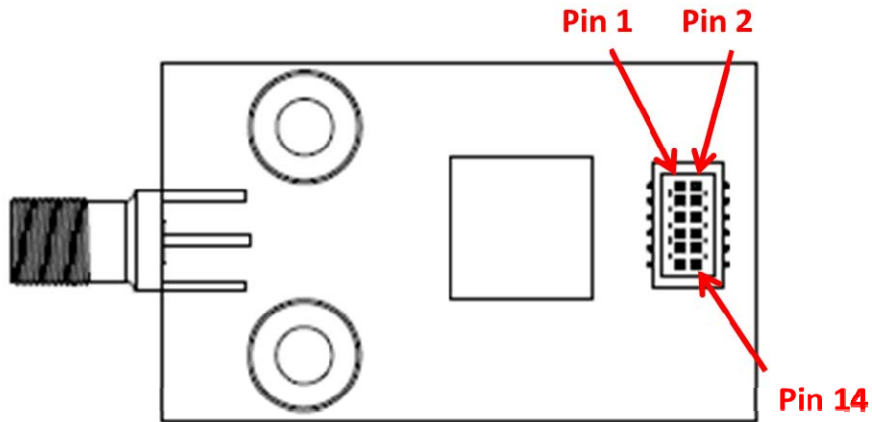
Figure 4. ADIS16000 Pin Assignments

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type¹	Description
1, 2	VDD	S	Power Supply, 3.3 V.
3, 4	GND	S	Ground.
5	DO2	I/O	Digital Input/Output Line 2.
6, 8, 9 , 10	DNC	I/O	Do not connect
7	DOUT	O	SPI, Data Output. DOUT is an output when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is in a three-state, high impedance mode.
9	SCLK	I	SPI, Serial Clock.
11	$\overline{CS}$	I	SPI, Chip Select.
12	DIN/RXD	I	SPI, Data Input.
13	DO1	I/O	Digital Input/Output Line 1.
14	$\overline{RST}$	I	Reset, Active Low.

¹ S is supply, O is output, I is input, and I/O is input/output.

THEORY OF OPERATION

The ADIS16000 is the "Gateway Node" and the ADIS16229 serves as the remote "Sensor Node" in a wireless vibration monitoring system. Using a proprietary wireless protocol, one ADIS16000 can support up to six ADIS16229 nodes at one time in local star network configuration (see Figure 8). As the gateway node, the ADIS16000's SPI interface provides access to an addressable register map that manages configuration parameters (gateway and sensor node), remote alarm flags and remote vibration data. The ADIS16000's SPI interface enables simple connection to most embedded processors and its standard SMA connector supports direct connection to a wide variety of antennas. The ADIS16229 only requires an antenna and battery to start-up, connect with the ADIS16000 and begin operation.

SENSING ELEMENT

Digital vibration sensing in the ADIS16229 starts with a MEMS accelerometer core on two different axes. Accelerometers translate linear changes in velocity into a representative electrical signal, using a micromechanical system like the one shown in Figure 6. The mechanical part of this system includes two different frames (one fixed, one moving) that have a series of plates to form a variable, differential capacitive network. When experiencing the force associated with gravity or acceleration, the moving frame changes its physical position with respect to the fixed frame, which results in a change in capacitance. Tiny springs tether the moving frame to the fixed frame and govern the relationship between acceleration and physical displacement. A modulation signal on the moving plate feeds through each capacitive path into the fixed frame plates and into a demodulation circuit, which produces the electrical signal that is proportional to the acceleration acting on the device.
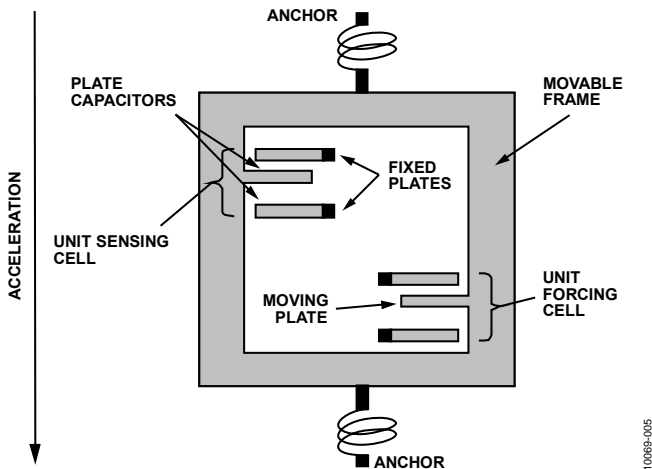
Figure 6. MEMS Sensor Diagram

SIGNAL PROCESSING

Figure 9 offers a simplified block diagram for the ADIS16229. The signal processing stage includes time-domain data capture, digital decimation/filtering, windowing, FFT analysis, FFT

averaging, and record storage. See Figure 16 for more details on the signal processing operation.

SENSOR COMMUNICATION

The ADIS16000 provides access to the ADIS16229 through dedicated pages in the register structure. When the ADIS16000 communicates with a remote ADIS16229, it copies all configuration information in these registers to their respective locations in the ADIS16229 and acquires all of the data in the ADIS16229's output registers/data records.

GATEWAY COMMUNICATION

SPI Interface

The data collection and configuration command uses the SPI, which consists of four wires. The chip select ($\overline{CS}$) signal activates the SPI interface, and the serial clock (SCLK) synchronizes the serial data lines. Input commands clock into the DIN pin, one bit at a time, on the SCLK rising edge. Output data clocks out of the DOUT pin on the SCLK falling edge. Since the ADIS16000 serves only as a SPI slave, the DOUT contents reflect the information requested using a DIN command.

Register organization

The ADIS16000's memory map contains 7 pages of user accessible registers, which enable simple organization of both local (gateway) and remote (sensor) functions. Each page has a page control register (PAGE_ID) address 0x00. Before accessing a register within a particular page, write that page's identification number to this register. For example, write "2" to the PAGE_ID register to access sensor node #2. Once a particular page has been "accessed," there is no need to write the same value to PAGE_ID, in order to access the rest of the registers within that page

Each 16-bit register has its own unique bit assignment and two addresses: one for its upper byte and one for its lower byte. Table 9 and Table 10 provide more details on these memory maps, which list each register, along with its function and lower byte address.

Table 6. ADIS16000 Register Map Page Organization

PAGE_ID	Function	Reference
0x0000	Gateway configuration	Table 9
0x0001	Sensor Node #1	Table 10
0x0002	Sensor Node #2	Table 10
0x0003	Sensor Node #3	Table 10
0x0004	Sensor Node #4	Table 10
0x0005	Sensor Node #5	Table 10
0x0006	Sensor Node #6	Table 10

Dual-Memory Structure

The user registers provide addressing for all input/output operations in the SPI interface. The control registers use a dual-

memory structure. The controller uses SRAM registers for normal operation, including user-configuration commands. The flash memory provides nonvolatile storage for control registers that have flash backup (see Table 9 and Table 10). When the device powers on or resets, the flash memory contents load into the SRAM, and the device starts producing data according to the configuration in the control registers. Storing configuration data in the flash memory requires a manual flash update command. For the ADIS16000, set DIN = 0x8000 (access page 0), then set DIN = 0x9240 (set GLOB_CMD[6] = 1). For a remote ADIS16229, using the following steps to update its flash: (1) turn to its page (DIN = 0x8001, to access note, for example), (2) set DIN = 0xB640 (GLOB_CMD[6] = 1), (3) set DIN = 0x8000 (turn to page 0) and (4) set DIN = 0x9202 (GLOB_CMD[8] = 1).
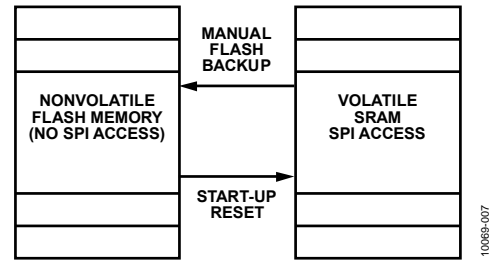
Figure 7. SRAM and Flash Memory Diagram
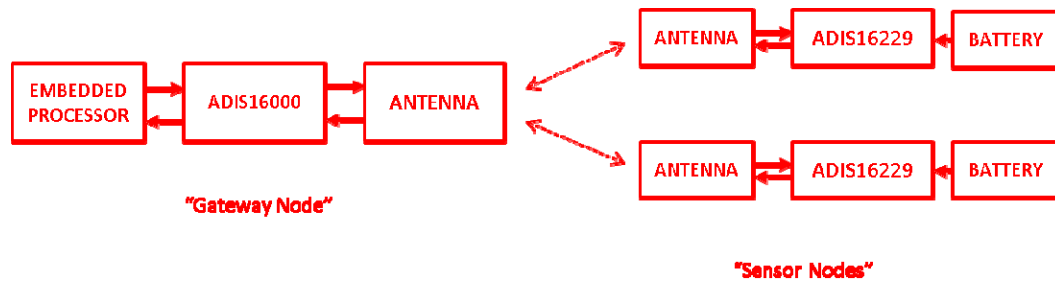
Figure 8. Star Wireless Network Example
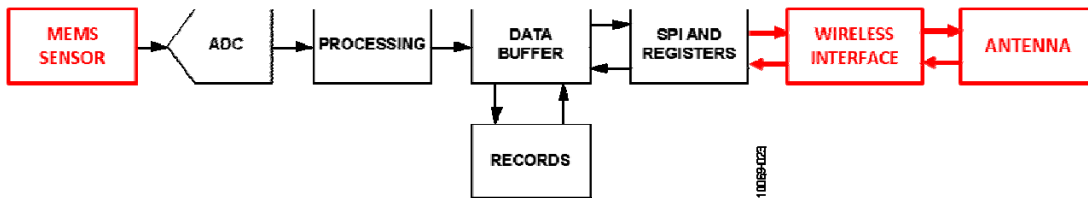
Figure 9. ADIS16229 Simplified Block Diagram

ADIS16000 BASIC OPERATION

Once it has appropriate power on the VDD pin, the ADIS16000 will automatically begin a self-initialization process. Once this process is complete, the SPI interface activates and provides access to its register structure. The SPI interface supports connectivity with most embedded processor platforms, using the connection diagram in Figure 10. The factory default configuration for DO1 provides a busy indicator signal that indicates when to avoid SPI communication requests.
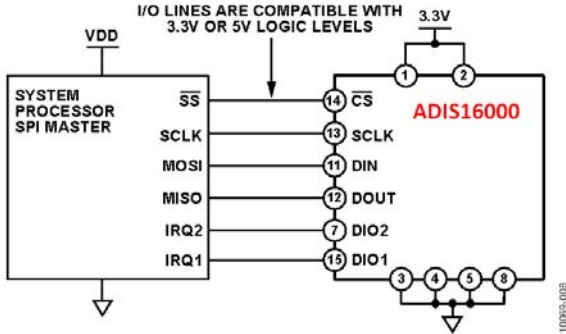
Figure 10. Electrical Hook-Up Diagram

Table 7. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ1, IRQ2	Interrupt request inputs (optional)

The ADIS16000 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 14. Table 8 provides a list of the most common settings that require attention to initialize a processor serial port for the ADIS16000 SPI interface.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16000 operates as a slave.
SCLK Rate ≤ 2.5 MHz	Bit rate setting.
SPI Mode 3	Clock polarity/phase (CPOL = 1, CPHA = 1).
MSB First	Bit sequence.
16-Bit	Shift register/data length.

Table 9 and Table 10 provide lists of user registers with their lower byte addresses. Each register consists of two bytes that each has its own unique 7-bit address. Figure 11 relates the bits of each register to their upper and lower addresses.
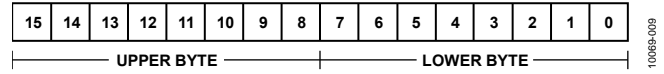
Figure 11. Generic Register Bit Definitions

SPI WRITE COMMANDS

User control registers govern many internal operations. The DIN bit sequence in Figure 14 provides the ability to write to these registers, one byte at a time. Some configuration changes and functions require only one write cycle. For example, set PAGE_ID[7:0] = 1 (DIN = 0x8001) to select Page 1 of the register map.
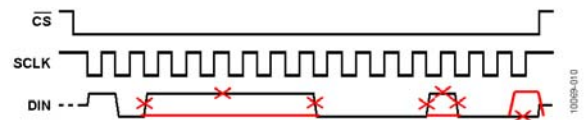
Figure 12. SPI Sequence for Selecting Page 1 for Access (DIN = 0x8001)

SPI READ COMMANDS

A single register read requires two 16-bit SPI cycles that also use the bit assignments that are shown in Figure 14. The first sequence sets R/W = 0 and communicates the target address (Bits[A6:A0]). Bits[D7:D0] are don't care bits for a read DIN sequence. DOUT clocks out the requested register contents during the second sequence. The second sequence can also use DIN to set up the next read. Figure 13 provides a signal diagram for all four SPI signals while reading the PROD_ID. In this diagram, DIN = 0x1600 and DOUT reflects the decimal equivalent of 16,000.

DOUT = 0011 1110 1000 0000 = 0x3E80 = 16,000 = PROD_ID
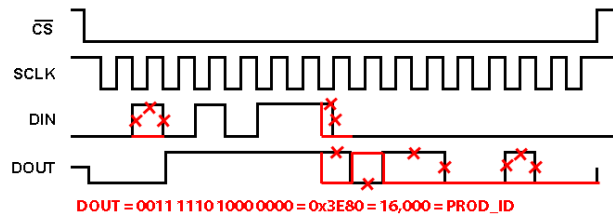
Figure 13. Example SPI Read, PROD_ID (Page 0), Second Sequence
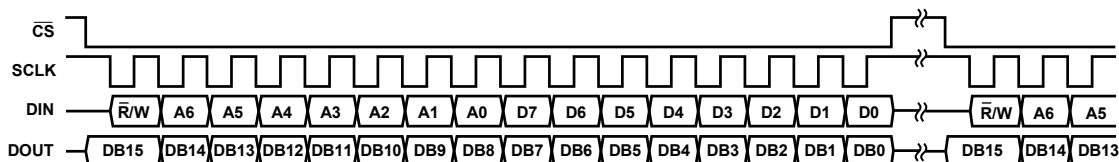
NOTES
1. DOUT BITS ARE BASED ON THE PREVIOUS 16-BIT SEQUENCE ($\overline{R}$/W = 0).

Figure 14. Example SPI Read Sequence

Table 9. User Register Memory Map, PAGE_ID = 0x0000

Register Name	Access	Flash Backup	Address	Default	Function	Reference
PAGE_ID	Read/write	N/A	0x00	0x0000	Page Identifier	
NETWORK_ID	Read/write	Yes	0x02	1234	Network Identifier, unique to a network	
FLASH_CNT	Read	Yes	0x04	N/A	Flash update counter	
NW_ERROR_STAT	Read	No	0x06	0x0000	Network error indicators	
TX_PWR_CTRL_G	Read/write	Yes	0x08	0x0000	Transmission power control, Gateway	
RSSI_G	Read	No	0x0A	0x0000	Received signal strength	
TEMP_OUT_G	Read	No	0x0C	0x8000	Output, temperature	
SUPPLY_OUT_G	Read	No	0x0E	0x8000	Output, supply voltage	
BEACON_SETUP	Read/write	Yes	0x10	0x0000	Beacon frequency	
GLOB_CMD	Read/write	No	0x12	0x0000	System commands	
CMD_DATA	Read/write	No	0x14	0x0000	Data to sensor nodes	
PROD_ID	Read only	Yes	0x16	0x3E80	Product identifier, 16000	
Reserved	N/A	No	0x18	N/A	Reserved	
Reserved	N/A	No	0x1A	N/A	Reserved	
Reserved	N/A	No	0x1C	N/A	Reserved	
Reserved	N/A	No	0x1E	N/A	Reserved	
Reserved	N/A	No	0x20	N/A	Reserved	
Reserved	N/A	No	0x22	N/A	Reserved	
LOT_ID1	Read only	No	0x24	N/A	Lot identifier 1	
LOT_ID2	Read only	No	0x26	N/A	Lot identifier 2	
Reserved	N/A	No	0x28	N/A	Reserved	
GPO_CTRL	Read/write	Yes	0x2A	N/A	General-purpose output control	

Table 10. User Register Memory Map, PAGE_ID ≥ 0x0001

Register Name	Access	Flash Backup	Address	Default[1]	Function	Reference
PAGE_ID	Read/write	N/A	0x00	N/A	Page Identifier	
SENS_ID	Read only	Yes	0x02	N/A	Sensor Identifier	
FLASH_CNT	Read only	Yes	0x04	N/A	Status, flash memory write count	
X_BUF	Read only	No	0x06	0x8000	Output, buffer for x-axis acceleration data	Table 59
Y_BUF	Read only	No	0x08	0x8000	Output, buffer for y-axis acceleration data	Table 60
TEMP_OUT	Read only	No	0x0A	0x8000	Output, temperature during capture	
SUPPLY_OUT	Read only	No	0x0C	0x8000	Output, power supply during capture	
FFT_AVG1	Read/write	Yes	0x0E	0x8000	Control, FFT average size of 1, SR0 and SR1	Table 34
FFT_AVG2	Read/write	Yes	0x10	0x0108	Control, FFT average size of 2, SR2 and SR3	Table 35
BUF_PNTR	Read/write	No	0x12	0x0101	Control, buffer address pointer	Table 57
REC_PNTR	Read/write	No	0x14	0x0000	Control, record address pointer	Table 58
X_SENS	Read/write	No	0x16		Control, x-axis acceleration scale adjustment	Table 32
Y_SENS	Read/write	No	0x18		Control, y-axis acceleration scale adjustment	Table 33
REC_CTRL1	Read/write	Yes	0x1A	0x0002	Record Control Register	Table 27
REC_CTRL2	Read/write	Yes	0x1C	0x000F	Record Control Register	Table 30
			0x1E			
ALM_F_LOW	Read/write	Yes	0x20	0x0000	Spectral Alarm Band, Low Frequency	Table 43
ALM_F_HIGH	Read/write	Yes	0x22	0x0000	Spectral Alarm Band, High Frequency	Table 44
ALM_X_MAG1	Read/write	Yes	0x24	0x0000	Spectral Alarm Band, X-axis, Alarm 1 Magnitude	Table 45
ALM_Y_MAG1	Read/write	Yes	0x26	0x0000	Spectral Alarm Band, Y-axis, Alarm 1 Magnitude	Table 46
ALM_X_MAG2	Read/write	Yes	0x28	0x0000	Spectral Alarm Band, X-axis, Alarm 2 Magnitude	Table 47
ALM_Y_MAG2	Read/write	Yes	0x2A	0x0000	Spectral Alarm Band, Y-axis, Alarm 2 Magnitude	Table 48
ALM_PNTR	Read/write	No	0x2C	0x0000	Spectral Alarm Band Pointer	Table 42
ALM_S_MAG	Read/write	Yes	0x2E	0x0000	Alarm, system alarm threshold	Table 49
ALM_CTRL	Read/write	Yes	0x30	0x0000	Alarm, control register	Table 41
AVG_CNT	Read/write	Yes	0x32	0x9630	Sample rate control (average count)	Table 28
DIAG_STAT	Read only	No	0x34	0x0000	System status register	
GLOB_CMD	Write only	No	0x36	0x0000	Global command register	Table 74
ALM_X_STAT	Read only	No	0x38	0x0000	Alarm, X-axis status register	Table 50
ALM_Y_STAT	Read only	No	0x3A	0x0000	Alarm, Y-axis status register	Table 51
ALM_X_PEAK	Read only	No	0x3C	0x0000	Alarm, X-axis peak level	Table 52
ALM_Y_PEAK	Read only	No	0x3E	0x0000	Alarm, Y-axis peak level	Table 53
TIME_STAMP_L	Read only	No	0x40	0x0000	Time stamp, low integer	Table 72
TIME_STAMP_H	Read only	No	0x42	0x0000	Time stamp, high integer	Table 73
ALM_X_FREQ	Read only	No	0x44	0x0000	Alarm, x-axis, frequency of ALM_X_PEAK	Table 54
ALM_Y_FREQ	Read only	No	0x46	0x0000	Alarm, y-axis, frequency of ALM_Y_PEAK	Table 55
PROD_ID	Read only	Yes	0x48	0x0000	Product identification register	
REC_FLSH_CNT	Read only	No	0x4A	0x0000		Table 39
REC_INFO1	Read only	No	0x4C	0x0000	Record settings 1	Table 70
REC_INFO2	Read only	No	0x4E	0x0000	Record settings 2	Table 71
REC_CNTR	Read only	No	0x50	0x0000	Record counter	Table 37
PKT_TIME_L	Read only	Yes	0x52	0x0000	Received packet time stamp, low integer	
PKT_TIME_H	Read only	Yes	0x54	0x0000	Received packet time stamp, high integer	
PKT_ERR_STAT	Read only	Yes	0x56	0x0000	Missed packets/Error indicator	
TX_PWR_CTRL_S	Read/write	Yes	0x58	0x0000	Transmission power control	
RSSI_S	Read only	Yes	0x5A	0x0000	Received signal strength indicator	
RF_MODE	Read/write	Yes	0x5C		Wireless communication configuration	
UPDAT_INT	Read/write	Yes	0x5E	0x0000	Update interval	
INT_SCL	Read/write	No	0x60	0x0000	Update interval scale	
BEACON_INT	Read/write	Yes	0x62	0x0000	Beacon interval	
USER_SCR	Read only	Yes	0x64	0x0000	User scratch register	

Reserved	N/A	N/A	0x66	N/A	Reserved	
LOT_ID1	Read only	Yes	0x68	N/A	Lot identification 1	
LOT_ID2	Read only	Yes	0x6A	N/A	Lot identification 2	
Reserved	N/A	N/A	0x6C	N/A	Reserved	
Reserved	N/A	N/A	0x6E	N/A	Reserved	
X_ANULL	Read only	Yes	0x70	0x0000	Automatic null value, x-axis	
Y_ANULL	Read only	Yes	0x72	0x0000	Automatic null value, y-axis	
UPDT_FLAG	Read/write	Yes	0x74		Register update tracking register	

[1] All registers in pages 1, 2, 3, 4, 5 and 6 will read 0x0000, prior to connecting with the ADIS16229

NETWORK MANAGEMENT

Once they have an appropriate supply voltage across their VDD and GND pins, both ADIS16000 and ADIS16229 will self-initialize and prepare themselves for connecting. After completing this process, the ADIS16229 will start sending "connection requests" to any available ADIS16000 devices that are within range. The system microcontroller manages the ADIS16000's response to these requests, using the CMD_DATA (See Table 11) and GLOB_CMD registers (See Table 12), which are both in Page 0 of the ADIS16000. Adding an ADIS16229 network requires two steps: (1) write the node number (between 0 and 6) to the CMD_DATA register and then (2) set GLOB_CMD[0] = 1 (DIN = 0x9201, in page 0). After this second step, the connection process can take up to 3 minutes after writing this code. Removing a sensor from the network uses a similar two-step process: (1) write the sensor node number to the CMD_DATA register and then (2) Set GLOB_CMD[8] = 1 (DIN = 0x9301, page 0).

Set GLOB_CMD[1] = 1 (DIN = 0x9202) to initial an update of all of the registers, except those associated with the spectral alarms. Set GLOB_CMD[12] = 1 (DIN = 0x9310) to update all of the alarm registers, after configuring them. Separating this function will help manage the flash memory endurance.

Table 11. CMD_DATA,
Page 0, Low-Byte Address = 0x14, Read/Write

Bits	Description (Default = 0x0000)
[15:4]	Not used
[3:0]	Sensor node for GLOB_CMD[1] and GLOB_CMD[0] commands. Range = 000 (0) to 110 (6)

Table 12. GLOB_CMD
Page 0, Low-Byte Address = 0x12, Write Only

Bits	Description	Execution Time
[15:8]	Not used	
8	Remove sensor node in CMD_DATA from the network	
7	Software reset	
6	Save registers to flash memory	
5	Flash test, compare sum of flash memory with factory value	
4	Clear DIAG_STAT register	
3	Restore factory register settings, including capture buffer and alarm registers	
2	Self-test, result in DIAG_STAT[5]	
1	Update sensor node in CMD_DATA register, in one of the manual modes	
0	Add sensor node in CMD_DATA to the network	

After connecting with an ADIS16229, the ADIS16000 will automatically copy the contents from its own NETWORK_ID[7:0] location (see Table 13) to the SENS_ID[7:0] location in the ADIS16229's page. (see Table 14).

Table 13. NETWORK_ID
Page 0, Low-Byte Address = 0x02, Read/Write

Bits	Description (Default = 0x1234)
[15:0]	Network identification number

The SENS_ID register will contain the value 0x0000 when not connected to a network. When connected to the network, as node 1, it will contain 0xAD34.

Table 14. SENS_ID
Page 1-6, Low-Byte Address = 0x02, Read Only

Bits	Description (Default = 0xAAAA)
[15:0]	Sensor identification

Receiver Signal Strength

The RSSI_G (see Table 15) and RSSI_S (see Table 16) provide tools for tuning the transmission power control at each location. In order to maintain effective communication, keep the transmission power high enough to maintain at least -94dBm in these registers.

Table 15. RSSI_G
Page 0, Low Byte Address = 0x0A, Read Only

Bits	Description (Default = 0x)
[15:0]	Received signal strength Twos complement format, 1 LSB = 1dBm 0x0000 = 0dBm 0xFFA2 = -94dBm

Table 16. RSSI_S
Page 1-6, Low Byte Address = 0x5A, Read Only

Bits	Description (Default = 0x1100)
[15:0]	Received signal strength Twos complement format, 1 LSB = 1dBm 0x0000 = 0dBm 0xFFA2 = -94dBm

Transmission Power Control

Both ADIS16000 and ADIS16229 units provide controls for transmission power in a registers called, TX_PWR_CTRL_G (see Table 17) and TX_PWR_CTRL_S. The registers provide users with the ability to optimize the transmission power for battery optimization and to manage interference influence on other networks. Note that compliance with FCC Part 15.249 involves limiting the transmission power to -1dBm.

Table 17. TX_PWR_CTRL_G
Page 0, Low Byte Address = 0x08, Read/Write

Bits	Description (Default = 0x)
[15:5]	Not used (do not care)
[40]	Transmission power, offset binary format 1LSB = 1.6dBm (25.5/15) 0 = -15.5dBm (minimum) F = +10dBm (maximum)

Table 18. TX_PWR_CTRL_S
Page 1-6, Low Byte Address = 0x58, Read/Write

Bits	Description (Default = 0x)
[15:5]	Not used (do not care)
[40]	Transmission power, offset binary format 1LSB = 1.6dBm (25.5/15) 0 = -15.5dBm (minimum) F = +10dBm (maximum)

Wireless Configuration

The RF_MODE (see Table 19) register provides a number of important wireless configuration parameters. Note that when the transmission power exceeds -1dBm, FCC Part 15.247 requires the use of "frequency-hopping."

Table 19. RF_MODE
Page 0, Low Byte Address = 0x58, Read/Write

Bits	Description (Default = 0x)
[15:9]	Not used (do not care)
[8]	Complete register dump during update cycle (0 = enable, 1 = disable)
[7]	Periodic wake-up/beacon synchronization (0 = disable, 1 = enable)
[6]	Frequency hoping (0 = disable, 1 = enable)
[5]	Complete synchronization after missing 2 beacons (0 = disable, 1 = enable)
[4:2]	Not used (do not care)
[1]	Update gateway on Alarm only (0 = disable, 1 = enable)
[0]	Update gateway on beacon synchronization (0 = disable, 1 = enable)

The UPDAT_INT (See Table 20) and INT_SCL (See Table 21) registers establish the time between wake-up events, where the remote ADIS16229 captures data, analyzes it and communicates the information.

Table 20. UPDAT_INT
Page 1-6, Low Byte Address = 0x5E, Read/Write

Bits	Description (Default = 0x)
[15:0]	Offset binary number, scale factor set by INT_SCL register

Table 21. INT_SCL
Page 1-6, Low Byte Address = 0x60, Read/Write

Bits	Description (Default = 0x)
[15:2]	Not used (do not care)
[1:0]	Scale factor 00 = 30.52μsec/LSB, maximum = 2 seconds 01 = 0.488msc/LSB, maximum = 31.98 seconds 10 = 1/128 sec/LSB, maximum = 512 seconds 11 = 1 sec/LSB, maximum = 18.2 hours

The beacon synchronization function uses periodic monitoring for drift in sensor node clocks and limits their sleep time to 30 minutes (or less) in order to maintain consistent synchronization. The BEACON_SETUP (See Table 22) register provides a user control for this function. When operating in real-time mode (REC_CTRL1 register, See Table 27) this mode is not necessary and automatically turns off.

Table 22. BEACON_SETUP
Page 0, Low Byte Address = 0x10, Read/Write

Bits	Description (Default = 0x)
[15:1]	Not used
0	1 = Beacon synchronization enable

| | 0 = Beacon synchronization disable |

The BEACON_INT (See Table 23) register sets the interval time between re-synchronizing events with the ADIS16000 (gateway).

Table 23. BEACON_INT
Page 1-6, Low Byte Address = 0x62, Read/Write

Bits	Description (Default = 0x)
[15:0]	Offset binary number, scale factor set by INT_SCL register

Communication Tools

The PKT_TIME_H (upper word) and PKT_TIME_L (lower word) registers provide a 32-bit timer for tracking the relative times associated with packet transmission times. This maximum value for this number is 49.71 days. At this point, the registers start over at 0x0000.

Table 24. PKT_TIME_H
Page 1-6, Low Byte Address = 0x54, Read/Write

Bits	Description (Default = N/A))
[15:0]	Offset binary number, upper word

Table 25. PKT_TIME_L
Page 1-6, Low Byte Address = 0x52, Read/Write

Bits	Description (Default = N/A)
[15:0]	Offset binary number, lower word, 1 LSB = 1msec

The NW_ERROR_STAT (see Table 26) register provides all of the error flags associated with the wireless communication.

Table 26. NW_ERROR_STAT
Page 0, Low Byte Address = 0x06), Read/Write

Bits	Description (Default = 0x1100)
[15:12]	Sensor node associated present error flags in this register
[11:10]	Not used
9	Received packet from an unknown device.
8	Packet synchronization failure, from the most recent received packet
7	No response from one or more sensor nodes during beacon synchronization
6	Failed to receive a packet from the sensor node
5	Packet length mismatch
4	Missing packet
3	Packets received out of SYNC
2	Failure to receive acknowledgement from a sensor node
1	Low signal strength from a sensor node, read RSSI_S register for power level of this signal. See Table 16
0	CRC mismatch error associated with the most recent packet from the Sensor Node Packet

SENSOR NODE RECORDING MODE/SIGNAL PROCESSING

The ADIS16229 provides a complete sensing system for recording and monitoring vibration data. Figure 15 provides a simplified block diagram for the signal processing associated with spectral record acquisition on both axes (x and y). User registers provide controls for data type (time or frequency), trigger mode (manual or automatic), collection mode (real time or capture), sample rates/filtering, windowing, FFT averaging, spectral alarms, and I/O management.

RECORDING MODE

The recording mode selection establishes the data type (time or frequency domain), trigger type (manual or automatic), and data collection (captured or real time). The REC_CTRL1[1:0] bits (see Table 27) provide four operating modes: manual FFT, automatic FFT, manual time capture, and real time. After setting REC_CTRL1, the manual FFT, automatic FFT, and manual time capture modes require a start command to start acquiring a spectral or time domain record. All of these modes automatically trigger when the sensor receives the configuration packet from the gateway. Set GLOB_CMD[11] = 1 to halt the operation and wait for further instructions from the ADIS16000..

Table 27. REC_CTRL1
Page 1-6, Low Byte Address = 0x1A, Read/Write

Bits	Description (Default = 0x1100)
[15:14]	Not used (don't care).
[13:12]	Window setting. 00 = rectangular, 01 = Hanning, 10 = flat top, 11 = N/A.
11	SR3, 1 = enabled for FFT, 0 = disable. Sample rate = $20{,}000 \div 2^{AVG\_CNT[15:12]}$ (see Table 28).
10	SR2, 1 = enabled for FFT, 0 = disable. Sample rate = $20{,}000 \div 2^{AVG\_CNT[11:8]}$ (see Table 28).
9	SR1, 1 = enabled for FFT, 0 = disable. Sample rate = $20{,}000 \div 2^{AVG\_CNT[7:4]}$ (see Table 28).
8	SR0, 1 = enabled for FFT, 0 = disable. Sample rate = $20{,}000 \div 2^{AVG\_CNT[3:0]}$ (see Table 28).
7	Power-down between each recording. 1 = enabled.
[6:4]	Not used (don't care).
[3:2]	Storage method. 00 = none, 01 = alarm trigger, 10 = all, 11 = N/A.
[1:0]	Recording mode. 00 = manual FFT, 01 = automatic FFT, 10 = manual time capture, 11 = real-time sampling/data access.

Manual FFT Mode

Set REC_CTRL1[1:0] = 00 to place the device in manual FFT mode, which will result in triggering a single FFT cycle. When the spectral record is complete, the device will transmit the data to the ADIS16000 and wait for another start command.

Automatic FFT Mode

Set REC_CTRL1[1:0] = 01 to place the device in automatic FFT mode. Use the UPDAT_INT and INT_SCL registers to establish the period between "wake-up times," which triggers data capture, FFT computation and analysis.

Manual Time Capture Mode

Set REC_CTRL1[1:0] = 10 to place the device into manual time capture mode, which will result in triggering a single time domain data capture. When the device is operating in this mode, 512 samples of time domain data are loaded into the buffer for each axis. This data goes through all time domain signal processing, except the pre-FFT windowing, prior to loading into the data buffer for user access. When the data record is complete, the device will transmit the data to the ADIS16000 and wait for another start command.
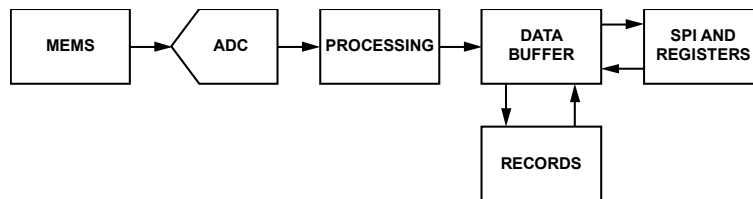

Figure 15. Simplified Block Diagram

Real-Time Mode

Set REC_CTRL1[1:0] = 11 to place the device into real-time mode. In this mode, the device samples only one axis, at a rate of 5 kSPS, and provides data on its output register at the SR0 sample rate setting in AVG_CNT[3:0] (see Table 28). Select the axis of measurement in this mode by reading its assigned register. For example, select the x-axis by reading X_BUF, using DIN = 0x1400. See Table 59 or Table 60 for more information on the x_BUF registers. No other ADIS16229 nodes will be able to communicate with the ADIS16000 when one of them is in real-time mode.

SPECTRAL RECORD PRODUCTION

The ADIS16229 produces a spectral record by taking a time record of data on both axes, then scaling, windowing, and performing an FFT process on each time record. This process repeats for a programmable number of FFT averages, with the FFT result of each cycle accumulating in the data buffer. After completing the selected number of cycles, the FFT averaging process completes by scaling the data buffer contents. Then the data buffer contents are available to the SPI and output data registers.

SAMPLE RATE/FILTERING

The sample rate for each axis is 20 kSPS. The internal ADC samples both axes in a time-interleaving pattern (x1, y1, x2, y2…) that provides even distribution of data across the data record. The averaging/decimating filter provides a control for the final sample rate in the time record. By averaging and decimating the time domain data, this filter provides the ability to focus the spectral record on lower bandwidths, which produces finer frequency resolution in each FFT frequency bin. AVG_CNT (see Table 28) provides the setting for the four different sample rate options in REC_CTRL1[11:8] (SRx, see Table 27). All four options are available when using the manual FFT, automatic FFT, and manual time capture modes. When more than one sample rate option is enabled while the device is in one of the manual modes, the device produces a spectral record for one SRx at a time, starting with the lowest number. After completing the spectral record for one SRx option, the device waits for another start command before producing a spectral record for the next SRx option that is enabled in REC_CTRL1[11:8]. When

more than one sample rate option is enabled while the device is in the automatic FFT mode, the device produces a spectral record for one SRx option, and then waits for the next automatic trigger, which occurs based on the UPDAT_INT and INT_SCL registers. See Figure 17 for more details on how multiple SRx options influence data collection and spectral record production. When in real-time mode, the output data rate reflects the SR0 setting.

Table 29 provides a list of SRx settings available in the AVG_CNT register (see Table 28), along with the resulting sample rates, FFT bin widths, bandwidth, and estimated total noise. Note that each SRx setting also has associated range settings in the REC_CTRL2 register (see Table 30) and the FFT averaging settings that are shown in the FFT_AVG1 and FFT_AVG2 registers (see Table 34 and Table 35, respectively).

Table 28. AVG_CNT
Page 1-6, Low Byte Address = 0x32, Read/Write

Bits	Description (Default = 0x9630)
[15:12]	Sample Rate Option 3, binary (0 to 10), SR3 option sample rate = $20{,}000 \div 2^{AVG\_CNT[15:12]}$
[11:8]	Sample Rate Option 2, binary (0 to 10), SR2 option sample rate = $20{,}000 \div 2^{AVG\_CNT[11:8]}$
[7:4]	Sample Rate Option 1, binary (0 to 10), SR1 option sample rate = $20{,}000 \div 2^{AVG\_CNT[7:4]}$
[3:0]	Sample Rate Option 0, binary (0 to 10), SR0 option sample rate = $20{,}000 \div 2^{AVG\_CNT[3:0]}$

Table 29. Sample Rate Settings and Filter Performance

SRx Option	Sample Rate, f_S (SPS)	Bin Width (Hz)	Bandwidth (Hz)	Peak Noise per Bin (mg)
0	20,000	39.1	10,000	5.18
1	10,000	19.5	5,000	3.66
2	5,000	9.8	2,500	2.59
3	2,500	4.9	1,250	1.83
4	1,250	2.4	625	1.29
5	625	1.2	313	0.91
6	313	0.6	156	0.65
7	156	0.3	78	0.46
8	78	0.2	39	0.32
9	39	0.1	20	0.23
10	20	0.0	10	0.16
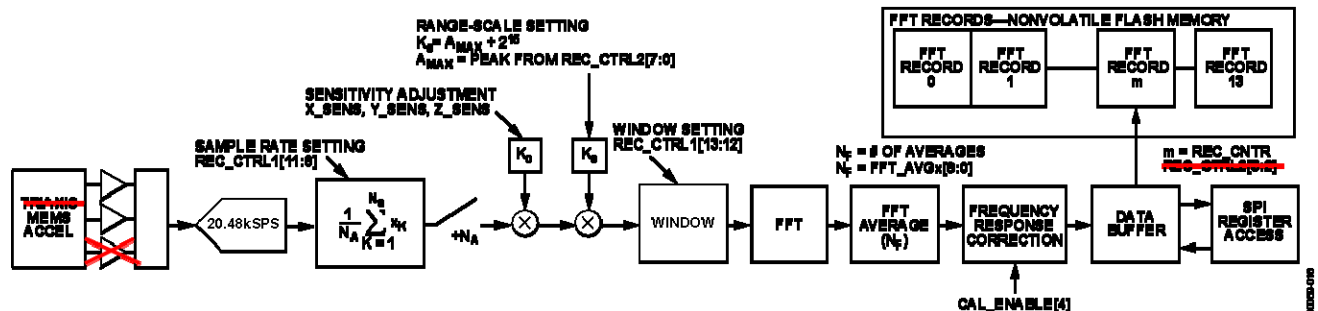
Figure 16. Signal Flow Diagram, REC_CTRL1[1:0] = 00 or 01, FFT Analysis Modes
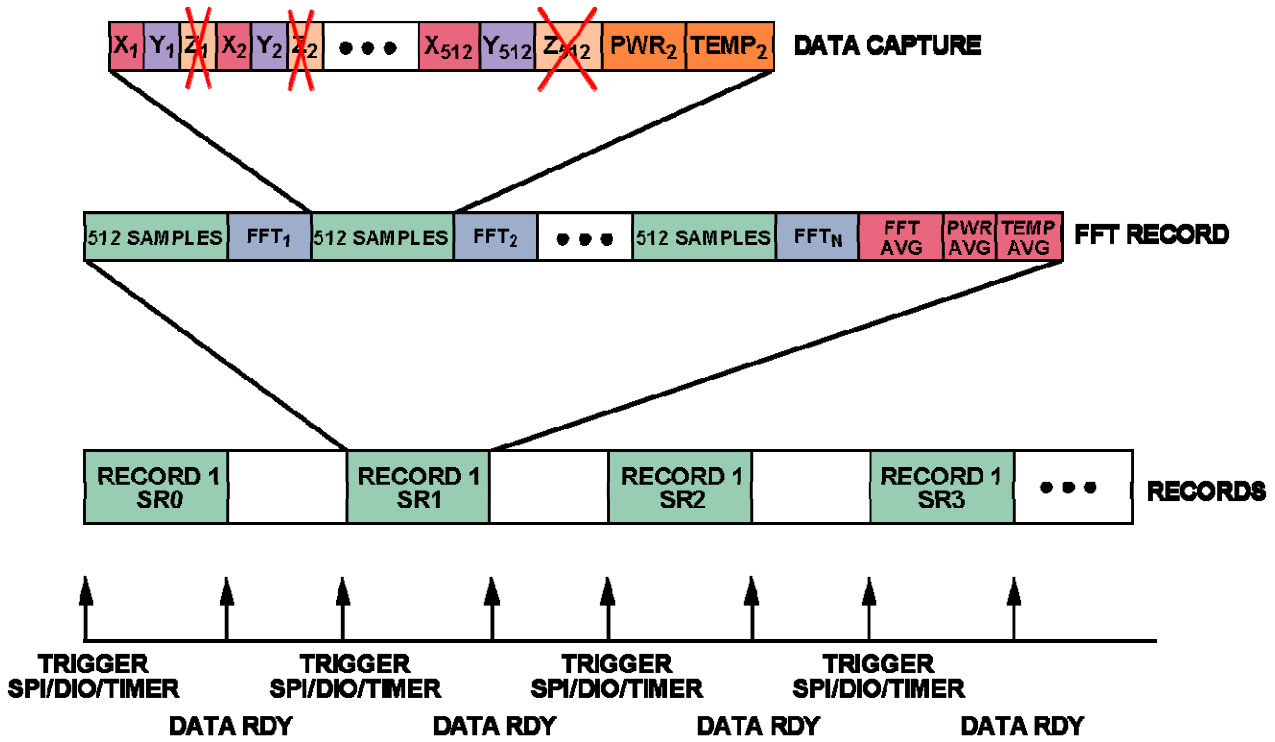
Figure 17. Spectral Record Production, with All SRx Settings Enabled

DYNAMIC RANGE/SENSITIVITY

The range of the ADIS16229 accelerometers depends on the frequency of the vibration. The accelerometers have a self-resonant frequency of 5.5 kHz, and the signal conditioning circuit applies a single-pole, low-pass filter (2.5 kHz) to the response. The self-resonant behavior of the accelerometer influences the relationship between vibration frequency and dynamic range, as shown in Figure 18, which displays the response to peak input amplitudes, assuming a sinusoidal vibration signature at each frequency. The accelerometer resonance and low-pass filter also influence the magnitude response, as shown in Figure 19.
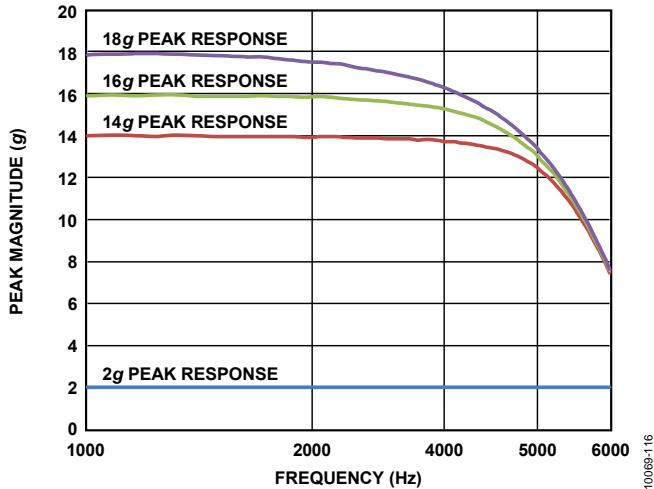
Figure 18. Peak Magnitude vs. Frequency
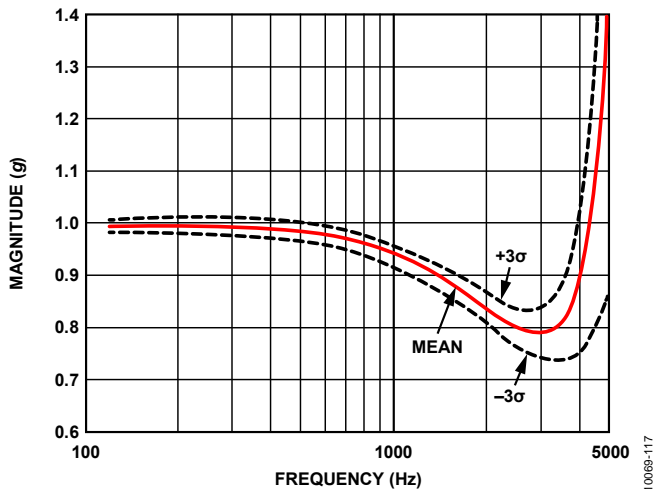
Figure 19. Magnitude/Frequency Response (CAL_ENABLE[4] = 0)

Dynamic Range Settings

REC_CTRL2 (see Table 30) provides four range settings that are associated with each sample rate option, SRx. The range options that are referenced in REC_CTRL2 reflect the maximum dynamic range, which occurs at the lower part of the frequency range and does not account for the decrease in range (see Figure 18). For example, set REC_CTRL2[5:4] = 10 (DIN = 0x9C20) to set the peak acceleration (A_{MAX}) to 10 g on the SR2 sample rate option. These settings help optimize FFT precision and sensitivity when monitoring lower magnitude vibrations. For each range setting in Table 30, this stage scales the time domain data so that the maximum value equates to 2^{15} LSBs for time domain data and 2^{16} LSBs for frequency domain data.

Note that the maximum range for each setting is 1 LSB smaller than the listed maximum. For example, the maximum number of codes in the frequency domain analysis is $2^{16} - 1$, or 65,535. For example, when using a range setting of 1 g in one of the FFT modes, the maximum measurement is equal to 1 g times $2^{16} - 1$, divided by 2^{16}. See Table 31 for the resolution associated with each setting and Figure 16 for the location of this operation in the signal flow diagram. The real-time mode automatically uses the 20 g range setting.

Table 30. REC_CTRL2
Page 1-6, Low Byte Address = 0x1C, Read/Write

Bits	Description (Default = 0x00FF)
[15:8]	Not used (don't care)
[7:6]	Measurement range, SR3 00 = 1 g, 01 = 5 g, 10 = 10 g, 11 = 20 g
[5:4]	Measurement range, SR2 00 = 1 g, 01 = 5 g, 10 = 10 g, 11 = 20 g
[3:2]	Measurement range, SR1 00 = 1 g, 01 = 5 g, 10 = 10 g, 11 = 20 g
[1:0]	Measurement range, SR0 00 = 1 g, 01 = 5 g, 10 = 10 g, 11 = 20 g

Table 31. Range Settings and LSB Weights

Range Setting (g) (REC_CTRL2[5:4])	Time Mode (mg/LSB)	FFT Mode (mg/LSB)
0 to 1	0.0305	0.0153
0 to 5	0.1526	0.0763
0 to 10	0.3052	0.1526
0 to 20	0.6104	0.3052

Scale Adjustment

The x_SENS registers (see Table 32 and Table 33) provide a fine-scale adjustment function for each axis. The following equation describes how to use measured and ideal values to calculate the scale factor for each register in LSBs:

$$SCFx = \left[a_{XI} \middle/ a_{XM} - 1 \right] \times 2^{18}$$

where:

a_{XI} is the ideal x-axis value.

a_{XM} is the actual x-axis measurement.

These registers contain correction factors, which come from the factory calibration process. The calibration process records accelerometer output in four different orientations and computes the correction factors for each register.

These registers also provide write access for in-system adjustment. Gravity provides a common stimulus for this type of correction process. Use both +1 *g* and −1 *g* orientations to reduce the effect of offset on this measurement. In this case, the ideal measurement is 2 *g*, and the measured value is the difference of the accelerometer measurements at +1 *g* and −1 *g* orientations. The factory-programmed values are stored in flash memory and are restored by setting GLOB_CMD[3] = 1 (DIN = 0xB604) (see Table 74).

Table 32. X_SENS
Pages 1-6, Low Byte Address = 0x16, Read/Write

Bits	Description (Default = N/A)
[15:0]	X-axis scale correction factor (SCFx), twos complement

Table 33. Y_SENS
Pages 1-6, Low Byte Address = 0x18, Read/Write

Bits	Description (Default = N/A)
[15:0]	Y-axis scale correction factor (SCFy), twos complement

PRE-FFT WINDOWING

REC_CTRL1[13:12] provide three options for pre-FFT windowing of time data. For example, set REC_CTRL1[13:12] = 01 to use the Hanning window, which offers the best amplitude resolution of the peaks between frequency bins and minimal broadening of peak amplitudes. The rectangular and flat top windows are also available because they are common windowing options for vibration monitoring. The flat top window provides accurate amplitude resolution with a trade-off of broadening the peak amplitudes.

FFT

The FFT process converts each 512-sample time record into a 256-point spectral record that provides magnitude vs. frequency data.

FFT Averaging

The FFT averaging function combines multiple FFT records to reduce the variation of the FFT noise floor, which enables detection of lower vibration levels. Each SRx option in the REC_CTRL1 register has its own FFT average control, which establishes the number of FFT records to average into the final FFT record. To enable this function, write the number of averages for each SRx option that is enabled in the REC_CTRL1 register to the FFT_AVGx registers. For example, set FFT_AVG2[8:0] = 0x4A (DIN = 0x904A) to set the number of FFT averages to 16 for the SR2 sample rate option and 1024 for the SR3 sample rate option.

Table 34. FFT_AVG1

Page 0, Low Byte Address = 0x0E, Read/Write

Bits	Description (Default = 0x0108)
[15:8]	FFT averages for a single record, SR1 sample rate, N_F in Figure 16; range = 1 to 255, binary
[7:0]	FFT averages for a single record, SR0 sample rate, N_F in Figure 16; range = 1 to 255, binary

Table 35. FFT_AVG2

Page 0, Low Byte Address = 0x10, Read/Write

Bits	Description (Default = 0x0101)
[15:8]	FFT averages for a single record, SR3 sample rate, N_F in Figure 16; range = 1 to 255, binary
[7:0]	FFT averages for a single record, SR2 sample rate, N_F in Figure 16; range = 1 to 255, binary

RECORDING TIMES

When using automatic FFT mode, the automatic recording period (REC_PRD) must be greater than the total recording time. Use the following equations to calculate the recording time:

Manual time mode

$$t_R = t_S + t_{PT} + t_{ST} + t_{AST}$$

FFT modes

$$t_R = N_F \times (t_S + t_{PT} + t_{FFT}) + t_{ST} + t_{AST}$$

Table 36 provides a list of the processing times and settings that are used in these equations.

Table 36. Typical Processing Times

Function	Time (ms)
Sample Time, t_S	$1 \div f_S$, per AVG_CNT
Processing Time, t_{PT}	18.7
FFT Time, t_{FFT}	32.7
Number of FFT Averages, N_F	Per FFT_AVG1, FFT_AVG2
Storage Time, t_{ST}	120.0
Alarm Scan Time, t_{AST}	2.21

The storage time (t_{ST}) applies only when a storage method is selected in REC_CTRL1[3:2] (see Table 27 for more details about the record storage settings). The alarm scan time (t_{AST}) applies only when the alarms are enabled in ALM_CTRL[4:0] (see Table 41 for more information). Understanding the recording time helps predict when data is available, for systems that cannot use DO1 to monitor the status of these operations. Note that when using automatic FFT mode, the automatic recording period (REC_PRD) must be greater than the total recording time.

DATA RECORDS

After the ADIS16229 finishes processing FFT data, it stores the data into the data buffer, where it is available for external access using the SPI and x_BUF registers (see Table 59 and Table 60). REC_CTRL1[3:2] (see Table 27) provides programmable conditions for writing buffer data into the FFT records, which are in nonvolatile flash memory locations. Set REC_CTRL1[3:2] = 01 to store data buffer data into the flash memory records only when an alarm condition is met. Set REC_CTRL1[3:2] = 10 to store every set of FFT data into the flash memory locations. The flash memory record provides space for a total of 14 records. Each record stored in flash memory contains a header and frequency domain (FFT) data from all axes (x, and y). When all 14 records are full, new records do not load into the flash memory. The REC_CNTR register (see Table 37) provides a running count for the number of records that are stored. Set GLOB_CMD[8] = 1 (DIN = 0xBF01) to clear all of the records in flash memory.

Table 37. REC_CNTR

Page 0, Low Byte Address = 0x50), Read Only

Bits	Description (Default = 0x0000)
[15:5]	Not used
[4:0]	Total number of records taken; range = 0 to 14, binary

When used in conjunction with automatic trigger mode and record storage, FFT analysis for each sample rate option requires no additional inputs. Depending on the number of FFT averages, the time between each sample rate selection may be quite large. Note that selecting multiple sample rates reduces the number of records available for each sample rate setting, as shown in Table 38.

Table 38. Available Records per Sample Rate Selected

Number of Sample Rates Selected	Available Records
1	14
2	7
3	4
4	3

FFT RECORD FLASH ENDURANCE

The REC_FLSH_CNT register (see Table 39) increments when all 14 records contain FFT data.

Table 39. REC_FLSH_CNT

Page 1-6, Low Byte Address = 0x4A, Read Only

Bits	Description
[15:0]	Flash write cycle count; record data only, binary

SENSOR NODE SPECTRAL ALARMS

The alarm function offers six spectral bands for alarm detection. Each spectral band has high and low frequency definitions, along with two different trigger thresholds (Alarm 1 and Alarm 2) for each accelerometer axis. Table 40 provides a summary of each register used to configure the alarm function.

Table 40. Alarm Function Register Summary

Register	Address	Description
ALM_F_LOW	0x20	Alarm frequency band, lower limit
ALM_F_HIGH	0x22	Alarm frequency band, upper limit
ALM_X_MAG1	0x24	X-Axis Alarm Trigger Level 1 (warning)
ALM_Y_MAG1	0x26	Y-Axis Alarm Trigger Level 1 (warning)
ALM_X_MAG2	0x2A	X-Axis Alarm Trigger Level 2 (fault)
ALM_Y_MAG2	0x2C	Y-Axis Alarm Trigger Level 2 (fault)
ALM_PNTR	0x2C	Alarm pointer
ALM_S_MAG	0x2E	System alarm trigger level
ALM_CTRL	0x30	Alarm configuration
DIAG_STAT	0x34	Alarm status
ALM_X_STAT	0x38	X-axis alarm status
ALM_Y_STAT	0x3A	Y-axis alarm status
ALM_X_PEAK	0x3C	X-axis alarm peak
ALM_Y_PEAK	0x3E	Y-axis alarm peak
ALM_X_FREQ	0x44	X-axis alarm frequency of peak alarm
ALM_Y_FREQ	0x46	Y-axis alarm frequency of peak alarm

The ALM_CTRL register (see Table 41) provides control bits that enable the spectral alarms of each axis, configures the system alarm, sets the record delay for the spectral alarms, and configures the clearing function for the DIAG_STAT error flags (see Table 84).

Table 41. ALM_CTRL
Page 1-6, Low Byte Address = 0x30, Read/Write

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:8]	Response delay; range = 0 to 15. Represents the number of spectral records for each spectral alarm before a spectral alarm flag is set high.
7	Latch DIAG_STAT error flags. Requires a clear status command (GLOB_CMD[4]) to reset the flags to 0. 1 = enabled, 0 = disabled.
6	Enable DO1 as an Alarm 1 output indicator and enable DO2 as an Alarm 2 output indicator. 1 = enabled.
5	System alarm comparison polarity. 1 = trigger when less than ALM_S_MAG[11:0]. 0 = trigger when greater than ALM_S_MAG[11:0].
4	System alarm. 1 = temperature, 0 = power supply.
3	Alarm S enable (ALM_S_MAG). 1 = enabled, 0 = disabled.
2	Not used
1	Alarm Y enable (ALM_Y_MAG). 1 = enabled, 0 = disabled.
0	Alarm X enable (ALM_X_MAG). 1 = enabled, 0 = disabled.

ALARM DEFINITION

The alarm function provides six programmable spectral bands, as shown in Figure 20. Each spectral alarm band has lower and upper frequency definitions for all of the sample rate options

(SRx). It also has two independent trigger level settings, which are useful for systems that value warning and fault condition indicators.
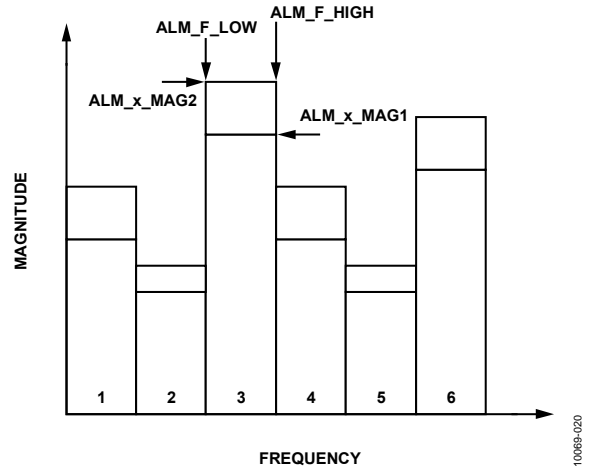
Figure 20. Spectral Band Alarm Setting Example, ALM_PNTR = 0x03

Select the spectral band for configuration by writing its number (1 to 6) to ALM_PNTR[2:0] (see Table 42). Then select the sample rate option using ALM_PNTR[9:8]. This number represents a binary number, which corresponds to the x in the SRx sample rates option associated with REC_CTRL1[11:8] (see). For example, set ALM_PNTR[7:0] = 0x05 (DIN = 0xAC05) to select Alarm Spectral Band 5, and set ALM_PNTR[15:8] = 0x02 (DIN = 0xB102) to select the SR2 sample rate option.

Table 42. ALM_PNTR
Page 1-6, Low Byte Address = 0x2C, Read/Write

Bits	Description (Default = 0x0000)
[15:10]	Not used
[9:8]	Sample rate option; range = 0 to 3 for SR0 to SR3
[7:3]	Not used
[2:0]	Spectral band number; range = 1 to 6

Alarm Band Frequency Definitions

After the spectral band and sample rate settings are set, program the lower and upper frequency boundaries by writing their bin numbers to the ALM_F_LOW register (see Table 43) and ALM_F_HIGH register (see Table 44). Use the bin width definitions listed in Table 29 to convert a frequency into a bin number for this definition. Calculate the bin number by dividing the frequency by the bin width that is associated with the sample rate setting. For example, if the sample rate is 5000 Hz and the lower band frequency is 400 Hz, divide that number by the bin width of 10 Hz to arrive at the 40th bin as the lower band setting. Then set ALM_F_LOW[7:0] = 0x28 (DIN = 0xA028) to establish 400 Hz as the lower frequency for the 5000 SPS sample rate setting.

Table 43. ALM_F_LOW
Page 1-6, Low Byte Address = 0x20, Read/Write

Bits	Description (Default = 0x0000)

[15:8]	Not used
[7:0]	Lower frequency, bin number; range = 0 to 255

Table 44. ALM_F_HIGH
Page 1-6, Low Byte Address = 0x22, Read/Write

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Upper frequency, bin number; range = 0 to 255

Alarm Trigger Settings

The ALM_x_MAG1 and ALM_x_MAG2 registers (see Table 45 to Table 48) provide two independent trigger settings for both axes of acceleration data. They use the data format established by the range settings in the REC_CTRL2 register (see Table 30) and recording mode in REC_CTRL1[1:0] (see Table 27). For example, when using the 0 *g* to 1 *g* mode for FFT analysis, 32,768 LSB is the closest setting to 500 m*g*. Therefore, set ALM_Y_MAG2 = 0x8000 (DIN = 0xAB80, 0xAA00) to set the critical alarm to 500 m*g*, when using the 0 *g* to 1 *g* range option in REC_CTRL2 for FFT records. See Table 30 and Table 31 for more information about formatting each trigger level. Note that trigger settings that are associated with Alarm 2 should be greater than the trigger settings for Alarm 1. In other words, the alarm magnitude settings should meet the following criteria:

ALM_X_MAG2 > ALM_X_MAG1
ALM_Y_MAG2 > ALM_Y_MAG1

Table 45. ALM_X_MAG1
Page 1-6, Low Byte Address = 0x24, Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis Alarm Trigger Level 1, 16-bit unsigned (see Table 30 and Table 31 for the scale factor)

Table 46. ALM_Y_MAG1
Page 1-6, Low Byte Address = 0x26, Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Y-axis Alarm Trigger Level 1, 16-bit unsigned (see Table 30 and Table 31 for the scale factor)

Table 47. ALM_X_MAG2
Page 1-6, Low Byte Address = 0x2A, Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis Alarm Trigger Level 2, 16-bit unsigned (see Table 30 and Table 31 for the scale factor)

Table 48. ALM_Y_MAG2
Page 1-6, Low Byte Address = 0x2C, Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Y-axis Alarm Trigger Level 2, 16-bit unsigned (see Table 30 and Table 31 for the scale factor)

Table 49. ALM_S_MAG
Page 1-6, Low Byte Address = 0x2E, Read/Write

Bits	Description (Default = 0x0000)
[15:0]	System alarm trigger level, data format matches target from ALM_CTRL[4]

Enable Alarm Settings

Before configuring the spectral alarm registers, clear their current contents by setting GLOB_CMD[9] = 1 (DIN = 0xB702). After completing the spectral alarm band definitions, save the settings by setting GLOB_CMD[12] = 1 (DIN = 0xB710). The device ignores the save command if any of these locations has already been written to.

ALARM INDICATOR SIGNALS

GPO_CTRL[5:0] (see Table 83) and ALM_CTRL[6] (see Table 41) provide controls for establishing DO1 and DO2 as dedicated alarm output indicator signals. Use GPO_CTRL[5:0] to select the alarm function for DO1 and/or DO2; then set ALM_CTRL[6] = 1 to enable DO1 to serve as an Alarm 1 indi-cator and DO2 as an Alarm 2 indicator. This setting establishes DO1 to indicate Alarm 1 (warning) conditions and DO2 to indicate Alarm 2 (critical) conditions.

ALARM FLAGS AND CONDITIONS

The FFT header (see Table 69) contains both generic alarm flags (DIAG_STAT[13:8]; seeTable 84) and spectral band-specific alarm flags (ALM_x_STAT; see Table 50, Table 51). The FFT header also contains magnitude (ALM_x_PEAK; see Table 52, Table 53) and frequency information (ALM_x_FREQ; see Table 54, Table 55) associated with the highest magnitude of vibration content in the record.

ALARM STATUS

The ALM_x_STAT registers (see Table 50, Table 51) provide alarm bits for each spectral band on the current sample rate option.

Table 50. ALM_X_STAT
Low Byte Address = 0x38, Read Only

Bits	Description (Default = 0x0000)
15	Alarm 2 on Band 6; 1 = alarm set, 0 = no alarm
14	Alarm 1 on Band 6; 1 = alarm set, 0 = no alarm
13	Alarm 2 on Band 5; 1 = alarm set, 0 = no alarm
12	Alarm 1 on Band 5; 1 = alarm set, 0 = no alarm
11	Alarm 2 on Band 4; 1 = alarm set, 0 = no alarm
10	Alarm 1 on Band 4; 1 = alarm set, 0 = no alarm
9	Alarm 2 on Band 3; 1 = alarm set, 0 = no alarm
8	Alarm 1 on Band 3; 1 = alarm set, 0 = no alarm
7	Alarm 2 on Band 2; 1 = alarm set, 0 = no alarm
6	Alarm 1 on Band 2; 1 = alarm set, 0 = no alarm
5	Alarm 2 on Band 1; 1 = alarm set, 0 = no alarm
4	Alarm 1 on Band 1; 1 = alarm set, 0 = no alarm
3	Not used
[2:0]	Most critical alarm condition, spectral band; range = 1 to 6

Table 51. ALM_Y_STAT
Low Byte Address = 0x3C, Read Only

Bits	Description (Default = 0x0000)
15	Alarm 2 on Band 6; 1 = alarm set, 0 = no alarm
14	Alarm 1 on Band 6; 1 = alarm set, 0 = no alarm
13	Alarm 2 on Band 5; 1 = alarm set, 0 = no alarm
12	Alarm 1 on Band 5; 1 = alarm set, 0 = no alarm
11	Alarm 2 on Band 4; 1 = alarm set, 0 = no alarm
10	Alarm 1 on Band 4; 1 = alarm set, 0 = no alarm
9	Alarm 2 on Band 3; 1 = alarm set, 0 = no alarm
8	Alarm 1 on Band 3; 1 = alarm set, 0 = no alarm
7	Alarm 2 on Band 2; 1 = alarm set, 0 = no alarm
6	Alarm 1 on Band 2; 1 = alarm set, 0 = no alarm
5	Alarm 2 on Band 1; 1 = alarm set, 0 = no alarm
4	Alarm 1 on Band 1; 1 = alarm set, 0 = no alarm
3	Not used
[2:0]	Most critical alarm condition, spectral band; range = 1 to 6

WORST-CASE CONDITION MONITORING

The ALM_x_PEAK registers (see Table 52, Table 53) contain the peak magnitude for the worst-case alarm condition in each axis. The ALM_x_FREQ registers (see Table 54, Table 55) contain the frequency bin number for the worst-case alarm condition.

Table 52. ALM_X_PEAK
Page 1-6, Low Byte Address = 0x3C, Read Only

Bits	Description (Default = 0x0000)
[15:0]	Alarm peak, x-axis, accelerometer data format

Table 53. ALM_Y_PEAK
Page 1-6, Low Byte Address = 0x3E, Read Only

Bits	Description (Default = 0x0000)
[15:0]	Alarm peak, y-axis, accelerometer data format

Table 54. ALM_X_FREQ
Page 1-6, Low Byte Address = 0x44, Read Only

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Alarm frequency for x-axis peak alarm level, FFT bin number; range = 0 to 255

Table 55. ALM_Y_FREQ
Page 1-6, Low Byte Address = 0x46, Read Only

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Alarm frequency for y-axis peak alarm level, FFT bin number; range = 0 to 255

READING OUTPUT DATA

After the ADIS16229 updates the ADIS16000 with its data, it is available in the data buffer and FFT records (if selected). In manual time capture mode, the record for each axis contains 512 samples. In manual and automatic FFT mode, each record contains the 256-point FFT result for each accelerometer axis. Table 56 provides a summary of registers that provide access to processed sensor data.

Table 56. Output Data Registers

Register	Address	Description
TEMP_OUT	0x0A	Internal temperature
SUPPLY_OUT	0x0C	Internal power supply
BUF_PNTR	0x12	Data buffer index pointer
REC_PNTR	0x14	FFT record index pointer
X_BUF	0x06	X-axis accelerometer buffer
Y_BUF	0x08	Y- axis accelerometer buffer
GLOB_CMD	0x36	FFT record retrieve command
TIME_STAMP_L	0x40	Time stamp, lower word
TIME_STAMP_H	0x42	Time stamp, upper word
REC_INFO1	0x4C	FFT record header information
REC_INFO2	0x4E	FFT record header information

READING DATA FROM THE DATA BUFFER

After completing a spectral record and updating each data buffer, the ADIS16000 loads the first data sample from each data buffer into the x_BUF registers (see Table 59 and Table 60) and sets the buffer index pointer in the BUF_PNTR register (see Table 57) to 0x0000. The index pointer determines which data samples load into the x_BUF registers. For example, writing 0x009F to the BUF_PNTR register (DIN = 0x9300, DIN = 0x929F) causes the 160th sample in each data buffer location to load into the x_BUF registers. The index pointer increments with every x_BUF read command, which causes the next set of capture data to load into each capture buffer register automatically. This enables an efficient method for reading all 256 samples in a record, using sequential read commands, without having to manipulate the BUF_PNTR register.

Figure 21. Data Buffer Structure and Operation

Table 57. BUF_PNTR

Page 1-6, Low Byte Address =10, Read/Write

Bits	Description (Default = 0x0000)
[15:9]	Not used
[8:0]	Data bits; range = 0 to 255 (FFT), 0 to 511 (time)

ACCESSING FFT RECORD DATA

The FFT records can be stored in flash memory. The REC_PNTR register (see Table 58) and GLOB_CMD[13] (see Table 74) provide access to the FFT records, as shown in Figure 22. For example, set REC_PNTR[7:0] = 0x0A (DIN = 0x940A) and GLOB_CMD[13] = 1 (DIN = 0xB720) to load FFT Record 10 in the FFT buffer for SPI/register access.

Table 58. REC_PNTR

Page 1-6, Low Byte Address = 0x14, Read/Write

Bits	Description (Default = 0x0000)
[15:4]	Not used
[3:0]	Data bits

Figure 22. FFT Record Access
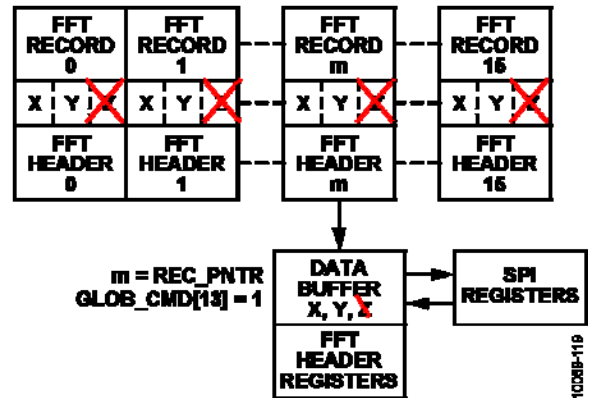
DATA FORMAT

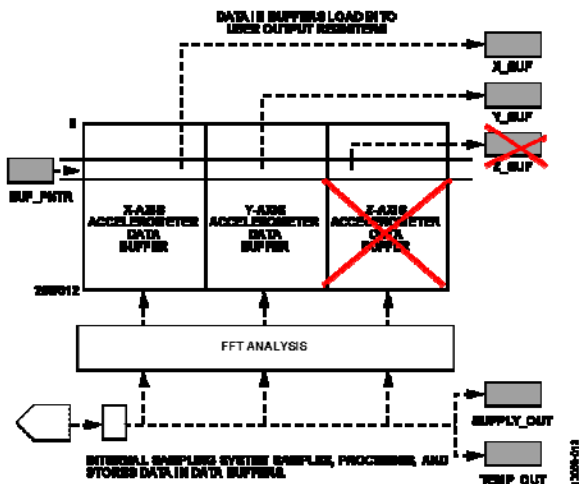Table 59 and Table 60 list the bit assignments for the x_BUF registers. The acceleration data format depends on the range scale setting in REC_CTRL2 (see Table 30) and the recording mode settings in REC_CTRL1 (see Table 27). Table 61 provides some data formatting examples for the FFT mode, and Table 62 offers some data formatting examples for the16-bit, twos complement format used in manual time mode.

Table 59. X_BUF
Low Byte Address = 0x06, Read Only

Bits	Description (Default = 0x8000)
[15:0]	X-acceleration data buffer register.
	See Table 31 for scale sensitivity.
	Format = twos complement (time), binary (FFT).

Table 60. Y_BUF
Low Byte Address = 0x08, Read Only

Bits	Description (Default = 0x8000)
[15:0]	Y-acceleration data buffer register.
	See Table 31 for scale sensitivity.
	Format = twos complement (time), binary (FFT).

Table 61. FFT Mode, 5 *g* Range, Data Format Examples

Acceleration (mg)	LSB	Hex	Binary
4,999.9237	65,535	0xFFFF	1111 1111 1111 1111
$100 \times 5 \div 65,536$	100	0x0064	0000 0000 0110 0100
$2 \times 5 \div 65,536$	2	0x0002	0000 0000 0000 0010
$1 \times 5 \div 65,536$	1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000

Table 62. Manual Time Mode, 5 *g* Range, Data Format Examples

Acceleration (m*g*)	LSB	Hex	Binary
+4999.847	+32,767	0x7FFF	1111 1111 1111 1111
~1000	+6,554	0x199A	0001 0001 1001 1010
$+2 \times 5 \div 32,768$	+2	0x0002	0000 0000 0000 0010
$+1 \times 5 \div 32,768$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-1 \times 5 \div 32,768$	−1	0xFFFF	1111 1111 1111 1111
$-2 \times 5 \div 32,768$	−2	0xFFFE	1111 1111 1111 1110
~−1000	−6554	0xE666	1110 0110 0110 0110
−5000	−32,768	0x8000	1000 0000 0000 0000

REAL-TIME DATA COLLECTION

When using real-time mode, select the output channel by reading the associated x_BUF register. For example, set DIN = 0x1600 to select the y-axis sensor for sampling. After selecting the channel, use the data-ready signal to trigger subsequent data reading of the Y_BUF register. In this mode, use the time domain data formatting for a range setting of 20 *g*, as shown in Table 31.

POWER SUPPLY/TEMPERATURE

At the end of each spectral record, the ADIS16229 also measures power supply and internal temperature. It accumulates a 5.12 ms record of power supply measurements at a sample rate of 50 kHz and takes 64 samples of internal temperature data over a period of 1.7 ms. The average of the power supply and internal tempera-ture loads into the SUPPLY_OUT register (see

Table 64 and Table 65) and the TEMP_OUT registers (See

Table 66 and Table 67), respectively. When using real-time mode, these registers update only when this mode starts.

Table 63. SUPPLY_OUT
Page 0, Low Byte Address = 0x0C, Read Only

Bits	Description (Default = 0x8000)
[15:12]	Not used
[11:0]	Power supply, binary, 3.3 V = 0xA8F, 1.22 mV/LSB

Table 64. SUPPLY_OUT
Page 1- 6, Low Byte Address = 0x0A, Read Only

Bits	Description (Default = 0x8000)
[15:12]	Not used
[11:0]	Power supply, binary, 3.3 V = 0xA8F, 1.22 mV/LSB

Table 65. Power Supply Data Format Examples

Supply Level (V)	LSB	Hex	Binary
3.6	2949	0xB85	1011 1000 0101
3.3 + 0.0012207	2704	0xA90	1010 1001 0000
3.3	2703	0xA8F	1010 1000 1111
3.3 − 0.0012207	2702	0xA8E	1010 1000 1110
3.15	2580	0xA14	1010 0001 0100

Table 66. TEMP_OUT
Page 0, Low Byte Address = 0x0E, Read Only

Bits	Description (Default = 0x8000)
[15:12]	Not used
[11:0]	Temperature data, offset binary, 1278 LSB = +25°C, −0.47°C/LSB

Table 67. TEMP_OUT
Page 1-6, Low Byte Address = 0x0C8, Read Only

Bits	Description (Default = 0x8000)
[15:12]	Not used
[11:0]	Temperature data, offset binary, 1278 LSB = +25°C,

−0.47°C/LSB

Table 68. Internal Temperature Data Format Examples

Temperature (°C)	LSB	Hex	Binary
125	1065	0x429	0100 0010 1001
25 + 0.47	1277	0x4FD	0100 1111 1101
25	1278	0x4FE	0100 1111 1110
25 − 0.47	1279	0x4FF	0100 1111 1111
0	1331	0x533	0101 0011 0011
−40	1416	0x588	0101 1000 1000

FFT EVENT HEADER

Each FFT record has an FFT header that contains information that fills all of the registers listed in Table 69. The information in these registers contains recording time, record configuration settings, status/error flags, and several alarm outputs. The registers listed in Table 69 update with every record event and also update with record-specific information when using GLOB_CMD[13] (see Table 74) to retrieve a data set from the FFT record in flash memory.

Table 69. FFT Header Register Information

Register	Address	Description
DIAG_STAT	0x34	Alarm status
ALM_X_STAT	0x38	X-axis alarm status
ALM_Y_STAT	0x3A	Y-axis alarm status
ALM_X_PEAK	0x3C	X-axis alarm peak
ALM_Y_PEAK	0x3E	Y-axis alarm peak
TIME_STMP_L	0x40	Time stamp, lower word
TIME_STMP_H	0x42	Time stamp, upper word
ALM_X_FREQ	0x44	X-axis alarm frequency of peak alarm
ALM_Y_FREQ	0x46	Y-axis alarm frequency of peak alarm
REC_INFO1	0x4C	FFT record header information
REC_INFO2	0x4E	FFT record header information

The REC_INFO1 register (see Table 70) and the REC_INFO2 register (see Table 71) capture the settings associated with the current FFT record.

Table 70. REC_INFO1
Page 1-6, Low Byte Address = 0x4E), Read Only

Bits	Description
[15:14]	Sample rate option 00 = SR0, 01 = SR1, 10 = SR2, 11 = SR3
[13:12]	Window setting 00 = rectangular, 01 = Hanning, 10 = flat top, 11 = N/A
[11:10]	Signal range 00 = 1 *g*, 01 = 5 *g*, 10 = 10 *g*, 11 = 20 *g*
[9:8]	Not used (don't care)
[7:0]	FFT averages; range = 1 to 255

Table 71. REC_INFO2
Page 1-6, Low Byte Address = 0x4E, Read Only

Bits	Description
[15:4]	Not used (don't care)
[3:0]	AVG_CNT setting

The TIME_STMP_x registers (see Table 72 and Table 73) provide a relative time stamp that identifies the time for the current FFT record.

Table 72. TIME_STMP_L
Page 1-6, Low Byte Address = 0x40, Read Only

Bits	Description (Default = 0x0000)
[15:0]	Record time stamp, low integer, binary, seconds

Table 73. TIME_STMP_H
Page 1-6, Low Byte Address = 0x42, Read Only

Bits	Description (Default = 0x0000)
[15:0]	Record time stamp, high integer, binary, seconds

SYSTEM TOOLS

GLOBAL COMMANDS

The GLOB_CMD register (see Table 74) provides an array of single-write commands for convenience. Setting the assigned bit to 1 activates each function. When the function completes, the bit restores itself to 0. For example, clear the capture buffers by setting GLOB_CMD[8] = 1 (DIN = 0xB701). All of the commands in the GLOB_CMD register require that the power supply be within normal limits for the execution times listed in Table 74.

Table 74. GLOB_CMD
Page 1-6, Low Byte Address = 0x36, Write Only

Bits	Description	Execution Time
15	Clear autonull correction	35 µs
14	Retrieve spectral alarm band information from the ALM_PNTR setting	40 µs
13	Retrieve record data from flash memory	1.9 ms
12	Save spectral alarm band registers to SRAM	461 µs
11	Record start/stop	N/A
10	Set BUF_PNTR = 0x0000	36 µs
9	Clear spectral alarm band registers from flash memory	25.8 ms
8	Clear records	25.9 ms
7	Software reset	52 ms
6	Save registers to flash memory	29.3 ms
5	Flash test, compare sum of flash memory with factory value	5 ms
4	Clear DIAG_STAT register	36 µs
3	Restore factory register settings and clear the capture buffers	84 ms
2	Self-test, result in DIAG_STAT[5]	32.9 ms
1	Power-down	N/A
0	Autonull	822 ms

DEVICE IDENTIFICATION

Table 75. LOT_ID1
Page = 0, Low Byte Address = 0x1A, Read Only

Bits	Description
[15:0]	Lot identification code

Table 76. LOT_ID1
Page = 1-6, Low Byte Address = 0x68, Read Only

Bits	Description
[15:0]	Lot identification code

Table 77. LOT_ID2
Page 0, Low Byte Address = 0x1C, Read Only

Bits	Description
[15:0]	Lot identification code

Table 78. LOT_ID2
Page 1-6, Low Byte Address = 0x6A, Read Only

Bits	Description
[15:0]	Lot identification code

Table 79. PROD_ID
Page 0, Low Byte Address = 0x16), Read Only

Bits	Description (Default = 0x3E80
[15:0]	0x3E80 = 16,000

Table 80. PROD_ID
Page 0, Low Byte Address = 0x48), Read Only

Bits	Description (Default = 0x3E80
[15:0]	0x3F65 = 16,229

Table 81. SERIAL_NUM (Base Address = 0x58), Read Only

Bits	Description
[15:0]	Serial number, lot specific

Table 82 shows a blank register that is available for writing user-specific identification.

Table 82. USER_ID (Base Address = 0x5C), Read/Write

Bits	Description (Default = 0x000)
[15:0]	User-written identification

Table 83. GPO_CTRL
Page 0, Low Byte Address = 0x2A, Read/Write

Bits	Description (Default = 0x)
[15:6]	Not used
[5:4]	DO2 Function selection 00 = General purpose 01 = Alarm indicator 10 = Busy indicator/data-ready (real-time mode) 11 = Not used
[3:2]	DO1 Function selection 00 = General purpose 01 = Alarm indicator 10 = Busy indicator/data-ready (real-time mode) 11 = Not used
1	DO2 Polarity 1 = active high

| 0 | 0 = active low DO1 Polarity 1 = active high 0 = active low |

STATUS/ERROR FLAGS

Critical system error flags are in the DIAG_STAT register for each ADIS16229. These flags indicate various error or alarm conditions that may influence system performance. Multiple flags in these registers can be high at one time and the flags will persist (go high again, after clearing) when the error conditions continue to exist. The flags in bits 0 through 6 will remain in a latch condition, until clearing the problem or clearing (using Use GLOB_CMD[4]). The Alarm flags (upper byte) will latch if ALM_CTRL[7] = 1 (See Table 41)

Table 84. DIAG_STAT
Page 1-6, Low Byte Address = 0x34, Read/Write

Bits	Description (Default = 0x)
15	Not used
14	System alarm (1 = error condition exists, 0 = no error)
13	Not used
12	Sensor Node 6 (1 = alarm condition, 0 = no alarm)
11	Sensor Node 5 (1 = alarm condition, 0 = no alarm)
10	Sensor Node 4 (1 = alarm condition, 0 = no alarm)
9	Sensor Node 3 (1 = alarm condition, 0 = no alarm)
8	Sensor Node 2 (1 = alarm condition, 0 = no alarm)
7	Sensor Node 1 (1 = alarm condition, 0 = no alarm)
6	Flash memory failure, from GLOB_CMD[5] test
[5:4]	Not used
3	SPI communication failure (SCLKs ≠ even multiple of 16)
2	Flash update failure
1	Power supply > 3.625 V
0	Power supply < 3.125 V

SELF-TEST

Set GLOB_CMD[2] = 1 (DIN = 0xBE02) (see Table 74) to run an automatic self-test routine, which reports a pass/fail result to DIAG_STAT[5] (see Table 84).

FLASH MEMORY MANAGEMENT

Set GLOB_CMD[5] = 1 (DIN = 0xB620) to run an internal checksum test on the flash memory, which reports a pass/fail result to DIAG_STAT[6]. The FLASH_CNT register (see Table 85) provides a running count of flash memory write cycles. This is a tool for managing the endurance of the flash memory. Figure 23 quantifies the relationship between data retention and junction temperature.

Table 85. FLASH_CNT
Page 1-6, Low Byte Address = 0x04, Read Only

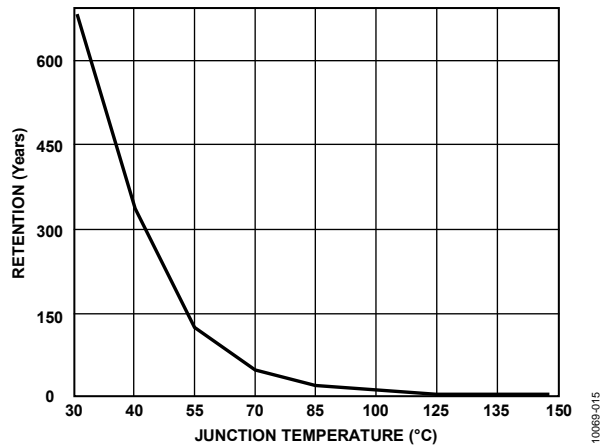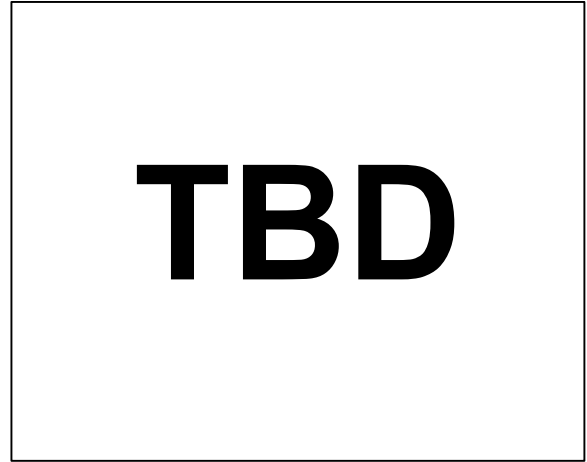| Bits	Description
[15:0]	Binary counter for writing to flash memory

Figure 23. Flash®/EE Memory Data Retention

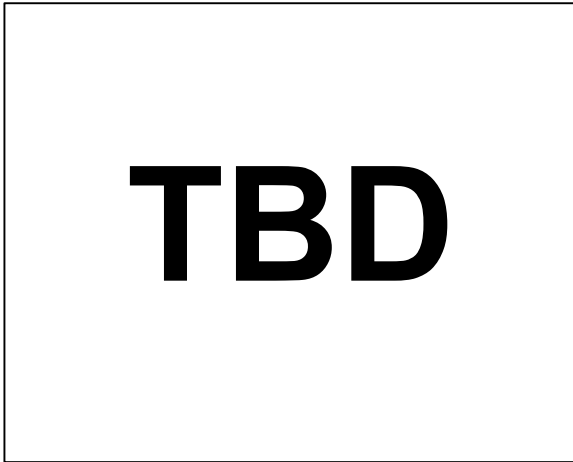# APPLICATIONS INFORMATION

INTERFACE BOARD

The ADIS16COM1/PCBZ accessory provides a direct attachment method for connecting the ADIS16000CMLZ directly to the EVAL-ADIS evaluation system.
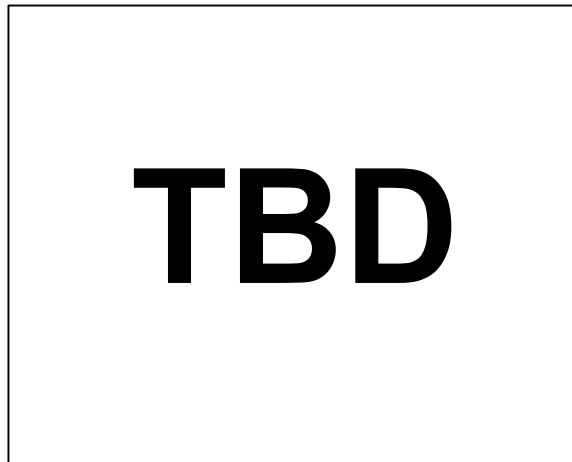
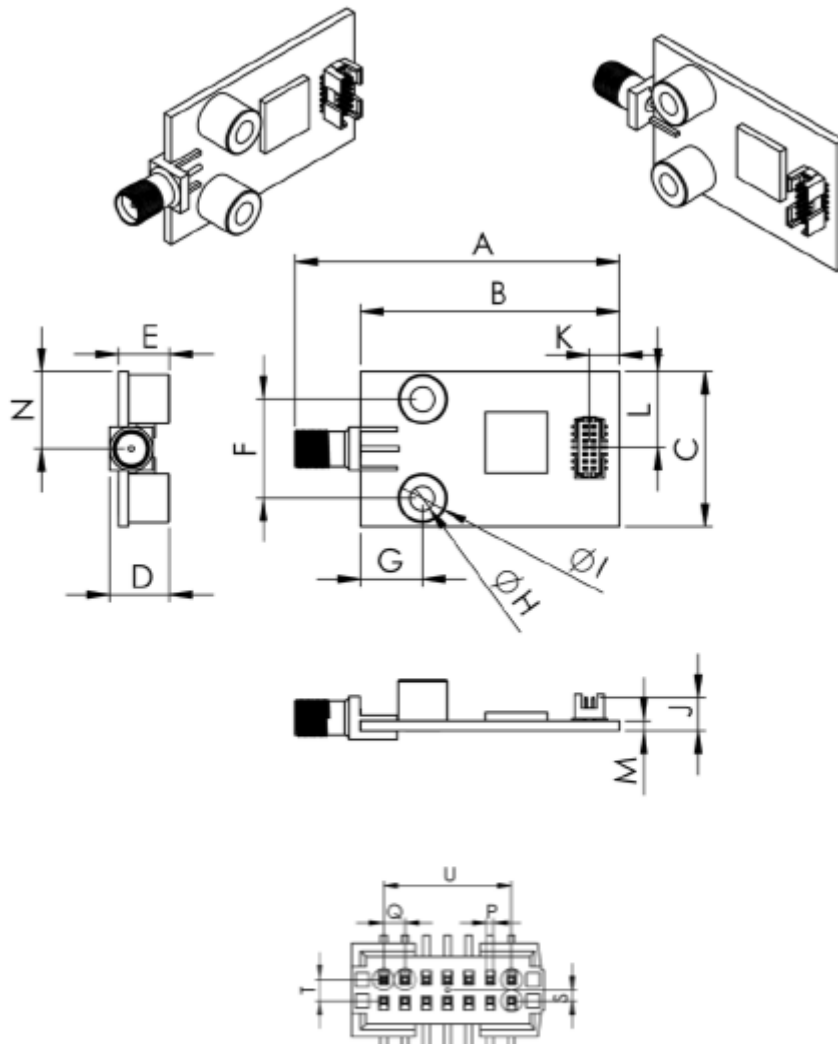## MATING CONNECTOR

TBD

TBD

Figure 25. Mating Connector Detail

TBD

Figure 24. PCB Assembly View and Dimensions

TBD

Figure 26. Electrical Schematic

OUTLINE DIMENSIONS

SAMTEC 14 Pin Connector
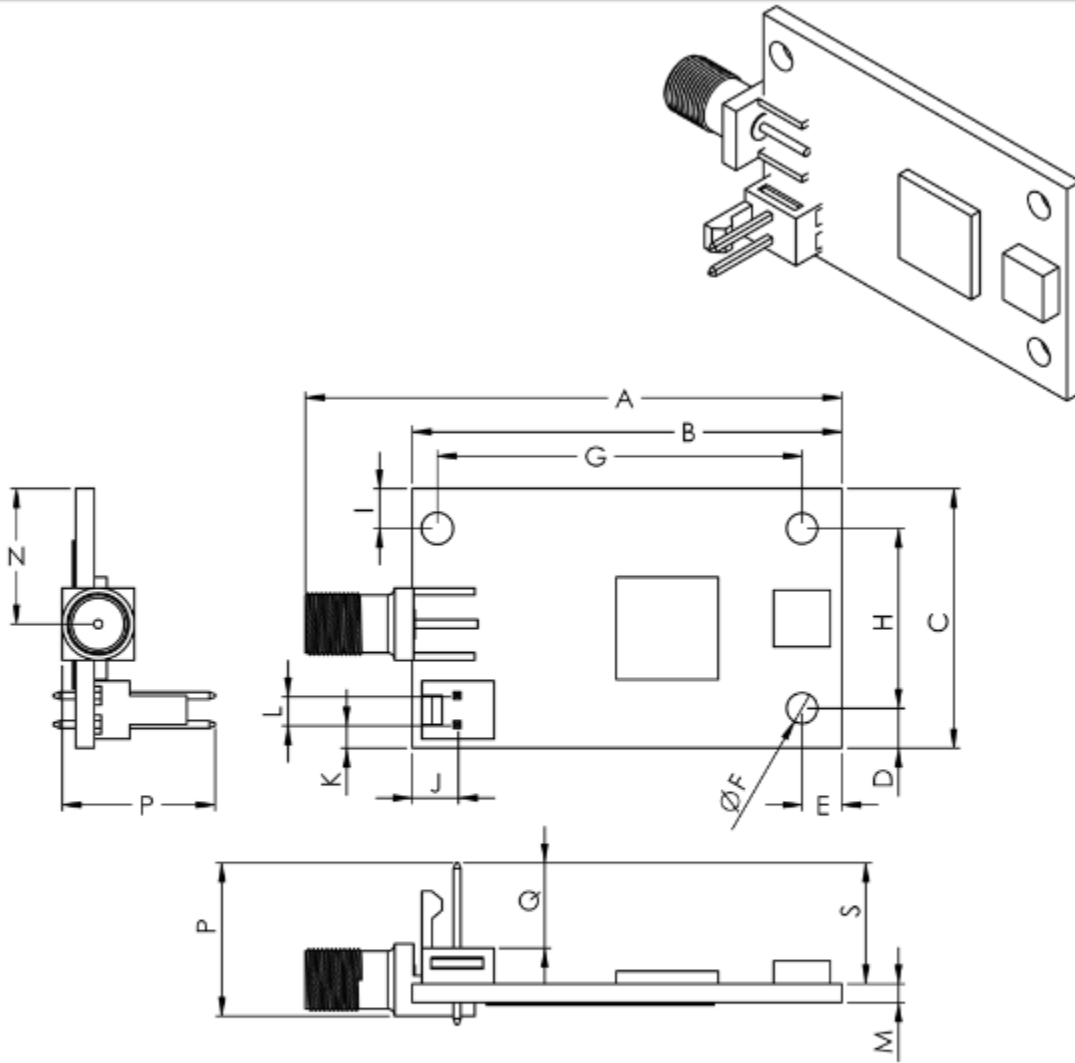For more information on this connector. See Samtec ASP-171959-01

For more information on the SMA Connector, see:
Molex SD-73251-115
Emerson 142-0701-801

Dimension	Typical	Nominal	Minimum	Maximum
A		47.35	46.95	47.75
B		37.80	37.60	38.00
C		22.80	22.60	23.00
D	8.77			
E	7.54			
F	14.6			
G	9.0			
H	3.6			
I	7.14			
J	5.37			
K	4.50			
L	11.40			
M		1.60	1.473	1.727
N	11.40			
P	0.3			
Q	1.0			
S	0.5			
T	1.0			
U	6.0			

Figure 27. 14-Lead Module with Connector Interface
(ML-14-2))
Dimensions shown in millimeters

For more information on the SMA Connector, see:
Molex SD-73251-115
Emerson 142-0701-801

Dimension	Typical	Nominal	Minimum	Maximum
A		47.35	46.95	47.75
B		37.80	37.60	38.00
C		22.80	22.60	23.00
D	3.50			
E	3.50			
F	2.70			
G	30.8			
H	15.8			
I	3.5			
J	3.94			
K	1.27			
L	2.54			
M		1.60	1.473	1.727
N	11.40			
P	13.50			
Q	7.50			
S	10.60			

Figure 28. Remote Sensor with SMA Antenna Interface
(ML-1-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16000AMLZ	−40°C to +85°C	14-Lead Module with Connector Interface and SMA Antenna Interface	ML-14-2
ADIS16COM1/PCBZ		Evaluation Board	
ADIS16229AMLZ	−40°C to +85°C	Sensor Module with SMA Antenna Interface	ML-1-1

[1] Z = RoHS Compliant Part.

NOTES

**ANALOG
DEVICES**

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